Dynamic Analog Testing via ATE Digital Test Channels

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Abstract

A dynamic analog test methodology using digital tester is proposed. A simple triangular waveform is built on the device interface board for the stimulus generation. The response waveform is quantized by the dual comparators in a digital pin electronic circuit. . Statistical analysis is conducted to enhance the quantization resolution and minimize the noise effect. The experimental results using an ATE show that the error is less than 2%. It confirms the feasibility of the proposed methodology.

1. Introduction

System on Chip (SoC) technologies put analog and digital circuitry on the same chip to improve system performance and reduce manufacturing cost. However, it worsens the testing difficulty. For high end applications, such as wireless communications and multi media applications, analog functions are complicated and sensitive. It requires thorough testing procedure. Hence, high end mixed signal testers are often used to verify the not only the function but also the performance. However, for the low end applications, it may not be econmic to use mixed signal testers just for simple analog function verification. Therefore, the development of analog testing techniques using digital means is desirable.

IEEE Std. 1149.4 [1], a standard for mixed signal test buses, targets at the interconnect testing of mixed signal *printed circuit boards* (PCB). It provides digital means to test open short via the use of the built-in comparators. Unfortunately, it cannot test analog function without add-on instrument. [2] proposes an test signal generation using digital testers. Sigma delta modulation is used to generate the desired analog stimuli. However, a digitizer, or mixed signal channel is still required to capture analog responses. [3] uses statistical samplers to capture analog waveforms. But, a powerful *digital signal processing* (DSP) functions is required to obtain the *power spectrum density* (PSD) function of the waveform.

[4] proposes a novel *liquid crystal display* LCD driver testing method based on dual comparators in *pin electronic* (PE) circuits of a digital tester. It is

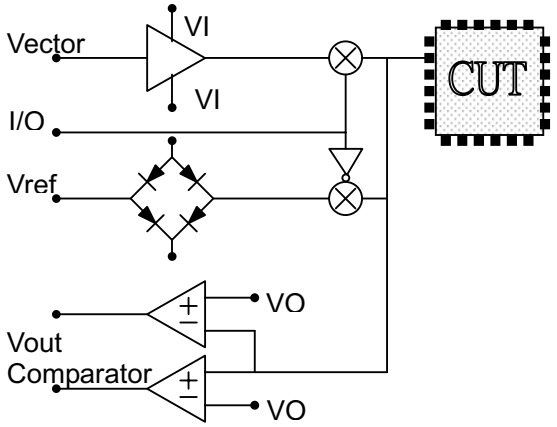

Figure 1. Pin Electronic Interface Circuit

for static testing which measures the DC level only. [5] extends the technique to on-line analog testing by monitoring the quiescent voltage level of analog circuits. None of the above techniques cover the full spectrum of mixed signal testing with stimulus generation and response verification.

In this paper, we would like to propose a dynamic analog test methodology that uses digital test channels only. A triangular (Δ) waveform is generated by a simple stimulus generation module added onto the *device interface board* (DIB) as the test stimulus. The response waveform is compared to two reference voltages by the dual comparators in the PE circuits of digital test channels. The quantized binary read outs of the comparators are analyzed statistically to obtain the amplitude and bias of the response waveform. Based on which, one is able to calculate the gain and offset of the response waveform and determine the correctness of the circuit.

The proposed analog test methodology has the following advantages. First, the replacement of mixed signal test channels by digital ones significantly reduces the test cost. Second, the test time and test accuracy tradeoff can be obtained by the number of samples being taken. Third, as compare to the use of sinusoidal waveforms for the parametric test, the test time is significantly reduced. Forth, through DSP techniques, other parametric properties can also be obtained [3].

In the rest of the paper, the proposed test archi-

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tecture will be presented in Section 2, the mathematical analysis will be outlined in Section 3, the simulation and experimental results will be presented and discussed in Section 4, and finally, the conclusions will be given in Section 5.

2. Test Architecture

The test architecture is composed of test waveform generator and response capture circuitry. As stated earlier, the test stimulus is a triangular waveform. A low cost approach for the triangular waveform generator is to build a simple waveform generator on the DIB. The circuit is as simple as the one shown in Figure 2. A single output channel serves two purposes. First, the switching between high low controls the charge and discharge of the integrator. Hence, the frequency of the triangular waveform is the same as the switching frequency. Second, the high and low output voltages, defined as V_{IH} and V_{IL}, determine the charge and discharge current. The charge and discharge currents are

$$\begin{cases} I_{charge} = (V_{IH} - V_{AGnd})/R \\ I_{discharge} = (V_{AGnd} - V_{IL})/R \end{cases} \quad (1)$$

Here, V_{AGnd} is analog ground which is not necessarily the common ground V_{Gnd}. Suppose that the switch frequency is F_Δ, the frequency of the triangular waveform as well, the amplitude of the waveform is

$$\begin{aligned} V_A &= 0.25 \cdot F_S \cdot (V_{IH} - V_{AGnd})/C \\ &= 0.25 \cdot F_S \cdot (V_{AGnd} - V_{IL})/C \end{aligned} \quad (2)$$

Here we assume that V_{IH} and V_{IL} are symmetric with respect to V_{AGnd}. An alternative approach for the waveform generation is by the use of waveform generation instrument. However, this approach required additional hardware and the synchronization is difficult to achieve.

The response capture circuit is the dual comparator shown in Figure 1. Overall, the test architecture is shown in Figure 3. An output channel is responsible for control the test stimulus waveform generator. On can controls the data rate to control the signal frequency. One can also set V_{IH} and V_{IL} to set the amplitude. An input channel is responsible for capturing the test response waveform. In the next section, we will discuss the statistical analysis technique to obtain the amplitude and offset of the response waveform.

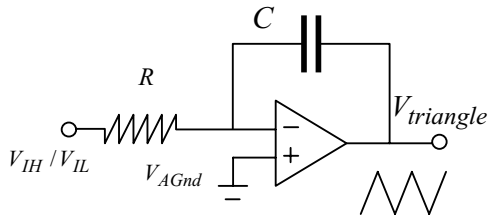

Figure 2, On-board Δ Waveform Generator

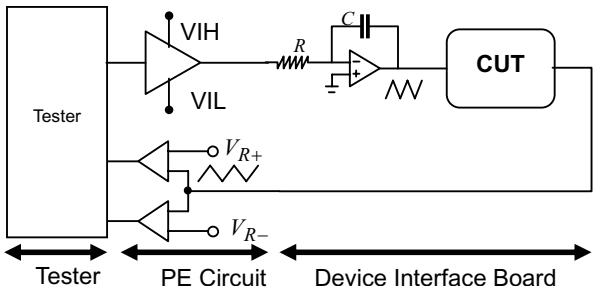

Figure 3, Test architecture

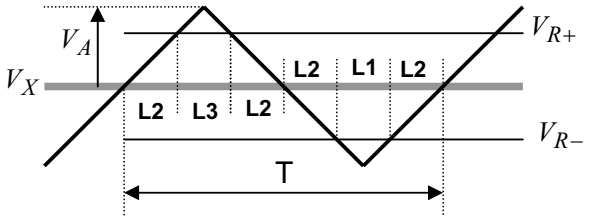

Figure 4, Δ Waveform Compared to V_{R+} V_{R-}.

3. Test Methodology Analysis

3.1 Mathematical Modeling

The proposed analog test methodology uses dualcomparators to compare the responses of triangular stimulus with two reference voltages (V_{R+} and V_{R-}) to obtain the amplitude and bias of the response waveform. From the gain and offset, we are able to determine the gain and offset of the CUT. Figure 4 shows the response waveform and the reference voltages. The triangular response has an offset of V_X and an amplitude of V_A.

When a triangular waveform is compared to two reference voltages, the waveform can be divided into three regions.

$$\begin{cases} L1 : v \le V_{R-} \\ L2 : V_{R-} \le v \le V_{R+} \\ L3 : v \ge V_{R+}. \end{cases} \quad (3)$$

The corresponding time intervals for the regions are

$$\begin{cases} T1 = (0.5 - \dfrac{V_X - V_{R-}}{2V_A})T \\ T2 = \dfrac{V_{R+} - V_{R-}}{2V_A} T \\ T3 = (0.5 - \dfrac{V_{R+} - V_X}{2V_A})T. \end{cases} \quad (4)$$

When the output of the dual comparators are randomly sampled by an asynchronous clock, the probability being in region L1, L2, and L3 are, the ratio of (4) to *T*.

$$\begin{cases} P_{L1} = 0.5 - \dfrac{V_X - V_{R-}}{2V_A} \\ P_{L2} = \dfrac{V_{R+} - V_{R-}}{2V_A} \\ P_{L3} = 0.5 - \dfrac{V_{R+} - V_X}{2V_A}. \end{cases} \quad (5)$$

The above derivation is from the case when V_{R-} and V_A are known. For a waveform under measurement, V_{R-} and V_A are to be determined. Hence the measurement procedure is rather simply. After certain number of samples being taken, we can obtain P_{L1}, P_{L2}, and P_{L3} from the outputs of the dual comparators. Suppose that a total of *N* samples are taken. There are *N1* samples greater than V_{R+} and *N2* samples smaller than V_{R-}. The probabilities can be obtained from

$$P_{L1} = \frac{N2}{N} \quad P_{L2} = \frac{N - N1 - N2}{N} \quad P_{L3} = \frac{N1}{N}. \quad (6)$$

For a typical case, the first case in Figure 8, we can solve the linear equations in (3) to obtain

$$V_A = \frac{V_{R+} - V_{R-}}{2P_{L2}}. \quad (7)$$

$$V_X = V_{R-} \frac{0.5 - P_{L1}}{P_{L2}} (V_{R+} - V_{R-}). \quad (8)$$

In other words, after we obtain P_{L1}, P_{L2}, and P_{L3} using (6), we are able to calculate V_X and V_A by (7) and (8). As a result, we can use the digital approach to measure the amplitude and offset of an analog waveform. Note that, although there are three equations in (5), one of them is redundant because $P_{L1} + P_{L2} + P_{L3} = 1$. A question is raised, how many samples to take in order to have certain accuracy. Note that, Case 2 and 3 in Figure 8 are invalid because there is no solution for V_{R-} and V_A if both of them are unknown.

3.2 Noise Reduction and Analysis

Quantization by a comparator can be regarded as a 1-bit *analog to digital conversion* (ADC). The quantization error is a function of bit length. For 1-bit ADC, the quantization error is very large. We must minimize the error. The quantization by a comparator can be regarded as a binomial trial. The variance is $\sigma^2 = \frac{p \cdot (1-p)}{N}$. p is the probability and N is the number of samples. Suppose that an accuracy of ε is required with 99.7% confidence level, then, N must satisfy the following equation,

$$\varepsilon \geq 3 \cdot \sqrt{\frac{p \cdot (1-p)}{N}}. \quad (9)$$

Note that, (9) achieves quantization error reduction through over sampling. It is also effective for random noise reduction. As we know, the *signal to noise ratio* (SNR) improve 3dB for doubling the over sampling rate. However, in our case, the situation is a little bit different. There are some limits on the noise reduction. Figure 5 shows the case when

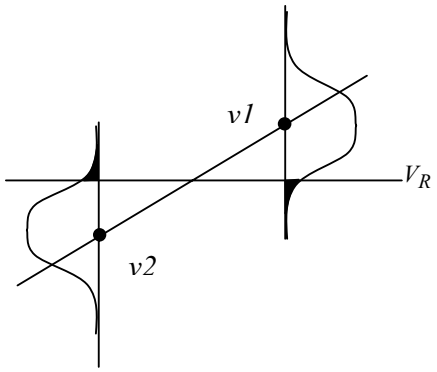

Figure 5, Noise cancellation analysis.

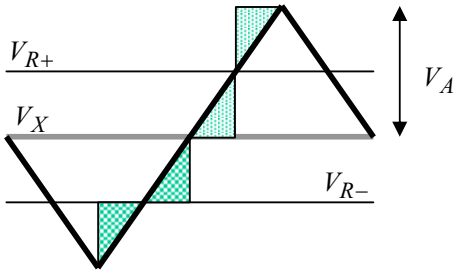

Figure 6, Optimal Noise cancellation.

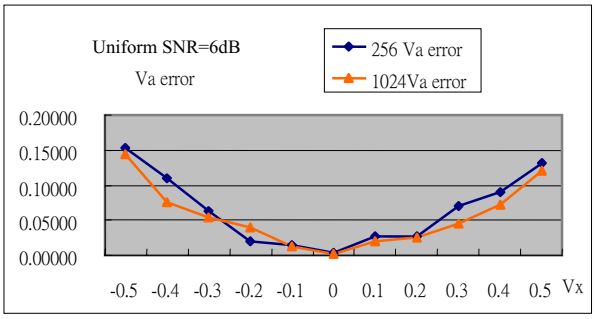

Figure 7, Error as function of Vx.

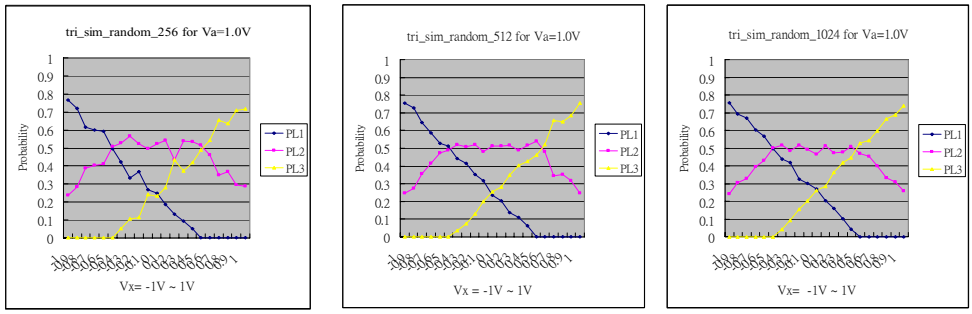

Figure 9, Probabilities obtained by simulation.

the triangular waveform is affected by noise. For the point with voltage *v1*, the probability being judge incorrectly is the area being marked. However, for the voltage *v2*, with the same distance from the reference voltage, it has the same probability for *v2* to be incorrectly judged. Therefore, the errors cancel each other.

After knowing that two points on different side of and with the same distance from the reference voltage can have their noise effects canceled each other, the maximal noise reduction can be obtained by setting the reference voltages to

$$V_{R+} = V_X + 0.5 \cdot V_A \qquad (10)$$
$$V_{R-} = V_X - 0.5 \cdot V_A .$$

There noise cancellation diagram is shown in Figure 6. Under this situation, the noise effects are completely canceled. Figure 7 shows the error as function of V_X. When V_X is 0V, it is the case as shown in Figure 6. The errors are canceled and the error is 0. If V_{R-} is not equal to 0V, there are constant error for the un canceled errors. The further it is offset the larger the error.

4. Simulation and Experimental Results

For simulation, let $V_A = 1V$, $V_{R+} = 0.5V$, and $V_{R-} = -0.5V$. Figure 8 shows the probability of *PL1*, *PL2*, and *PL3* when V_X varies from *-1.0V* to *1.0V* with *0.1V* increment. As expected, PL3 equals to 0 when V_X is less than -0.5V. It increases linearly as V_X increases. *PL2* equals 0.5 when $-0.5V \le V_X \le 0.5V$. Figure 9 shows the cases with 256, 1024, and 4096 samples respectively. As one can see, the more the number of samples are taken, the more accurate it will be.

In order to further verify the test methodology, we use an ATE to implement the proposed test methodology, as shown in Figure 10. The circuit under test is an unit gain buffer implemented by an OP-Amp. We use digital channels of the ATE to capture and quantize the response. The response waveforms have controllable offset and amplitude.

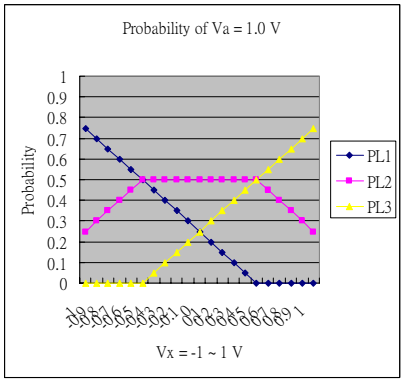

Figure 8, PL1,2,3 by mathematical derivation

Figure 10, Experiment with an ATE.

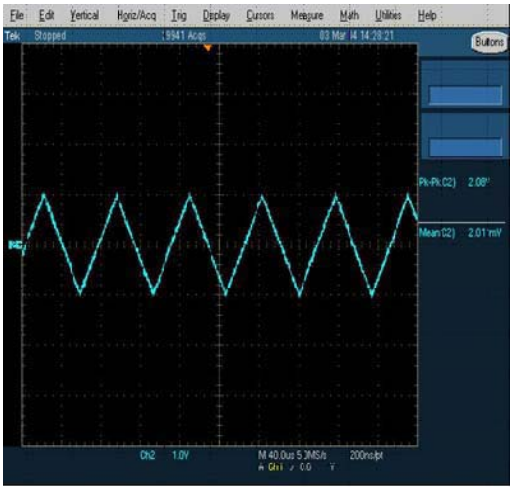

Figure 11, The response waveform

The waveform shown in Figure 11 has an amplitude of 1V and an offset of 0V.

Table 1 shows the overall test results. For all the cases, $V_{R+} = 0.5V$, and $V_{R-} = -0.5V$. The test waveform is programmed to have V_A of 1V, 1.3V, and 1.5V. and V_X varies from -0.5V to 0.5V. The total number of samples being taken is 1024. Figure 12

and 13 shows the error for V_A and V_X. Overall, the error for V_A is less than 2% and the error for V_X is less than 0.01V.

5. Conclusions

In this paper, we have proposed a novel dynamic analog test methodology based digital test channels. A triangular waveform is generated on DIB as test stimulus. The response waveform, also triangular, is quantized by the dual comparators in PE circuits. After the binary quantization, statistical analysis is conducted to obtain the offset and amplitude of the response waveform. In order to verify the feasibility of the methodology, software simulation and ATE implementation have been conducted. Both results reassure the feasibility of the methodology.

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Table 1, Experimental Results ($V_{R\pm} = \pm 0.5V$)

Vx	*Va=1.5V*	*Va=1.3V*	*Va=1.0V*
	Va/Vx	Va/Vx	Va/Vx
-0.5V	1.4971 -0.4942	1.2864 -0.4975	0.9961 -0.4961
-0.4V	1.4841 -0.4043	1.2864 -0.4020	0.9884 -0.3958
-0.3V	1.5095 -0.3029	1.3028 -0.3066	0.9942 -0.2942
-0.2V	1.5025 -0.2067	1.2929 -0.2045	0.9808 -0.2031
-0.1V	1.5148 -0.1035	1.2897 -0.1045	0.9903 -0.0938
0V	1.4884 -0.0087	1.2864 0.0025	0.9827 0.0048
0.1V	1.4841 0.1029	1.2897 0.0995	0.9884 0.1004
0.2V	1.4713 0.1983	1.2864 0.201	0.9903 0.2021
0.3V	1.4841 0.1983	1.2897 0.2985	0.9903 0.2969
0.4V	1.5059 0.4059	1.2832 0.4023	0.9922 0.4031
0.5V	1.5059 0.5000	1.2962 0.4949	1.0059 0.5059

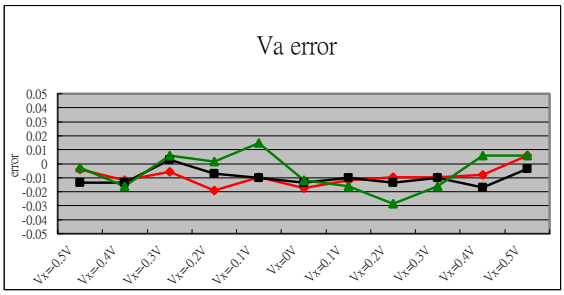

Figure 12, Errors on V_A

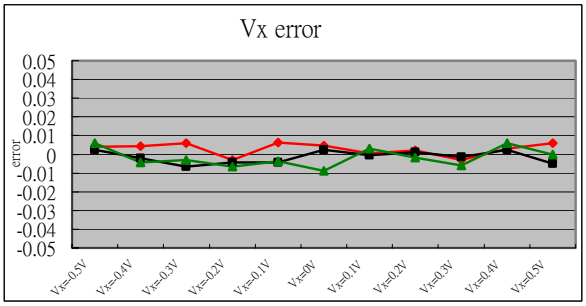

Figure 13, Errors on V_X estimation