An Analytical Model for the Above-Threshold Characteristics of Polysilicon Thin-Film Transistors

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Abstract—**An analytical model for the above-threshold characteristics of long-channel, small-grain and thin channel polysilicon thin film transistors (TFT's) is presented. This model is constructed by considering the barrier potential and the carrier trapping effect at grain boundaries of the channel. A band tail state located at E_c- 0.15 eV is taken into account to simulate the I-V characteristics. Based on the model, the theoretically simulated results show good agreement with the experimental data of the plasma-passivated and unpassivated TFT devices in a wide range of the gate, drain biases and the temperature. The correlation of the transconductance to the gate bias is also investigated. It is found that the decrease of grain-boundary barrier potential with the gate voltage enhances the transconductance, while this enhancement effect becomes insignificant and causes the decrease of the transconductance at the high gate bias.**

NOMENCLATURE

C_{ox}	Gate oxide capacitance, F/cm^2.
E_a	Activation energy of the drain current, eV.
E_c	Conduction band edge of the polysilicon, eV.
E_F	Fermi-level with respect to E_c, eV.
E_{tt}	Grain-boundary tail state level, eV.
E_x	Parallel electric field in channel, V/cm
k	Boltzmann's constant.
L	Device channel length, cm.
L_g	Grain size of the polysilicon channel, cm.
N	Total carrier density in channel, cm^{-3}.
N_A	Acceptor concentration, cm^{-3}.
N_c	Effective density of states in the conduction band, cm^{-3}.
N_D	Donor concentration, cm^{-3}.
$n_{\text{eff}}, n_{\text{eff}}(x)$	Effective free carrier concentration in each grain, cm^{-3}.
N_{tt}	Grain-boundary tail state density, cm^{-2} eV^{-1}.
$n(x)$	Gate-induced carrier(electron), cm^{-3}.
N^*	Critical carrier concentration for grains transformed from fully depleted to partially depleted, cm^{-3}.
p	Hole concentration, cm^{-3}.
q	Elementary charge, 1.602×10^{-19} coul.
T	Absolute temperature, °K.
t_p	Polysilicon channel thickness, cm.
t_{ox}	Gate oxide thickness, cm.
V_d	Drain bias, V.
V_{fb}	Flat-band voltage of TFT, V.
V_{th}	Threshold voltage of TFT, V.
V_g	Gate bias, V.
$V(x)$	Channel potential, which is a function of x, V.
W	Device channel width, cm.
W_d	Width of grain-boundary depletion region, cm.
x	Coordinate perpendicular to the channel, cm.
ε_s	Silicon permittivity.
ε_{ox}	Oxide permittivity.
$\phi(x)$	Potential at grain-boundary depletion region, V.
ϕ_b	Grain-boundary barrier potential, V.
μ_g	Carrier mobility in the grain, cm^2/V · sec.
μ_{gb}	Carrier mobility at the grain boundary, cm^2/V · sec.
μ_0	The prefactor of the grain-boundary mobility, cm^2/V · sec.

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I. INTRODUCTION

RECENTLY, polysilicon thin film transistors (TFT's) have been intensively investigated for the large-area device and VLSI applications [1]. Due to the existence of trap levels at grain boundaries, polysilicon TFT's exhibit a high threshold voltage and a low carrier mobility as compared to single crystal Si(c-Si) MOSFET's [2]–[5], [17]. Although analytical models for the I-V characteristics of polysilicon TFT's have been proposed by many researchers in terms of the potential barrier at grain boundaries, simulated results can not match well with experimental data for a wide range of biases and temperatures [6]–[8]. For a general simulation on polysilicon TFT's, the effect of trap-states located at the midgap was emphasized [6]–[10]. For those models, once the inversion is reached and all traps are filled for a TFT device, any further increase in the gate bias will substantially enhance the channel conductance. However, from the experimental observation, the above-threshold characteristics of polysilicon TFT's is much different that in c-Si MOSFET [11]. In previous investigations [3]–[5], the correlation of trap-states to device characteristics has been established. It is found that the above-threshold characteristics, likely mobility, of a polysilicon TFT is not dependent on the midgap deep-states but on the band tail-states [3]–[5].

In this paper, an analytical model for the I-V characteristics of polysilicon TFT's is developed. It is found that a tail-state

located at the energy level $E_c - 0.15$ eV must be taken into account to simulate the I-V characteristics. The developed model can well simulate experimental data measured on the plasma-passivated and unpassivated TFT devices over a wide range of the gate, drain biases and the temperature. It is shown that the decrease of the drain current is caused by the trappings of the gate-induced free carriers at tail-states. The relationship of the transconductance with the gate voltage can also be explained by this model.

II. The Model

The physical model for the TFT device studied in this work is shown in Fig. 1(a) in its cross-sectional view. Fig. 1(b) and (c) show the energy band diagrams of the grain in the channel under fully depleted and partially depleted conditions respectively. Although the experimental results had demonstrated that the density of defect states in the polysilicon is continuous across the forbidden band gap [12]–[14], in our model, for simplification, only a tail-state level located at $E_c - E_{tt}$ is considered. We do not consider the effect of midgap deep-states on the above-threshold characteristics of polysilicon TFT's because they mainly affect the below-threshold characteristics [3], [5] and the density of deep states is much smaller than that of tail-states [12]–[14]. In one grain, the total charge density per unit volume can be expressed as $\rho = q \cdot N = q \cdot (N_D^+ - N_A^- + p - n)$. By solving Poisson's equation, we obtained that the potential $\phi(x)$ at grain-boundary depletion region is proportional to $N \cdot x^2$ [15], [16]. By using the model proposed by Lu *et al.* [16], we calculated the grain-boundary depletion width W_d and the grain-boundary barrier potential ϕ_b from the trapped carrier areal density on grain boundaries using the Fermi-Dirac statistics and the grain-boundary depletion approximation. From the charge-neutrality condition, the depletion width near the grain boundary can be calculated to be

$$2N \times W_d = \frac{N_{tt}}{1 + \frac{1}{2}\exp[(E_{tt} - E_F + q\phi_b)/kT]}. \quad (1)$$

The critical carrier concentration N^* necessary to transfer the grain from the fully depleted condition to the partially depleted condition can be calculated by setting $2W_d = L_g$.

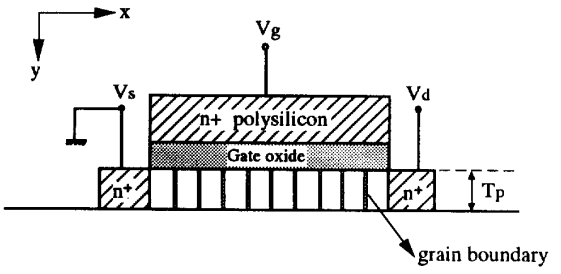
When the grains are fully depleted, the grain-boundary depletion width W_d is equal to L_g and the barrier potential of grain boundaries can be given by [16]:

$$\phi_b = \frac{q \times N \times L_g^2}{8\varepsilon_s}. \quad (2)$$

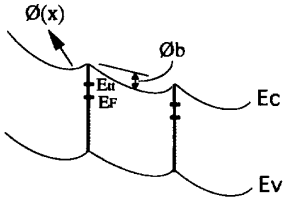
Because some of gate-induced carriers are trapped in grain boundaries, the effective free carrier concentration n_{eff} for conduction in one grain can be determined by integrating the free carrier concentration over one grain:

$$n_{\text{eff}} = \frac{\int_{-L_g/2}^{L_g/2} N_c \exp\left[\frac{-q\phi(x) - E_F}{kT}\right] dx}{L_g}. \quad (3)$$

Based on the symmetrical semiconductor-to-semiconductor junction model [16], the effective free carrier concentration

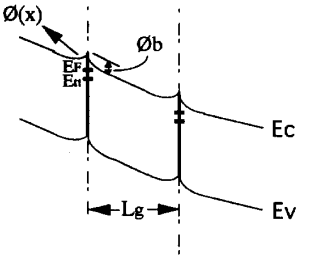


(a)



Fully depleted grain (at low gate bias)

(b)



Partially depleted grain (at high gate bias)

(c)

Fig. 1. The physical structure for the TFT device in (a) its cross-sectional view, and the energy band diagrams of the grain in the channel under (b) fully depleted, and (c) partially depleted conditions, respectively.

can be expressed as [15], [16]

$$n_{\text{eff}} = \frac{N_c \exp(-qE_F/kT)}{qL_g}\left[\frac{2\pi\varepsilon_s kT}{N}\right]^{1/2} \times \text{erf}\left[\frac{qL_g}{2}\left(\frac{N}{2\varepsilon_s kT}\right)^{1/2}\right]. \quad (4)$$

When the grain is partially depleted, the barrier potential of grain boundaries can be expressed as [16]

$$\phi_b = \frac{q \times N \times W_d^2}{2\varepsilon_s}. \quad (5)$$

The effective free carrier concentration for a partially depleted grain becomes [15], [16]

$$n_{\text{eff}} = N_c \exp(-qE_F/kT)\left\{\left(1 - \frac{2W_d}{L_g}\right) + \frac{1}{qL_g}\left[\frac{2\pi\varepsilon_s kT}{N}\right]^{1/2} \text{erf}\left[qW_d\left(\frac{N}{2\varepsilon_s kT}\right]\right)^{1/2}\right\}. \quad (6)$$

TABLE I
THE VALUES OF THE PARAMETERS OF DEVICES USED FOR SIMULATION. THE VALUES OF THE THRESHOLD VOLTAGE FOR THE UNPASSIVATED AND THE PLASMA-PASSIVATED DEVICES WERE EXPERIMENTALLY OBTAINED FROM THE INTERCEPT OF THE $I_d^{1/2} - V_g$ CURVES

Parameters / Conditions	Vth (V)	Ntt (cm^{-2})	Ett (eV)
Unpassivated device	6.3	$2.57 \cdot 10^{12}$	0.15
Plasma-passivated device	0.1	$1.42 \cdot 10^{12}$	0.15

We consider that an N-channel TFT which has an intrinsic polysilicon channel. The same derivation can be applied to a P-channel TFT. For an N-channel TFT, once inversion is reached, $n \gg p$ and $N_D^+ - N_A^- \approx 0$, and the total charged carrier concentration N is approximately equal to the gate-induced carrier (electron) concentration n. The gate-induced carrier concentration per unit volume in the strong-inversion channel can be expressed as

$$n(x) = \frac{C_{\text{ox}}(V_g - V_{\text{th}} - V(x))}{q \times t_p}. \tag{7}$$

In the above, we assumed that the gate-induced carriers occupy uniformly the total polysilicon channel thickness t_p. This is true for a thin film SOI MOSFET with a small Si film thickness (< 500 Å) and a sufficiently low doping concentration (< 10^{15} cm^{-3}). For this case, the electrostatic potential inside the Si film is nearly constant [19].

In the polysilicon channel, the channel mobility is contributed both by the grain mobility μ_g and by the grain boundary mobility μ_{gb}, i.e. it can be empirically described as [6], [8], [9]

$$\begin{aligned}\mu^{-1} &= \mu_g^{-1} + \mu_{gb}^{-1} \\ &= \mu_g^{-1} + [\mu_0 \exp(-q\phi_b/kT)]^{-1} \\ &\approx [\mu_0 \exp(-q\phi_b/kT)]^{-1}.\end{aligned} \tag{8}$$

In the above, μ_{gb} is the dominant one [20] and exhibits an activation energy $q\phi_b$ and can be expressed as $\mu_0 \times \exp(-q\phi_b/kT)$ [6], [8].

Using the gradual channel approximation, the current voltage relationship of the polysilicon TFT with a channel length L and a width W in the region of $V_g - V_{\text{th}} > V_d$ can be calculated as

$$\begin{aligned}I_d = \frac{W}{L} \int_0^{V_d} & C_{\text{ox}}(V_g - V_{\text{th}} - V(x)) \\ & \times \mu_0 \times \exp(-q\phi_b/kT) \times dV(x).\end{aligned} \tag{9}$$

In (9), the grain-boundary barrier potential ϕ_b is calculated from (2) or (5), and all the gate-induced carrier are considered to conduct in the channel. Since some of the free charges are trapped in the grain boundary, we replace $n(x)$ by $n_{\text{eff}}(x)$. Equations (4) and (6), instead of (1), are used and (9) can then be rederived to be

$$I_d = q\frac{W}{L} \int_0^L n_{\text{eff}}(x) \times t_p \times \mu_0 \times \exp(-q\phi_b/kT) \times E_x \times dx \tag{10}$$

where the effective free carrier concentration, $n_{\text{eff}}(x)$, is a function of x because the channel potential $V(x)$ in (7) is varied from the source end to the drain end. Assuming that the channel potential at $V_g - V_{\text{th}} > V_d$ is linearly dependent on the drain bias [21] and the $E_x = V_d/L$, the gate-induced carrier concentration can be expressed as

$$n(x) = \frac{C_{\text{ox}}(V_g - V_{\text{th}} - V_d \times x/L)}{q \times t_p}. \tag{11}$$

From (4), (6), (10) and (11), the relationship of I_d to V_g and V_d can be calculated.

At small drain bias, the gate-induced carriers are assumed to be uniformly distributed in the x-direction and (10) can be simplified as

$$I_d = q \times \frac{W}{L} \times t_p \times n_{\text{eff}} \times V_d \times \mu_0 \times \exp(-q\phi_b/kT). \tag{12}$$

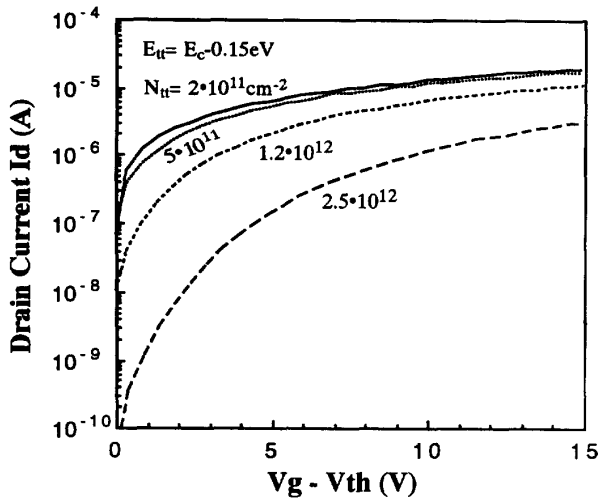


Fig. 2. The simulated $I_d - V_g$ curves for the devices with (a) different trap-state densities, and (b) different trap energy levels. The device dimension for this simulation is $W/L = 40\,\mu\text{m}/10\,\mu\text{m}$.

III. Results and Discussions

A. I-V Characteristics

Fig. 2(a) and (b) show the simulated $I_d - V_g$ curves at $V_d = 0.1$ V for the devices with different trap-state densities and trap energy levels respectively. The simulated curves were calculated by (12). It is clearly seen that the drain current is dependent on the trap-state density and also on the trap energy level location. The higher the trap-state density is and the closer to the midgap the trap energy level is and the smaller the drain current is. In Fig. 2(b), there is not much difference on the drain currents if the trap-level is below $E_c - 0.2$ eV. To verify the derived model, coplanar structure N-channel polysilicon TFT's were fabricated on thermally oxidized silicon substrates. The polysilicon channel thickness was 430 Å and the gate oxide thickness was 385 Å. The grain size of the polysilicon channel was about 2000 Å by Transmission Electron Microscopy (TEM) observation. Among the experimental devices, some of them were subjected to H_2-plasma treatment to passivate the trap-state density. The details of the fabrication process were described in [22]. Fig. 3 shows the $I_d - V_d$ plot for different gate voltages for a plasma-passivated device, where the solid curves are theoretically computed curves and the dotted data are the experimentally measured values. All devices were measured and simulated $W/L = 40\,\mu\text{m}/10\,\mu\text{m}$. The theoretical curves in Fig. 3 were calculated by (10). It can be seen that the theoretical data and the experimental curve fit very well. In fitting the theoretical data with the experimental curves, the value of N_{tt} and its location needed to be determined. The N_{tt} value obtained from this fitting was 1.42×10^{12} cm^{-2} and its location was at $E_c - 0.15$ eV. The prefactor of the grain boundary mobility μ_0 is 30 cm^2/V · sec. Fig. 4 shows another two fitting curves for the drain currents at $V_d = 0.1$ V versus $(V_g - V_{\text{th}})$ for two devices, where one is a plasma-passivated device and the other is an unpassivated device, and the theoretical data were computed from (12). Also, very good fittings are obtained and the values for N_{tt}, E_{tt} and V_{th} used were those listed in Table I, where the V_{th} values were experimentally obtained from the intercept of the $I_d^{1/2} - V_g$ curves of the device. It is seen that the trap-state density was reduced from 2.57×10^{12} cm^{-2} to 1.42×10^{12} cm^{-2} after hydrogenation, while the location of the trap-state level was unchanged. Fig. 5 shows the I_d plots for the same plasma-passivated device but for two different temperatures 22°C and 100°C. In this figure, the N_{tt} value and its location were kept the same and the I_d's are plotted in a linear scale in the range of $0 - 12 \times 10^{-6}$ A. 10 Good fittings are also obtained for the theoretical curves and the experimental data. In order to further study the temperature effect on our proposed model, the activation energies for the drain currents of the plasma-passivated and the unpassivated devices were measured and derived. The I_d's were measured at the temperature range from 22–150°C and the activation energies of their variations with respect to the temperature were deduced for different applied gate voltages. The results are shown in Fig. 6. For comparison, the theoretical curves derived based on the Levinson's model [6] are also included

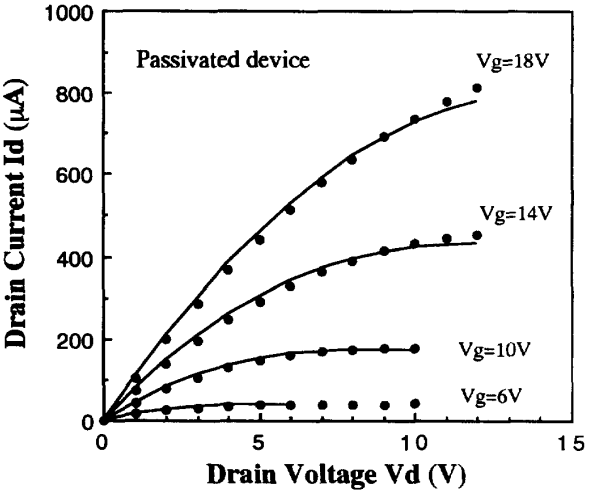


Fig. 3. The theoretically simulated and experimental $I_d - V_d$ characteristics for a plasma-passivated device. The solid lines represent the simulated result and the dots represent the experimental data.

in the figure. For our model, the activation energy of the drain current was calculated from (10) as $E_a \equiv (\partial \ln(I_d)/\partial T) \cdot q/k$. For the Levinson's model, the activation energy of the drain current is equal to the barrier potential of the grain boundary: $E_a \equiv qN_t^2/8\varepsilon_s n = q^2 N_t^2 t_p/8\varepsilon_s C_{\text{ox}}(V_g - V_{\text{th}})$, where N_t is the midgap areal trap-state density at the grain boundary. In Fig. 6, our model shows a good agreement with the experimental data, while the Levinson's model seems to overestimate the values, especially at the low $V_g - V_{\text{th}}$ bias, which is the same as the report of [23]. For our model, as the device is just turned on, the position of Fermi-level at the grain boundary is still below the position of the trap energy level at the grain boundary as shown in Fig. 1(b), where the trap-states are partially charged. While, in the Levinson's model, only the midgap deep-states are considered. As the device is turned on, the deep-states are fully charged, which causes a large grain-boundary barrier potential. As a result, the activation energy is overestimated. This overestimation of the activation energy also causes the underestimation of the drain current at the low gate voltage as reported in [8].

In addition, the ratios of the effective free carrier concentration to the gate-induced carrier concentration calculated from our model for the two devices of Fig. 4 are plotted in Fig. 7 as a function of the gate voltage. It is seen that for the unpassivated device with a larger N_{tt}, this n_{eff}/n ratio is smaller, especially at the low $V_g - V_{\text{th}}$ bias. Even at a large $V_g - V_{\text{th}}$ bias (> 10 V), the effective free carrier concentration is still 5% smaller than the gate-induced carrier concentration. This means that for a polysilicon TFT with a large trap-state density N_{tt}, beside the relatively large barrier potential of grain boundaries, which affects the mobility of the carriers, the small effective carrier concentration is also a factor which reduces the drain current of the device.

B. $g_m - V_g$ Characteristics

An important device characteristic is transconductance which is used to calculate the field effect mobility. It is

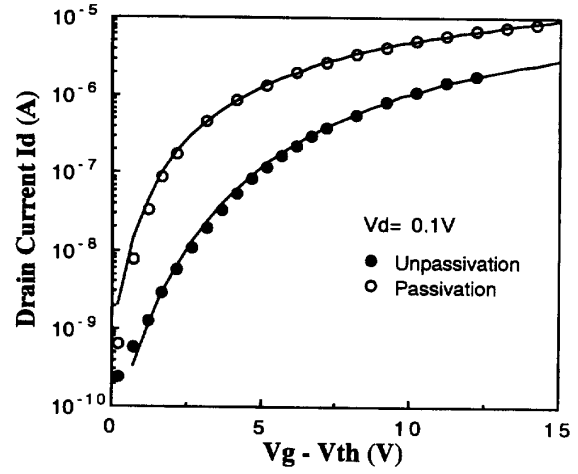


Fig. 4. The simulated and experimental $I_d - V_g$ characteristics at $V_d = 0.1$ V for an unpassivated and a plasma-passivated devices. The solid line represent the simulated result and the dots represent the experimental data. The values of the fitting parameters: N_{tt} and E_{tt} are shown in Table I.

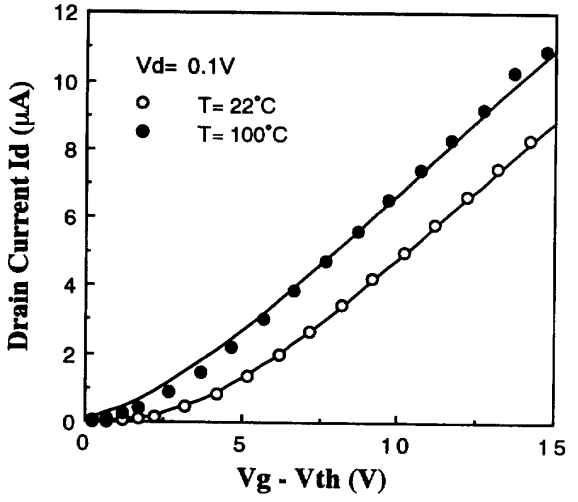


Fig. 5. The simulated and experimental $I_d - V_g$ characteristics at $V_d = 0.1$ V for a plasma-passivated device operated at 22 and 100°C. The solid lines represent the simulated result and the dots represent the experimental data.

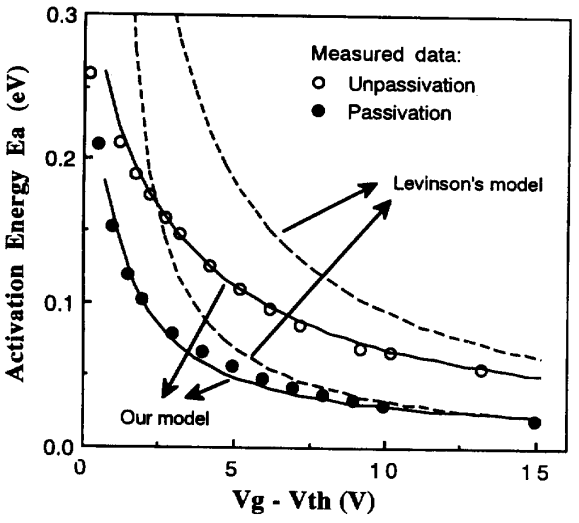


Fig. 6. The simulated and experimental results of the activation energy of the drain current of the unpassivated and the plasma-passivated devices. The solid curves are the theoretical curves, the dots are the experimental data, and the dashed curves are the theoretical curves computed from the Levinson's model.

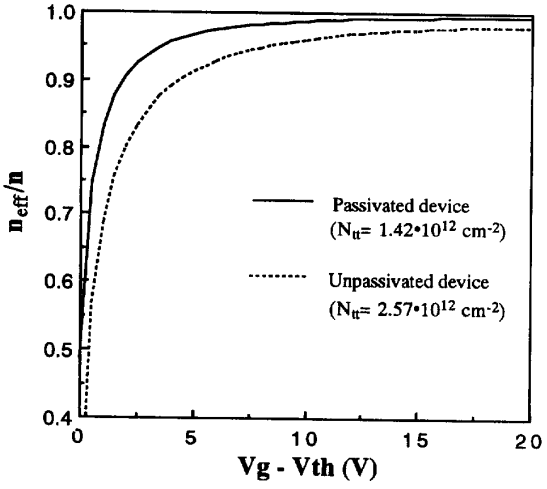


Fig. 7. The simulated effective free carrier concentration for the plasma-passivated and unpassivated devices.

defined as

$$g_m = \frac{\partial I_d}{\partial V_g} | V_d = \text{constant}. \tag{13}$$

We place (12) into (13) and obtain an analytical expression for the transconductance:

$$g_m = q\frac{W}{L} t_p V_d \mu_0 \cdot \exp(-q\phi_b/kT) \cdot \left(\frac{\partial n_{\text{eff}}}{\partial V_g}\right) + q\frac{W}{L} t_p V_d n_{\text{eff}} \mu_0 \cdot \exp(-q\phi_b/kT) \cdot \left(\left(-\frac{q}{kt}\right) \cdot \frac{\partial \phi_b}{\partial V_g}\right). \tag{14}$$

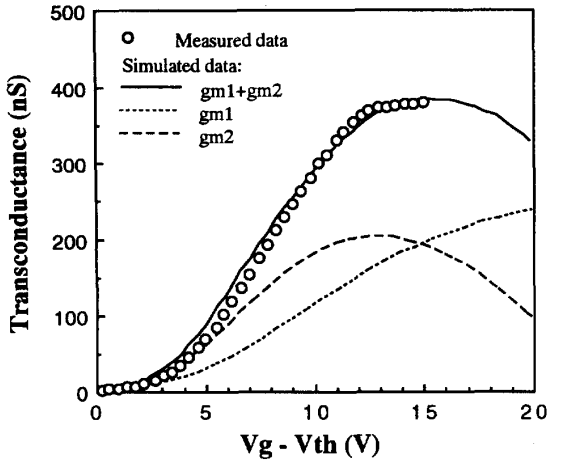
Clearly, the transconductance comprises of two components. They are

$$g_{m1} = q\frac{W}{L} \cdot t_p \cdot V_d \cdot \mu_0 \exp(-q\phi_b/kT) \cdot \left(\frac{\partial n_{\text{eff}}}{\partial V_g}\right) \tag{15}$$

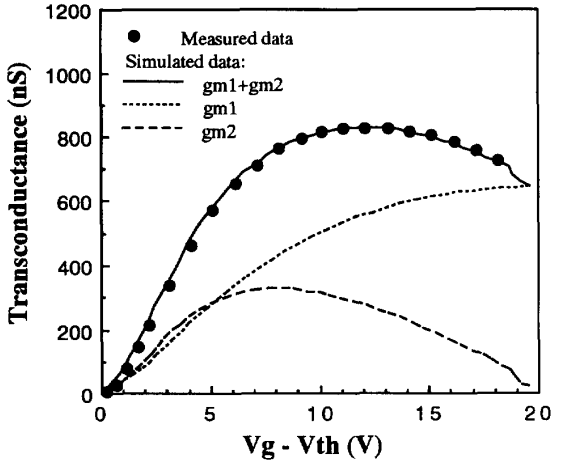
and

$$g_{m2} = q\frac{W}{L} \cdot t_p \cdot V_d \cdot n_{\text{eff}} \cdot \mu_0 \exp(-q\phi_b/kT) \cdot \left(\left(-\frac{q}{kT}\right) \cdot \frac{\partial \phi_b}{\partial V_g}\right), \tag{16}$$

respectively. The total transconductance is $g_m = g_{m1} + g_{m2}$. In (14) and (16), a discontinuity at the transition point of $N = N^*$



(a)



(b)

Fig. 8. The simulated curves and experimental data for the transconductances at $V_d = 0.1$ V as a function of gate biases for (a) the unpassivated device, and (b) the plasma-passivated device.

exists. While, at this point of small $V_g - V_{\rm th}$, the g_m value is too small to be considered.

It is noted that g_{m1} is related to the change of the effective free carrier concentration with respect to V_g, while g_{m2}, which is not observed in the single crystal Si MOSFET, is related to the change of the barrier potential of grain boundaries with respect to the gate bias. In other words, g_{m2} is caused by the gate-bias-induced grain-boundary barrier lowering. Fig. 8(a) and (b) show the plots of g_{m1}, g_{m2} and the total $g_m = g_{m1} + g_{m2}$ for the unpassivated and passivated devices respectively, where the experimental dots are also included. The theoretically computed curves agree with the experimental data very well. The transconductance increases first with the applied Vg and then decreases. In addition, the gate voltage where g_m reaches the maximum increases with N_{tt} because the gate-induced carrier concentration required to screen the potential barrier is increased. From Fig. 8, it is observed that the decrease of g_m is due to the decrease of g_{m2}. The component g_{m2} in the transconductance is caused by the effect of the grain-boundary barrier potential decrease with the gate voltage. At the low gate voltage, the grain-boundary barrier potential decreases with the gate voltage. However, as the gate voltage reaches a value such that the Fermi-level at the grain boundary is above the trap level, the decrease of the grain-boundary barrier potential will become increasingly small. That is, the value of the $-\partial\phi_b/\partial V_g$ term in (14) becomes smaller. This is the reason that g_{m2}, consequently g_m in Fig. 8, decrease as the $V_g - V_{\rm th}$ is above 8 V. It is interesting to note that when the transconductance is used to calculate the field effect mobility, the field effect mobility will decrease at high gate bias even when no vertical electric field-induced scattering is considered [24].

IV. Conclusion

In this paper, an analytical model for the above-threshold characteristics of long-channel, small-grain and thin channel polysilicon TFT's has been presented. In the model, a tail-level located at the position of $E_c - 0.15$ eV is considered. As a result of the inclusion of this trap level, the derived model can fit the I-V characteristics of the polysilicon TFT's in a wide range of the gate, drain voltages and the temperature. Also, the model can explain the behavior of the transconductance of the devices. At the low gate bias, g_m increases with the gate bias due to the increase of the gate-induced free carrier concentration and the gate-bias-induced grain-boundary barrier lowing. At the high gate bias, g_m decreases since the gate-bias-induced grain-boundary barrier lowing decreases.

References

[1] I. Yudasaka and H. Ohshima, "Polysilicon thin film transistors," *Mat. Res. Soc. Symp. Proc.*, vol. 182, p. 333, 1990.
[2] T. I. Kamins and P. J. Marcoux, "Hydrogenation of transistor fabricated in polysilicon films," *IEEE Electron Device Lett.*, vol. EDL–1, p. 159, 1980.
[3] H. N. Chern, C. L. Lee, and T. F. Lei, "Correlation of polysilicon thin film transistor characteristics to defect states via thermal annealing," *IEEE Trans. Electron Devices*, vol. 41, pp. 460–462, Mar. 1994.
[4] K. Ono, T. Aoyama, N. Konishi, and K. Miyata, "Analysis of current-voltage characteristics of low-temperature-processed polysilicon thin film transistor," *IEEE Trans. Electron Devices*, vol. 39, p. 792, 1992.
[5] I.-W. Wu, T. Y. Huang, W. B. Jackson, A. G. Lewis, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett.*, vol. 12, p. 181, 1991.
[6] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys.*, vol. 53, p. 1193, 1982.
[7] H. Baudrand, E. Hamadto, and J. L. Amalric, "An experimental and theoretical study of polycrystalline thin film transistors," *Solid-State Electron.*, vol. 24, p. 1093, 1982.
[8] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, "A model of current-voltage characteristics in polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. ED-34, p. 321, 1987.
[9] F. Qian, D. M. Kim, H. K. Park, and J. L. Sachitano, "Inversion-mode MOSFET's in polycrystalline silicon thin films: Characterization and modeling," *IEEE Trans. Electron Devices*, vol. ED–35, p. 2439, 1987.
[10] J. G. Fossum and A. Ortiz-Conde, "Effects of grain boundaries on the channel conductance of SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, p. 933, 1983.
[11] S. Koyama, "A novel cell structure for giga-bit EPROMs and flash memories using polysilicon thin film transistors," *1992 Symp. on VLSI Tech., Tech. Digest*, pp. 44–45.

[12] H. J. Queisser and J. Werner, "Electrical and electronical properties of grain boundaries in silicon," *Mat. Res. Soc. Symp. Proc.*, vol. 106, p. 53, 1988.
[13] W. B. Jackson, N. M. Johnson, and D. K. Biegeisen, "Density of gap states of silicon grain boundaries determined by optical absorption," *App. Phys. Lett.*, vol. 43, p. 196, 1983.
[14] J. R. Ayres, "Characterization of trapping states in polycrystalline-silicon thin film transistors by deep level transient spectroscopy," *J. Appl. Phys.*, vol. 74, p. 1787, 1993.
[15] G. Baccarani, B. Ricco, and G. Spadin, "Transport properties of polycrystalline silicon films," *J. Appl. Phys.*, vol. 49, p. 5565, 1978.
[16] N. C. C. Lu, L. Gerzberg, C. Y. Lu, and J. D. Meindl, "Modeling and optimization of monolithic polycrystalline silicon resistors," *IEEE Trans. Electron Devices*, vol. ED–28, p. 818, 1981.
[17] A. G. Lewis, I-W. Wu, T. Y. Huang, M. Koyanagi, A. Chiang, and R. H. Bruce, "Small geometry effects in N- and P-channel polysilicon thin film transistors," *IEDM'88 Tech. Dig.*, 1988, p. 260.
[18] R. E. Proano, R. S. Misage, and D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, p. 1915, 1989.
[19] F. Balestra, M. Benachir, J. Brini, and G. Ghibaudo, "Analytical models of subthreshold swing and threshold voltage for thin and ultra-thin film SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 37, no. 11, pp. 2303, 1990.
[20] C. W. Wu and E. S. Yang, "Physical basis of scattering potential at grain boundary of polycrystalline semiconductors," *Appl. Phys. Lett.*, vol. 40, p. 49, 1982.
[21] S. Shirai and T. Serikawa, "Electrical analysis of high-mobility poly-si TFT's made from laser-irradiated sputtered si films," *IEEE Trans. Electron Devices*, vol. 39, p. 450, 1992.
[22] H. N. Chern, C. L. Lee, and T. F. Lei, "H_2/O_2 plasma on polysilicon thin-film transistor," *IEEE Electron Device Lett.*, vol. 14, p. 115, 1993.
[23] T. Katoh and N. Hirashita, "Effects of trap state on field-effect mobility of MOSFET's formed on large-grain polysilicon films," *Jpn. J. Appl. Phys.*, vol. 28, p. L2291, 1989.
[24] S. Seki and B. Tsujiyama, "A semi-empirical model for the field-effect mobility of hydrogenated polycrystalline-silicon MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-35, p. 669, 1988.

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