Complementary-SCR ESD Protection Circuit with Interdigitated Finger-Type Layout for Input Pads of Submicron CMOS IC's

Ming-Dou Ker, *Member, IEEE,* and Chung-Yu Wu, *Member, IEEE,*

***Abstract*— A new ESD protection circuit with complementary SCR structures and junction diodes is proposed. This complementary-SCR ESD protection circuit with interdigitated finger-type layout has been successfully fabricated and verified in a 0.6-μm CMOS SRAM technology with LDD process. The proposed ESD protection circuit can be free of VDD-to-VSS latchup issue under 5-V VDD operation by means of base-emitter shorting method. To compensate the degradation on latching capability of lateral SCR devices in the ESD protection circuit caused by base-emitter shorting method, the p-well to p-well spacing of lateral BJT's in the lateral SCR devices is reduced to lower its ESD-trigger voltage and to enhance turn-on speed of positive-feedback regeneration in the lateral SCR devices. This ESD protection circuit can perform high ESD failure threshold in a small layout area, so it is very suitable for submicron CMOS VLSI/ULSI's in high-pin-count or high-density applications.**

I. Introduction

In CMOS IC's, the total layout area of a high-pin-count chip is usually dependent on the pitch of input or output pads with ESD (Electrostatic Discharge) protection circuits. If layout area of each pad with ESD protection circuit is reduced, the total layout area of a whole chip can be reduced as well as the parasitic resistances and capacitances at each pad also reduced to perform higher operating speed. So, an efficient ESD protection circuit which has high ESD failure threshold in a small layout area is much demanded by submicron CMOS VLSI/ULSI's.

Recently, the lateral SCR device has been used as a main protection element in CMOS on-chip ESD protection circuits [1]–[16], because the ESD robustness of thin-oxide and thick-oxide NMOS devices is much degraded by the LDD (Lightly-Doped Drain) structure, graded junction, and silicide diffusion of advanced submicron CMOS technologies [17]–[27]. The lateral SCR device can sustain highest ESD stress in a smallest layout area as compared to other ESD protection elements in submicron CMOS technologies. But, the switching voltage of lateral SCR devices without modifying their structures in submicron CMOS technologies is around 30 $\sim$ 50 V. Such lateral SCR devices can only work as primary protection elements and need the cooperation of other secondary protection elements to achieve ESD protection for input pins of submicron CMOS IC's [1]–[8]. But, secondary protection elements need additional layout area and interconnection, which also increase layout area of an input pad with such ESD protection circuit. If ESD-trigger voltage of lateral SCR devices can be lowered to appreciate voltage levels [9]–[16], it can perform very effective ESD protection alone without the help of secondary protection elements, as well as the layout area of input pad with ESD protection circuit can be further reduced.

Since ESD voltages may have positive or negative polarities to both VDD and VSS(ground) nodes, there are four modes of ESD stresses at each pin:

1) PS mode: ESD stress at a pin with positive voltage polarity to VSS(GND) pin when VDD pin is floating;
2) NS mode: ESD stress at a pin with negative voltage polarity to VSS(GND) pin when VDD pin is floating;
3) PD mode: ESD stress at a pin with positive voltage polarity to VDD pin when VSS(GND) pin is floating;
4) ND mode: ESD stress at a pin with negative voltage polarity to VDD pin when VSS(GND) pin is floating.

These ESD voltages could damage both NMOS and PMOS devices in the internal circuits of CMOS IC's. In [1]–[12], the lateral SCR device with or without secondary protection elements is only arranged from the input (or output) pad to VSS(GND). There is no ESD protection element arranged between the pad and VDD. For an ESD event happening between the input and VDD pins especially in the ND-mode ESD stress, ESD current/voltage is first diverted from input pad to VSS power line of CMOS IC through input-to-VSS ESD protection circuit with lateral SCR device. The ESD current/voltage flows along VSS power line which is ordinarily surrounding the whole chip, and then it flows through VDD-to-VSS ESD protection element to VDD power line. Along VDD power line, ESD current/voltage finally goes out of CMOS IC from a VDD pin. Due to parasitic resistance and capacitance of VSS and VDD power lines in CMOS IC's as well as voltage drops on input-to-VSS and VDD-to-VSS ESD protection elements, such nondirect ESD discharging path had been reported to cause some unexpected ESD damages on internal circuits beyond ESD protection circuits [28]–[30].

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The authors are with the Integrated Circuits and Systems Laboratory, Institute of Electronics and Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu 300, Taiwan, Republic of China.

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Thus, an effective ESD protection circuit for input pins of advanced submicron CMOS IC's should perform direct ESD discharging paths from the input pad to both VDD and VSS(GND) to avoid unexpected ESD stress on internal circuits [31].

To overcome above issue of nondirect ESD discharging path and to employ the advantage of high ESD protection capability of lateral SCR device with small layout area, a new complementary-SCR (CSCR) ESD protection circuit is proposed in this paper for the input pins of CMOS IC's with four direct and efficient ESD discharging paths to avoid the unexpected ESD damages on internal circuits.

II. Complementary-SCR (CSCR) ESD Protection Circuit

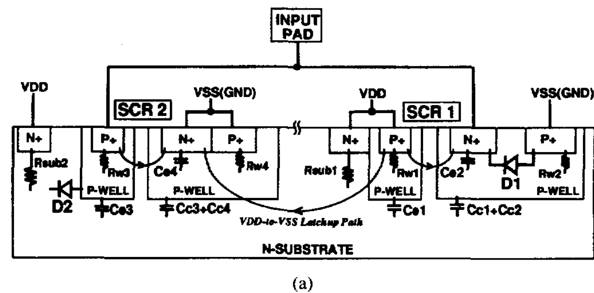
A. Complementary SCR Structures

The schematic cross-sectional view of the complementary SCR structures is shown in Fig. 1(a), where the n-substrate p-well CMOS process is used to demonstrate the complementary SCR structures. The corresponding lumped equivalent circuit of complementary SCR structures is shown in Fig. 1(b). There are two lateral SCR structures in this CSCR ESD protection circuit. The SCR1 device is arranged between VDD and input pad with its anode connected to VDD. The SCR2 device is arranged between input pad and VSS(GND) with its anode connected to the pad. The SCR1 (SCR2) device is basically formed by the parasitic lateral p-n-p bipolar junction transistor (BJT) $Q1$ ($Q3$) and parasitic vertical n-p-n BJT $Q2$ ($Q4$). $Q1$ and $Q3$ are parasitic lateral p-well/n-substrate/p-well BJT's, whereas $Q2$ and $Q4$ are parasitic vertical $N+$ diffusion/p-well/n-substrate BJT's. In lateral p-n-p BJT $Q1$ ($Q3$), p-well instead of $P+$ diffusion is used as its emitter to make a deeper anode structure for lateral SCR1 (SCR2) device. The deeper anode can allow higher current flowing capability to bypass ESD currents so as to increase its ESD failure threshold.

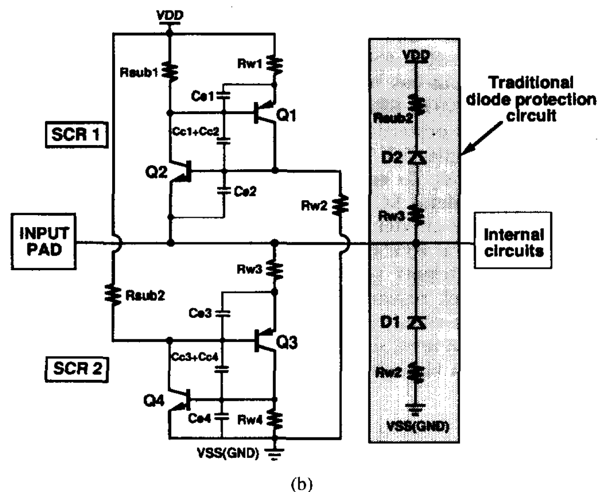
In the complementary SCR structures, there also exist two junction diodes $D1$ and $D2$. These two junction diodes are merged into the base-emitter junctions of BJT's $Q2$ and $Q3$ to save layout area. The diode $D1$ is formed by an $N+$ diffusion in a p-well, whereas the diode $D2$ is formed by a p-well in n-substrate.

The parasitic resistances and capacitances in complementary SCR structures are also shown in Fig. 1(a) and (b). $Rw1, Rw2, Rw3$, and $Rw4$ represent p-well inherent resistances. Rsub1 and Rsub2 are substrate inherent resistances. $Ce1, Cc1 + Cc2, Ce3$, and $Cc3 + Cc4$ are p-well/n-substrate junction capacitances. $Ce2$ and $Ce4$ are $N+$ diffusion/p-well junction capacitances. These capacitances have important effects to lower the ESD-trigger voltage of lateral SCR device [13], [14].

The cross-sectional view and lumped equivalent circuit shown in Fig. 1(a) and 1(b) are the implementation of this CSCR ESD protection scheme by a n-substrate/p-well CMOS process. This CSCR ESD protection scheme can also be implemented in a p-substrate/n-well CMOS process as well if appropriate modifications are made.



(a)



(b)

Fig. 1. (a) The schematic cross-sectional view of the CSCR ESD protection circuit. (b) The lumped equivalent circuit of the CSCR ESD protection circuit.

B. Operating Principles

In normal CMOS operations with 5-V VDD and 0-V VSS(GND), diodes $D1$ and $D2$ have a voltage-clamping effect on input signals. The input voltage level is limited approximately between -0.6 V and $+5.6$ V. The lateral SCR1 and SCR2 devices under normal operating conditions are in their high-impedance (off) states. Although diode $D1$ ($D2$) is merged into the emitter of BJT $Q2$ ($Q3$) in lateral SCR1 (SCR2) device, the current flowing path through diode $D1$ ($D2$) and that through SCR1 (SCR2) device in the cross-sectional view of Fig. 1(a) are different. So, if diode $D1$ ($D2$) is forwardly conducting due to input signals undershooting (overshooting) to clamp input voltage level on the pad, the lateral SCR1 (SCR2) device is still not triggered on by the forward-biased diode $D1$ ($D2$).

In ESD stress conditions, there are four ESD-stress cases at the input pad with positive or negative polarities to VDD or VSS(GND). In NS-mode (PD-mode) ESD stress, diode $D1$ ($D2$) is forwardly conducting to bypass ESD current but SCR2 (SCR1) device is off. On the contrary, SCR2 (SCR1) device is triggered on to bypass ESD current but $D1$ ($D2$) diode is off in PS-mode (ND-mode) ESD stress. The lateral SCR2 (SCR1) device is designed to be triggered on before breakdown of diode $D1$ ($D2$) during ESD transitions. Because diodes $D1$ and $D2$ are not arranged to perform ESD

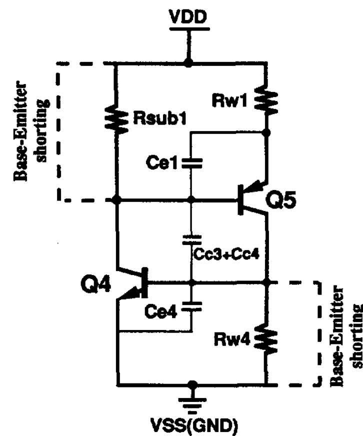


Fig. 2. The lumped equivalent circuit of the VDD-to-VSS latchup path.

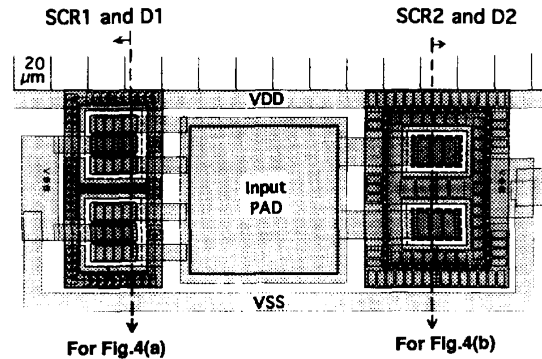


Fig. 3. The interdigitated finger-type layout of the CSCR ESD protection circuit.

protection in their reverse-biased breakdown conditions during ESD transitions, the ESD protection capability of this proposed ESD protection circuit can be improved significantly within a small layout area.

C. VDD-to-VSS Latchup Consideration

There is a parasitic VDD-to-VSS latchup path in the CSCR ESD protection circuit, which is also shown in Fig. 1(a). The corresponding lumped equivalent circuit of this VDD-to-VSS latchup path is shown in Fig. 2. In Fig. 2, the parasitic vertical $Q4$ transistor is the same of BJT $Q4$ in SCR2 structure. But, the parasitic lateral $Q5$ transistor is formed by the p-well emitter of BJT $Q1$ in SCR1 device as its emitter, long-distance n-substrate as its base, and the p-well base of BJT $Q4$ in SCR2 device as its collector. If SCR1 and SCR2 devices are separated by the metal bonding pad in layout, $Q5$ transistor will have a very small beta gain due to its long-distance base width. The beta gain of vertical $Q4$ transistor is also dependent on its base width which is the difference between the depths of p-well and $N+$ diffusion in CMOS technology. In submicron CMOS technologies, the beta gain of parasitic vertical BJT is ordinarily as high as $100 \sim 200$. With such a high beta gain in vertical BJT $Q4$, VDD-to-VSS latchup may occur if resistances $R\text{sub}1$ and $Rw4$ are large enough.

In order to avoid VDD-to-VSS latchup, the base-emitter shorting method [32], [33] is adopted to reduce the shunt resistances $R\text{sub}1$ and $Rw4$. In Fig. 2, the base-emitter shorting effect is presented by the dashed lines shunting across resistances $R\text{sub}1$ and $Rw4$. If $R\text{sub}1$ ($Rw4$) is small enough, the base-emitter voltage of BJT $Q5$ ($Q4$) will be hardly triggered above its turn-on voltage as a transient current in the n-substrate (p-well). The smaller $R\text{sub}1$ and $Rw4$ lead to higher holding voltage of VDD-to-VSS latchup path [32]. $R\text{sub}1$ can be significantly reduced by putting an $N+$ diffusion with n-substrate bias of 5 V close to the p-well emitter of BJT $Q5$. Similarly, $Rw4$ can be reduced by putting a $P+$ diffusion with p-well bias of 0 V close to the $N+$ diffusion emitter of BJT $Q4$. With base-emitter shorting layouts in BJT's $Q4$ and $Q5$ as shown in the cross-sectional view of Fig. 1(a), the holding voltage of VDD-to-VSS latchup can be increased to above 5 V. Thus, this proposed CSCR ESD protection circuit can be free of VDD-to-VSS latchup.

III. Layout of the CSCR ESD Protection Circuit

A. Interdigitated Layout Style of Complementary SCR Structures

Like the layout style of a CMOS output buffer, interdigitated finger-type layout style is used to implement this CSCR ESD protection circuit. The interdigitated finger-type layout can offer more ESD current discharging paths than that of parallel strip-line style to avoid current crowding effect in the anode areas of lateral SCR1 and SCR2 devices as well as to avoid electromigration in metal lines and contacts. A demonstrated layout is shown in Fig. 3 with the corresponding cross-sectional views shown in Fig. 4(a) and (b). In Fig. 3, there are four metal fingers from input pad to the left-hand side to form lateral SCR1 and $D1$ devices, whereas there are two metal fingers from input pad to the right-hand side to form lateral SCR2 and $D2$ devices.

In Fig. 4(a), the cathode of SCR1 device is the $N+$ diffusion connected to input pad in a VSS-biased p-well which is surrounded by the adjacent VDD-connected p-well anode of SCR1 device. The diode $D1$ is formed by a $P+$ diffusion connected to VSS in the center of the p-well where the cathode of SCR1 device is in the same p-well. An $N+$ diffusion in n-substrate closed to the p-well anode of SCR1 device is made to surround whole SCR1 device. This $N+$ diffusion is also connected to VDD to offer n-substrate bias.

In Fig. 4(b), the anode of SCR2 device is formed by the $P+$ diffusion in a p-well which is surrounded by its cathode of an $N+$ diffusion connected to VSS in the adjacent VSS-biased p-well. The $P+$ diffusion closed to the $N+$ diffusion cathode of SCR2 device in the adjacent p-well is made to surround whole SCR2 device. This $P+$ diffusion is also connected to VSS to offer p-well bias. An $N+$ diffusion connected to VDD in n-substrate, which is placed in the outside of SCR2 device and surrounds SCR2 device, offers the substrate bias and forms the cathode of diode $D2$. This $N+$ diffusion also works as

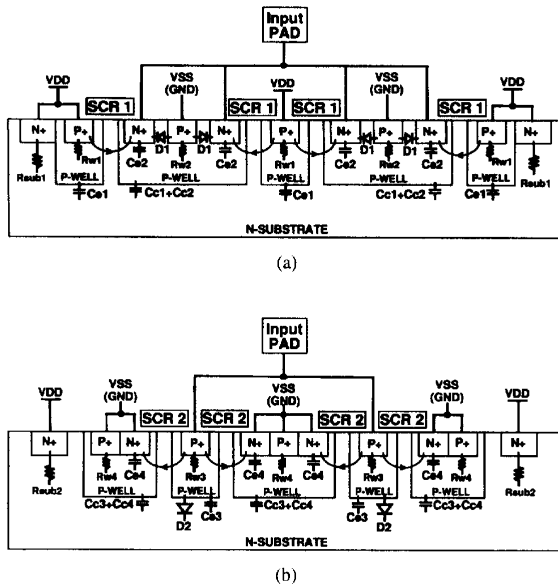
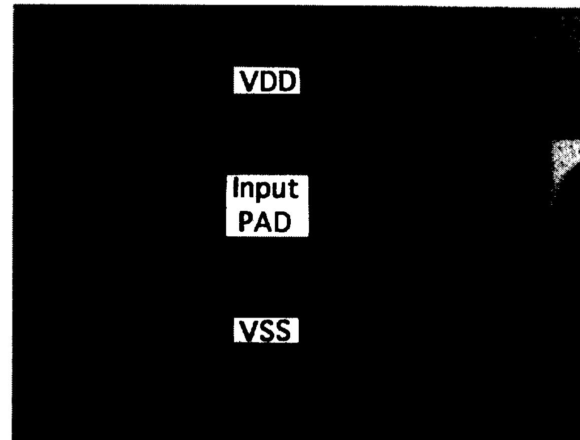


Fig. 4. The corresponding cross-sectional view of (a) the lateral SCR1 device and diode $D1$; (b) the lateral SCR2 device and diode $D2$, in the layout of Fig. 3.



SCR1 and D1 SCR2 and D2

Fig. 5. A microphotograph of the fabricated CSCR ESD protection circuit.

a guard ring to prevent VDD-to-VSS latchup. The anode of diode $D2$ is the same p-well anode of SCR2 device.

The parasitic VDD-to-VSS latchup path in this interdigitated finger-type layout is from the anode of SCR1 device through long-distance n-substrate under input pad to the cathode of SCR2 device. By means of base-emitter shorting layout on resistances $R\text{sub}1$ and $Rw4$, which are the VDD-connected $N+$ diffusion close to and surrounding the p-well anode of SCR1 device as well as the VSS-connected $P+$ diffusion close to and surrounding the $N+$ diffusion cathode of SCR2 device in Figs. 3 and 4, the VDD-to-VSS latchup path is repeatedly broken and guarded. The holding voltage of VDD-to-VSS latchup in this layout is expected to be above 5 V.

B. P-Well to P-Well Spacing

Due to base-emitter shorting effect in the VDD-to-VSS latchup path, the resistances of $R\text{sub}1$ and $Rw4$ are reduced significantly. Reducing the resistances of $R\text{sub}1$ and $Rw4$ also reduces the latching capability of lateral SCR1 and SCR2 devices in the ESD protection circuit. The junction capacitances in lateral SCR1 and SCR2 devices also provide transient currents to trigger on the lateral SCR devices during ESD transitions [13], [14]. But the base-emitter shorting technique on $R\text{sub}1$ ($Rw4$) also degrades the transient triggering effect of $Ce1$ ($Ce4$) capacitance in SCR1 (SCR2) device during ESD transitions. To increase the latching capability of SCR1 and SCR2 devices in the CSCR ESD protection circuit, the p-well to p-well spacings of lateral BJT's $Q1$ and $Q3$ can be reasonably shortened to increase their beta gains. The shorter p-well to p-well spacing could also lead to punchthrough between two adjacent p-wells before the p-well n-substrate breakdown in SCR1 and SCR2 devices. Thus, the trigger voltage of lateral SCR1 and SCR2 devices can be more reduced.

To experimentally investigate the effect of p-well to p-well spacing on the lateral SCR1 and SCR2 devices, this spacing on pattern layout varies from 1.2 μm to 3.0 μm with a step of 0.1 or 0.2 μm in the test chip.

IV. Experimental Results

Using the interdigitated finger-type layout in Fig. 3, the CSCR ESD protection circuit with one set of different p-well to p-well spacings is fabricated by a 0.6-μm twin-well n-substrate CMOS SRAM technology with modified LDD structure [34]. The thickness of gate oxide in PMOS or NMOS devices is 150 Å. The spacing of $N+$ diffusion inside p-well to the p-well edge is 2.8 μm. The layout area of lateral SCR1 device with $D1$ diode is 108×44 μm^2. The layout area of SCR2 device with $D2$ diode is 108×76 μm^2 which includes a surrounding $N+$ diffusion as latchup guard ring with ring width of 10 μm. A microphotograph of fabricated CSCR ESD protection circuit with p-well to p-well spacing of 2.0 μm is shown in Fig. 5.

A. VDD-to-VSS Latchup Characteristics

With 10-μm $N+$ diffusion guard ring and the base-emitter shorting technique, the dc I-V characteristics of VDD-to-VSS latchup path in the fabricated CSCR ESD protection circuit is shown in Fig. 6 with p-well to p-well spacing of 1.6 μm. It is shown that the dc holding voltage is as high as 17.5 V, which is much greater than the 5-V VDD power supply. In the fabricated CSCR ESD protection circuits with different p-well to p-well spacings, the holding voltage of VDD-to-VSS latchup path is around $16 \sim 18$ V. Thus, the proposed CSCR ESD protection circuit has been experimentally verified to be free of VDD-to-VSS latchup. The dc holding current in Fig. 6 is 16.5 mA and the dc switching voltage (current) is 44.15 V (11.75 mA).

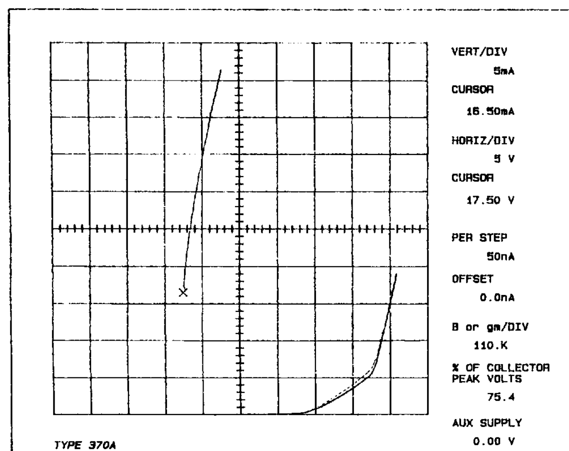


Fig. 6. The dc I-V characteristics of VDD-to-VSS latchup in the CSCR ESD protection circuit with p-well to p-well spacing of 1.6 μm.

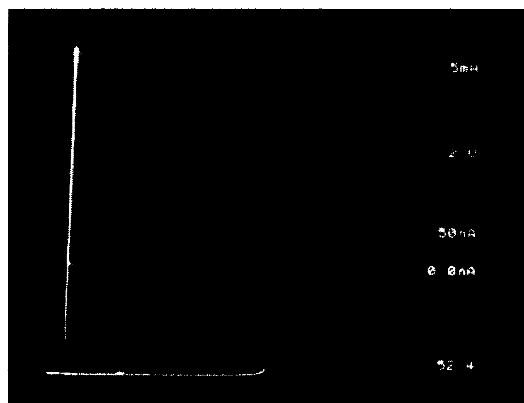
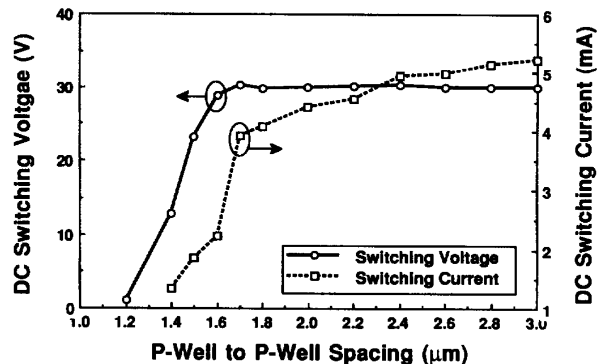
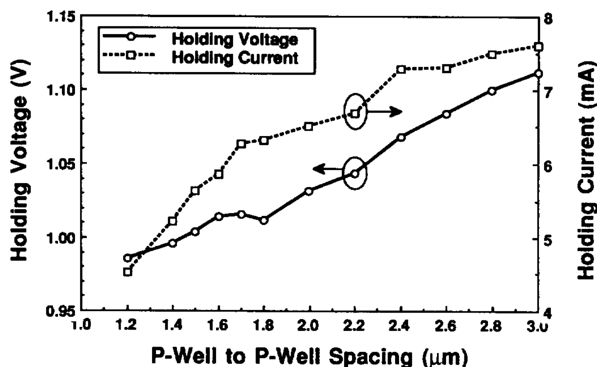


Fig. 7. The measured I-V characteristics of the lateral SCR1 device in the fabricated CSCR ESD protection circuit with p-well to p-well spacing of 1.4 μm, which is measured from VDD node to input pad with VSS node floating.



(a)



(b)

Fig. 8. The relations between (a) the dc switching voltage/current; (b) the holding voltage/current, and the p-well to p-well spacing in lateral SCR1 device.

B. Turn-on Characteristics of Complementary SCR Structures

The dc I-V characteristics of fabricated lateral SCR1 device with its p-well to p-well spacing of 1.4 μm is shown in Fig. 7 with turn-on resistance of 1.7 Ω, which is measured from VDD node to input pad with VSS node floating. The dc switching voltage (current) and holding voltage (current) are 12.92 V (1.34 mA) and 0.996 V (5.22 mA), respectively. The relation between the dc switching voltage (current) and the p-well to p-well spacing in lateral SCR1 device is shown in Fig. 8(a). The relation between the holding voltage (current) and the p-well to p-well spacing is shown in Fig. 8(b). It is shown that the dc switching voltage keeps around 30 V due to p-well/n-substrate junction breakdown when the p-well to p-well spacing is greater than 1.6 μm. But, the dc switching voltage nearly linearly decreases as the p-well to p-well spacing is less than 1.6 μm. The critical p-well to p-well spacing in this 0.6-μm CMOS technology to cause punchthrough is 1.6 μm. The dc switching voltage is lowered to 1.116 V when the spacing is only 1.2 μm, which is too low for the application in 5-V CMOS circuits. In Fig. 8(b), the holding voltage is around 0.986 V to 1.112 V with the spacing from 1.2 μm to 3.0 μm. With such low holding voltage, the ESD voltage at input pad can be clamped to a very low voltage level without damaging internal circuits. The turn-on resistance of lateral SCR1 device is around 1.6 to 2.0 Ω for the p-well to p-well spacing from 1.2 to 3.0 μm. With such low turn-on resistance in high-current range, the CSCR ESD protection circuit can provide very efficient discharging path to bypass ESD stresses. With the same structure as lateral SCR1 device, the turn-on characteristics of lateral SCR2 device are similar to those of SCR1 device.

The junction capacitances in lateral SCR device can provide transient currents to turn on itself during ESD transitions. Thus, the ESD-trigger voltage of lateral SCR device is lower than its dc switching voltage due to transient effect in device capacitance [14]. To investigate the ESD-trigger voltage of lateral SCR device with different p-well to p-well spacings, a pulse-type voltage waveform with 5-nS rise time and 20-μS pulse width generated by a HP8116A pulse generator is applied to the anode of lateral SCR1 device with its cathode grounded. The results are shown in Fig. 9. It is shown that the pulse-type trigger voltage of lateral SCR device is about 9.02 V when the spacing is 1.4 μm, and the pulse-type trigger

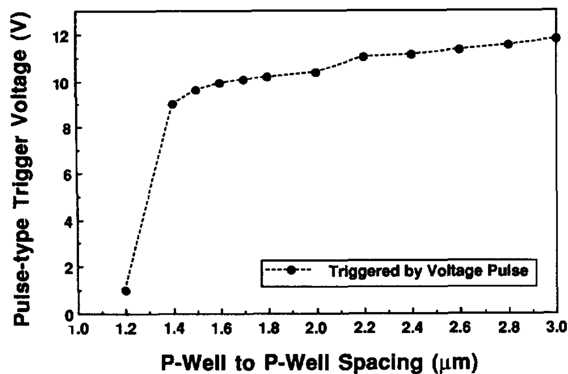


Fig. 9. The relations between the pulse-type trigger voltage of lateral SCR device and the p-well to p-well spacing.

voltage slightly increases to about 11.78 V when the p-well to p-well spacing increases to 3.0 μm. This implies an important design guideline that the p-well to p-well spacing should be chosen so that the SCR devices are triggered on by the pulse-type voltage triggering rather than by the breakdown or punchthrough between the two p-wells. This can guarantee an excellent reliability of the proposed CSCR ESD protection circuits. With a low pulse-type trigger voltage, the lateral SCR device can be quickly turned on to bypass ESD current before ESD damaging internal circuits. Although the base-emitter shorting technique on resistors Rsub1 and $Rw4$ used to avoid VDD-to-VSS latchup also degrades the transient currents of $Ce1$ and $Ce4$ in lateral SCR1 and SCR2 devices, the pulse-type trigger voltage of lateral SCR1 and SCR2 devices can still be lowered from the dc switching voltage about 30 V to only around 10 $\sim$ 11 V as shown in Figs. 8(a) and 9. Thus, with the interdigitated finger-type layout style and the base-emitter shorting method, the CSCR ESD protection circuit can offer effective low ESD-trigger voltage and also be free of VDD-to-VSS latchup.

Moreover, to show that the SCR1 and SCR2 devices are not triggered on in the high-speed CMOS operations, a voltage pulse string with the pulse width varying from 10 nS to 5 mS, high level voltage above 5.6 V, low level voltage below −0.6 V, and the rise time around 200 pS generated by a HP8131A 500 MHz pulse generator is applied to the input pad of fabricated ESD protection circuit with 5-V VDD and grounded VSS. The voltage pulse string does not trigger on the lateral SCR1 and SCR2 devices in the fabricated ESD protection circuit, because the voltage level on the pad with overshooting/undershooting input signals is clamped to −0.6 $\sim$ + 5.6 V by diodes $D1$ and $D2$. Thus the lateral SCR1 and SCR2 devices are not triggered on by high-speed operating input signals with overshooting/undershooting conditions.

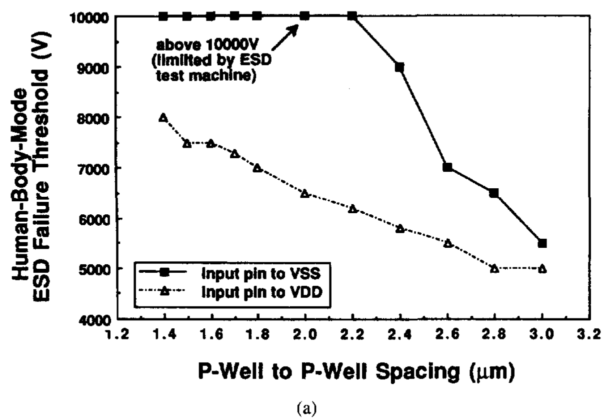
C. ESD Testing Results

The fabricated complementary-SCR ESD protection circuit with different p-well to p-well spacings are tested by both Human-Body-Mode (HBM) ESD and Machine-Mode (MM) ESD. The ESD voltage pulses have positive and negative polarities with respect to VDD and VSS nodes. For each p-well to p-well spacing, there are at least five samples of fabricated CSCR ESD protection circuits to be tested under each ESD-stress mode of both HBM and MM ESD. The minimum ESD failure voltage of the tested five samples is adopted as the ESD failure threshold of ESD protection circuit. The HBM and MM ESD testing results are shown in Fig. 10(a) and (b), respectively. The ESD failure criterion is defined as the initial voltage of 1-μA current leakage shifting 40% after ESD stress. In Fig. 10(a), it is seen that the HBM ESD failure threshold from input pin to VSS can be above ± 10 KV if the p-well to p-well spacing below 1.8 μm, whereas that from input pin to VDD is above ± 7000 V. In Fig. 10(b), it is shown that the MM ESD failure threshold from input pin to VSS node can be above ±1 KV if the p-well to p-well spacing below 1.8 μm, whereas that from input pin to VDD is above ±400 V. When the p-well to p-well spacing of lateral SCR device increases from 1.8 to 3.0 μm, both HBM and MM ESD failure thresholds in Figs. 10(a) and 10(b) roughly decrease to about ± 5000 V and ± 250 V, respectively. The shorter p-well to p-well spacing in lateral SCR devices provides higher beta gains of lateral p-n-p BJT's $Q1$ and $Q3$, which causes stronger positive-feedback regeneration and leads to quicker turn-on in the lateral SCR devices to bypass the sudden ESD stresses. Thus, the CSCR ESD protection circuit with shorter p-well to p-well spacing provides submicron CMOS IC's with higher ESD protection capability.

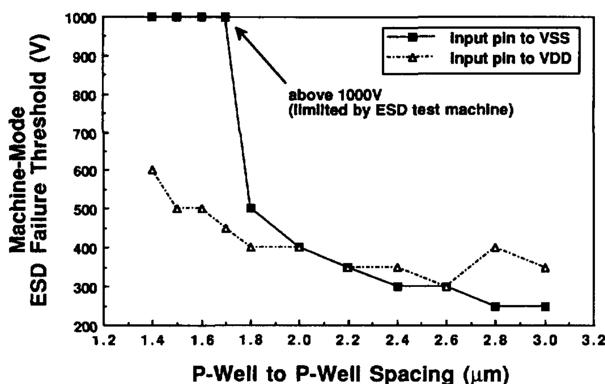
As seen in Figs. 10(a) and (b), the ESD failure threshold from input pin to VSS is almost higher than that from input pin to VDD under the same p-well to p-well spacing. The reason why the lateral SCR1 and SCR2 devices have the same p-well to p-well spacing but different ESD failure thresholds are due to the layout of cathode in SCR1 device. As seen in Fig. 3, the SCR2 device is fully surrounded by its cathode connected to VSS node, but the SCR1 device is partially surrounded by its anode connected to VDD node. The cathode of lateral SCR1 device is also the cathode of diode $D1$ as shown in Fig. 4(a). To improve the ESD failure threshold from input pin to VDD, the cathode of lateral SCR1 device should be fully surrounded by its VDD-connected p-well anode whereas the VSS-connected $P+$ diffusion anode of diode $D1$ should be placed in the center of the p-well and surrounded by the $N+$ diffusion cathode of SCR1 device.

V. Conclusion

A robust ESD protection circuit with complementary SCR structures and junction diodes has been designed and fabricated by a 0.6-μm CMOS SRAM technology. The VDD-to-VSS latchup issue in the ESD protection circuit has been overcome by means of base-emitter shorting method. The experimental results show that the dc holding voltage of VDD-to-VSS latchup can be increased up to 17.5 V. The p-well to p-well spacing in the lateral SCR devices is reduced to lower the pulse-type ESD trigger voltage and to enhance turn-on speed of positive-feedback regenerative process in the lateral SCR devices. ESD testing results show that an input pad with the CSCR ESD protection circuit under p-well to p-well spacing below 1.8 μm can sustain above ±7000 V human-



(a)



(b)

Fig. 10. The dependence of (a) the human-body-mode; (b) the machine-mode, ESD failure threshold of the fabricated CSCR ESD protection circuit on the p-well to p-well spacing in lateral SCR devices.

body-mode and ±400 V machine-mode ESD stresses within a small layout size. In normal CMOS operating conditions with 5-V VDD power supply, diodes $D1$ and $D2$ in the CSCR ESD protection circuit also offer voltage clamping effect to limit the input voltage level between -0.6 V $\sim +5.6$ V.

This proposed complementary-SCR ESD protection circuit can provide submicron CMOS IC's with direct and effective ESD discharging paths from the input pad to both VDD and VSS power lines. Thus, the unexpected ESD damages on the internal circuits beyond ESD protection circuits can be avoided.

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Ming-Dou Ker was born in Taiwan, Republic of China, in 1963. He received the B.S. degree from the Department of Electronics Engineering, and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1986, 1988, and 1993, respectively.

From 1986 to 1988, he studied the timing models of CMOS integrated circuits, and from 1989 to 1993, he engaged in the development of CMOS on-chip ESD protection circuits and CMOS latchup analysis, with support from the United Microelectronics Corporation (UMC), Taiwan. From 1993 to 1994 he was a postdoctoral researcher in Integrated Circuits and Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. In 1994, he joined the VLSI Design Department of *Computer & Communication Research Laboratories* (CCL), Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, as a circuit design engineer. Since then he was engaged in the development of mixed-mode integrated circuits in submicron CMOS technology. His research interests include reliability of CMOS integrated circuits, mixed-mode integrated circuits, and communication integrated circuits design.

Dr. Ker is a member of ESD Association.

Chung-Yu Wu was born in Chiayi, Taiwan, Republic of China, in 1950. He received the B.S. degree from the Department of Electrophysics, and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, in 1972, 1976, and 1980, respectively.

From 1975 to 1976, he studied ferroelectric films on silicon and their device applications, and from 1976 to 1979 he engaged in the development of integrated differential negative resistance devices and their circuit applications, with support from the National Electronics Mass Plan (Semiconductor Devices and Integrated Circuit Technologies) of the National Science Council. From 1980 to 1984, he was an Associate Professor at the Institute of Electronics, National Chiao-Tung University. From 1984 to 1986, he was an Associate Professor in the Department of Electrical Engineering, Portland State University, Portland, OR. Presently, he is a professor in the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University. He has published more than 60 journal papers and 80 conference papers on several topics, including digital integrated circuits, analog integrated circuits, computer-aided design, ESD protection circuits, special semiconductor devices, and process technologies. He has 9 patents, including 5 U.S. patents. His current research interests focus on low voltage mixed-mode integrated circuit design, hardware implementation of visual and auditory neural systems, and RF integrated circuit design.

Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi.