Investigation of Programmed Charge Lateral Spread in a Two-bit Storage Nitride Flash Memory Cell by Using a Charge Pumping Technique

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Abstract

The lateral distribution of programmed charge in a hot electron program/hot hole erase nitride storage flash cell is investigated by using a charge pumping technique. Our study shows that the secondly programmed bit has a wider trapped charge distribution than the first programmed bit. In addition, we find programmed charge spreads further into the channel with program/erase cycle number.

Introduction

Nitride storage flash cells have received much interest recently due to their smaller bit size, simpler fabrication process and absence of drain induced turn-on. By taking advantage of localized charge trapping in nitride above the source and the drain junctions (Fig. 1), two-bit storage of a nitride cell can be realized by hot electron program and band-to-band hot hole erase with a reverse read scheme [1]. In two-bit storage, the control of programmed charge lateral distribution is particularly important since stored electrons at the first bit will affect the threshold voltage of the second bit in reverse read and vice versa. This phenomenon is referred to as the second bit effect. Furthermore, the lateral spread of programmed charge will cause a mismatch between trapped electron distribution and injected hole distribution in erase, thus resulting in degradation of erase capability or erase speed. In this work, we will use a charge pumping technique to explore the programmed charge profile of each bit. The P/E cycling stress effect on the distribution of programmed charge is also investigated.

Charge Pumping Measurement

The samples have a gate length of 0.5μm and a gate width of 1.0μm. The voltage waveforms in charge pumping (CP) measurement are illustrated in Fig. 1. The gate pulse has a fixed high level (V_{gh}=6V) and a variable low level (V_{gl}). To profile the lateral extent of programmed charge in the drain side (or the source side), V_d (or V_s) is adjusted to modulate the drain (or source) depletion width while V_s (or V_d) is floating and the charge pumping current (I_{cp}) is measured at the substrate. The drain pulse is 180° phase-shifted with respect to V_g that the drain bias is applied only during the trapped electron emission cycle. The frequency in CP measurement is 2.5MHz.

Results and Discussion

(a) first bit Icp

Fig. 2 shows I_{cp} versus V_{gl} in a virgin cell, after programming only and after one P/E cycle. Only the first bit (drain side) is P/E cycled. The threshold voltage window (ΔV_t) is 2V. Here, V_t is defined as the gate voltage when the drain current is 1μA at a reverse read voltage of 1.6V. The observed I_{cp} bump in program state is caused by negative nitride charge trapping. Fig. 3 shows that the I_{cp} bump increases with a V_t window due to more trapped electrons. In Fig. 4, the dependence of the program-state I_{cp} bump on V_d in CP measurement is shown. At a sufficiently large V_d, interface traps underneath programmed charge are "masked" by the drain depletion region. Thus, the program-state I_{cp} bump is completely suppressed. In contrast, when V_s is applied in CP measurement, the I_{cp} bump is not affected at all (Fig. 5). This indicates that programmed charge is highly localized near the drain edge.

(b) two-bit storage Icp

The I_{cp} of four two-bit storage states, "11", "10", "01" and "00", is shown in Fig. 6. "00" denotes both bits in program state. Fig. 7 compares the I_{cp} of the first programmed bit and the secondly programmed bit. The 2nd programmed bit I_{cp} is measured with the first bit erased. Notably, a cross-over in Fig. 7 is observed. This cross-over suggests that the secondly programmed bit exhibits a wider charge distribution but a smaller peak density. By using a charge spatial profiling technique similar to [2], the nitride charge spatial distribution can be obtained as follows;

$$Q_N(x) = \frac{C_{ONO}}{q}(V_{gl} - V_{ti}), \quad x = \frac{I_{cp}(V_{gl})}{I_{cp,max}} L_{ch}$$

where $Q_N(x)$ is the nitride charge density, L_{ch} is the channel length and V_{ti} is the threshold voltage of a fresh device. x=0 is at the source or the drain edge. The extracted charge profile of the first programmed bit and the secondly programmed bit is shown in Fig. 8. The distribution of the secondly programmed bit (source side) is broader because a large channel field exists in the drain side during 2nd bit programming (Fig. 9). Such a large drain field results from stored electrons of the first programmed bit and will cause channel electrons to inject into the nitride earlier. It should be remarked that the above equation is derived from a 1D V_t model. For a narrow charge distribution by hot electron programming, it only serves as a first-order approximation. Accurate profiling of programmed charge distribution requires a 2D device simulation.

The programmed charge lateral extent can be also probed by varying V_d (or V_s) in CP measurement. The decrease of the program-state I_{cp} bump with V_d (or V_s) is shown in Fig. 10. The 2nd programmed bit needs a larger junction bias to "mask" the programmed charge. The same conclusion that the second bit has a broader charge distribution is reached.

(c) P/E cycling stress

The P/E cycling stress effect on programmed charge distribution is examined in Fig. 11. The V_t window keeps the same during cycling. In order to eliminate interface trap creation effect in cycling, the I_{cp} bump is normalized to its value at V_d=0V. As cycle number increases, the bottom oxide damaged region becomes broader and so does the hot electron injection region. Thus, a larger V_d in CP measurement is necessary to screen the programmed charge. In other words, the second bit effect is worsened after P/E cycling.

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[1]B. Eitan et al, IEEE EDL, p.543, 2000
[2]C. Chen et al, IEEE TED, p.512, 1998

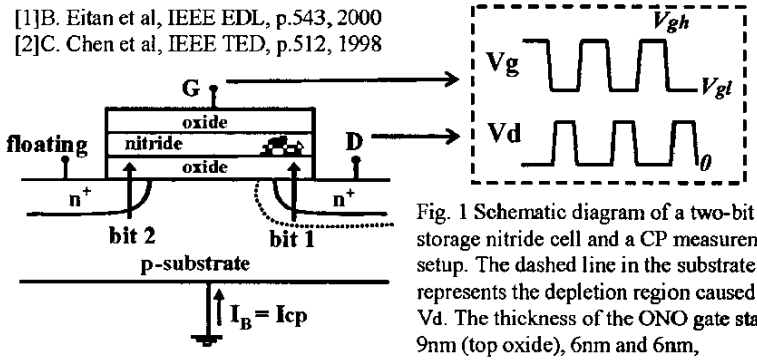

Fig. 1 Schematic diagram of a two-bit storage nitride cell and a CP measurement setup. The dashed line in the substrate represents the depletion region caused by Vd. The thickness of the ONO gate stack is 9nm (top oxide), 6nm and 6nm, respectively.

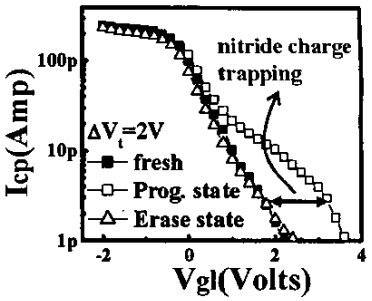

Fig. 2 Icp versus Vgl in a fresh cell, in program state and in erase state, respectively. The V_t window (ΔV_t) is 2V. Vd in CP measurement is 0V.

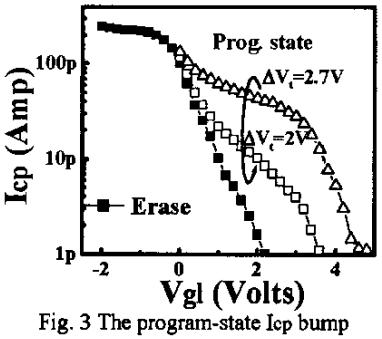

Fig. 3 The program-state Icp bump increases with V_t window due to more injected charges.

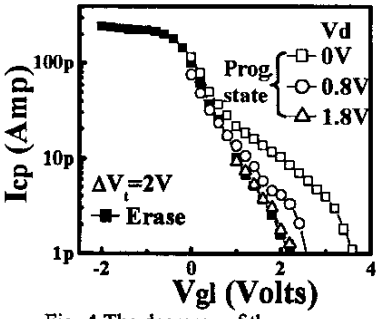

Fig. 4 The decrease of the program state Icp bump with Vd in CP measurement. The V_t window is 2V.

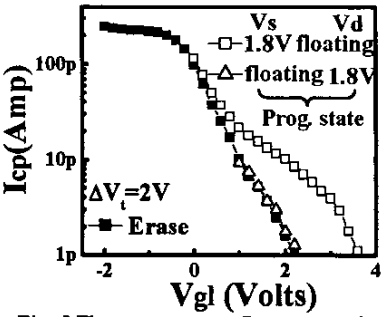

Fig. 5 The program state Icp measured at Vd=1.8V & Vs floating and at Vs=1.8V and Vd floating.

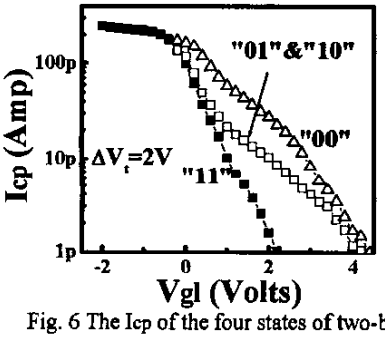

Fig. 6 The Icp of the four states of two-bit storage. "11" represents both bits in erase-state and "10" represents one bit in erase-state and one bit in program-state.

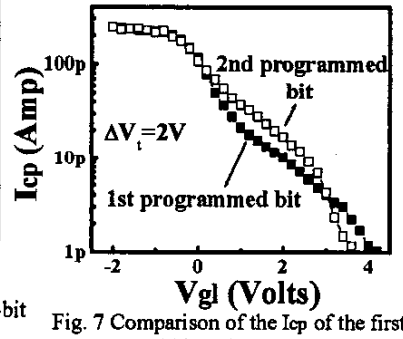

Fig. 7 Comparison of the Icp of the first programmed bit and the secondly programmed bit. The 2nd bit Icp is measured with the first bit erased.

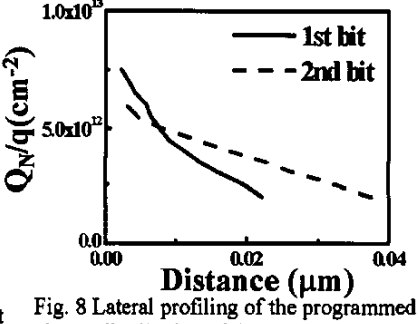

Fig. 8 Lateral profiling of the programmed charge distribution of the first programmed bit and the secondly programmed bit. An uniform interface trap distribution along the channel is assumed. Icp,max is 195pA.

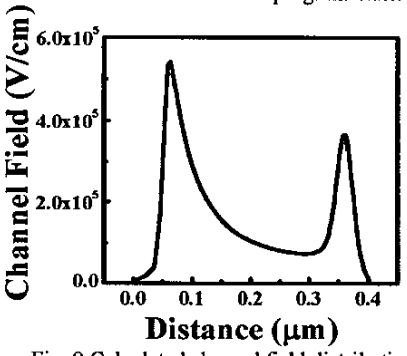

Fig. 9 Calculated channel field distribution in 2nd bit programming from 2D device simulation. x=0 is at the n^+ source edge and x=0.4 is at the n^+ drain edge. Vs=6.5V and Vg=11V in 2nd bit programming.

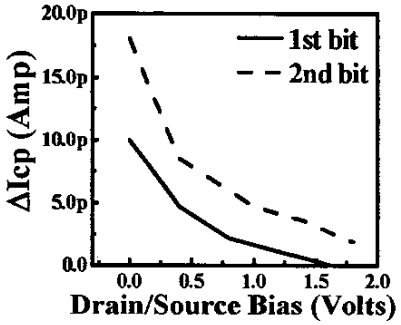

Fig. 10 The difference in Icp between program state and erase state as a function of drain bias for the 1st bit and source bias for the 2nd bit. ΔIcp is obtained from Fig. 7 at Vgl=1.6V. .

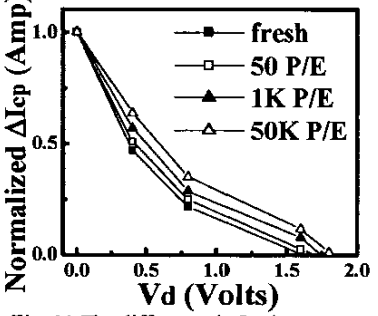

Fig. 11 The difference in Icp between program state and erase state as a function of Vd in CP measurement at various P/E cycle numbers. ΔIcp is measured at Vgl= 1.6V and is normalized to its value at Vd=0V to take into account interface trap creation in cycling.