Different Approaches for Reliability Enhancement of P-Channel Flash Memory

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Abstract- In this paper, we will demonstrate two different strategies for designing p-channel flash memories, for achieving better reliability, in particular data retention and drain-disturb. The first one is by using a gate-engineering approach and the other one is using a newly developed substrate bias enhanced Avalanche Hot Electron (AHE) injection programming scheme. For the former, a p-doped floating gate on both p-channel flash cells can be achieved with superior data retention characteristics as well as a 3-order improvement of the drain disturb. For the latter, it exhibits much higher speed and much lower voltage for programming, and very good drain disturb characteristics.

Introduction

In the past, n-channel flash cells [1] were widely used in the design of flash memory products. However, the requirement of high voltage operation for channel-hot-electron (CHE) programming results in a large power consumption. In order to improve it, the p-channel flash cell has been suggested for low voltage and low power applications [1-2]. A more matured p-channel cell using band-to-band tunneling induced hot electron injection (BBHE) has later been proposed [3]. However, in p-channel flash memory cells, there is a serious problem with the drain disturb [1] which impedes its practical applications for mass production purpose.

In this paper, reliability enhancement for p-channel flash cells has been demonstrated. Two different approaches, i.e., the p-type floating-gate (FG) and a low voltage programming scheme [4], will be demonstrated and the data retention and drain disturb will be the major focus.

Results and Discussion

A. The Gate Engineering Approach

In the past several years, there are quite few studies on the p-channel cells [1-4]. We found in our previous work [5] that the usage of p-type floating gate (p-FG) in an n-channel flash cell is feasible for the high speed programming/erasing as well as better endurance. As a result, special attention to a p-channel cell with p-doped FG flash memory cell has attracted much more interest. Fig. 1 shows the ETOX cell with various types of dopants (Table 1) for the floating gate. The difference between n-doped and p-doped FG are that: (1) the tunnel oxide field in p-FG is larger than that of n-FG, and (2) the ONO electric field in p-FG is smaller than that in n-FG, under the same applied field for two types of cells. As a consequence, the p-doped FG cell exhibits much faster speed (Fig. 2) and much better data retention(Fig. 3). The smaller charge loss in p-FG is attributed to a less oxide damage generated as a result of smaller electric field across the ONO layer and much less gate disturb. One most exciting result is shown in Fig. 4. The p-channel flash cell has an inherent disadvantage of poor drain-disturb [1] since its introduction in [1-2], while the use of p-type FG can solve the problem, as shown in Fig. 4, which shows a 3-order of drain-disturb improvement. The reason of this improvement is revealed in Fig. 5, which shows the gate currents for different floating-gate. Drain disturb is determined by BBHE tunneling when the cell is in programmed state, and by CHH(Channel Hot Hole) tunneling when the cell is in erased state. Obviously, the n-FG has larger CHH currents than the p-type ones. This can explain why the p-type FG cell has better drain disturb characteristics. Again, for a 10-year lifetime, the p-FG cell has a larger operating gate bias, which means a longer lifetime as shown in Fig. 6.

In summary, the p-FG cell has faster programming speed, but a slower erasing speed. However, the p-type floating-gate cell has much better reliabilities than those of n-type cell, in particular it features less gate disturb, larger lifetime tolerance voltage, three-order improvement in drain disturb, and better data retention characteristics etc. (Table 2). The p-type floating-gate flash cell also has much lower electric field in the ONO dielectric layer by comparing with that of conventional n-type floating-gate during programming. Therefore, fewer electrons will be injected into the ONO dielectric. This is the reason why p-type FG has much better data retention characteristics than that of n-type FG cell.

B. The Operating Scheme Approach

In addition to the gate-engineering approach, operating schemes can also be developed for reliability enhancement beyond the low voltage, low power, and/or high speed performance. The mechanism of the new AHE scheme is given in Fig. 7. First, drain/substrate junction is biased at avalanche breakdown region, from which electrons and holes are generated. The hot electrons will surmount the barrier and contribute to the gate current labeled 1, while holes are attracted toward the deep depletion region and cause impact ionization, which then give rise to gate current labeled 2 via a high field maintained between the gate and substrate. Fig. 8 shows the gate currents at various drain biases, in which FN, BBHE, or AHE dominates at their respective regions. In general, we need a much larger gate bias for BBHE to generate the same level of I_G by comparing to AHE scheme. In other words, a much higher gate voltage in BBHE will induce larger reliability problems. Furthermore, Fig. 9 shows the programming speed comparison between AHE and BBHE schemes. AHE scheme is always faster than BBHE scheme for a substrate bias ranged from 0V to 3V. Also, we see from Fig. 10 that AHE needs a smaller gate voltage for attaining a 10-year lifetime, which is suitable for low voltage operation and more reliable.

For the evaluation of drain disturb, the use of AHE scheme, drain disturb can also be greatly reduced for p-channel cells as given in Fig. 11, in which a 3-order improvement of the drain disturb can be achieved. The physical reason for this drain disturb improvement is that smaller drain bias is needed in the AHE scheme such that the hole injection, component(2), can be reduced.

In summary, we have demonstrated two successful methods to improve the reliability of p-channel flash cells. Results show that the p-FG approach and the AHE scheme offer many advantages. These include a faster programming speed, lower voltage, lower power, better lifetime, and better data retention. In particular, the drain disturb can be largely reduced by either using the p-FG or a low voltage scheme in a p-channel flash cell. This made p-channel possible for its advantages over n-channel flash cells.

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[3] T. Ohnakado et al., in *IEDM Tech. Digest*, p. 279, 1995.
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FG Split	U	P-	P+	N+
T_{ox}(Å)	90			
T_{max}(Å)	T.O/Si_3N_4/B.O=65/90/55= 165A(EOT)			
Floating Gate Doping	undoped	BF2 20Kev 1E13	BF2 20Kev 5E13	In-situ

Table 1 The split conditions of floating gate for both p-channel cells used in this study.

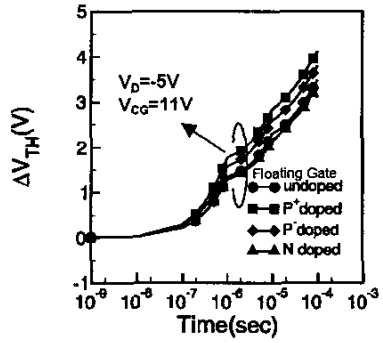

Fig. 2 Comparison of the programming characteristics for flash cells with different dopant types in the floating gate.

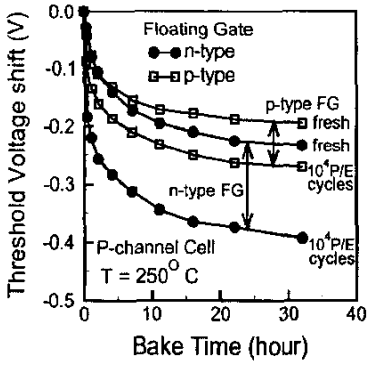

Fig. 3 Charge loss characteristics of p-channel cells with n- and p-type FG before and after 10^4 P/E cycles at 250°C.

Characteristics \ FG type	N-type	P-type
Program Speed	Slower	Faster
Erase Speed	Faster	Slower
Endurance	Similar	Similar
Gate Disturb	Worse	Better
Read Lifetime Voltage	Smaller	Larger
Drain Disturb	Worse	Better
Data Retention	Worse	Better

Table 2 The comparison of performance and reliability between p-FG and n-FG p-channel flash cells.

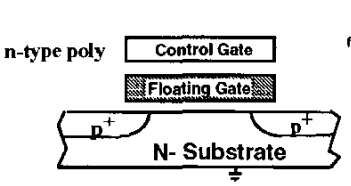

Fig. 1 The experimental p-doped floating gate flash cells with split conditions in Table 1. Control samples with n-doped floating gate were also made for comparison.

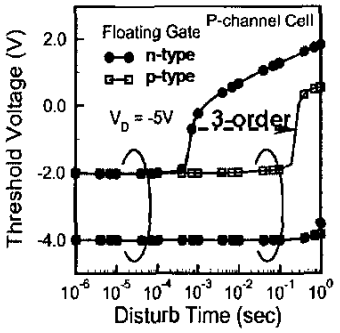

Fig. 4 Drain-disturb of p-channel cells under high oxide field. Note that drain-disturb has 3-order improvement by using p-type FG(square symbol).

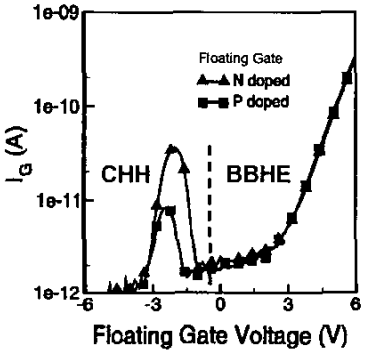

Fig. 5 The gate currents of p-channel flash cells with n- and p-type floating gate. The p-type FG cell has less gate current injection during CHH injection.

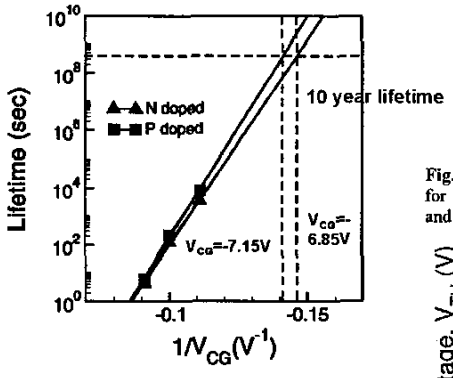

Fig. 6 Lifetime prediction of the operating gate bias for both n-type FG and p-type FG cells. Note that p-FG shows much larger operating gate bias.

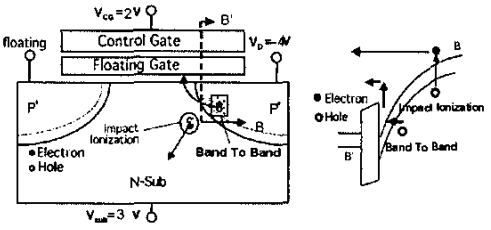

Fig. 7 The schematic diagram of the Avalanche Hot Electron (AHE) scheme in a p-channel flash cell.

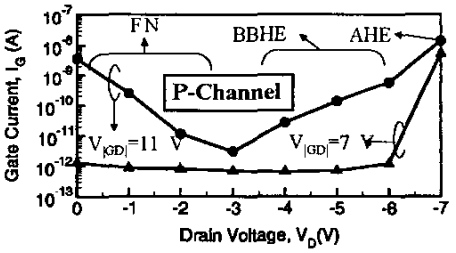

Fig. 8 Measured gate current as a function of drain bias at different gate voltages. The FN, BBHE, and AHE generated currents are shown in their respective regions of operation.

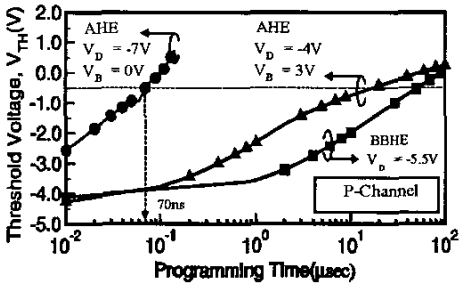

Fig. 9 The programming speed for AHE scheme at different substrate biases and the comparison with BBHE scheme

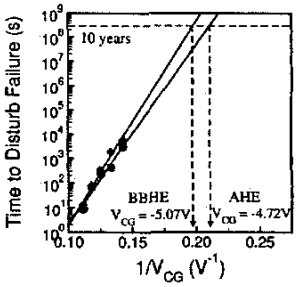

Fig. 10 The high oxide field gate-disturb characteristics for both n- and p-type floating-gate flash cells before and after 10^4 P/E cycles (N-channel cell).

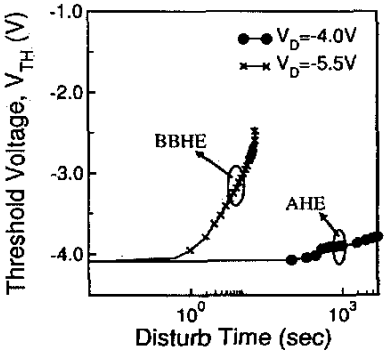

Fig. 11 Comparison of the drain-disturb characteristics between BBHE and AHE. Note that drain disturb is largely reduced in the AHE scheme. ➔