A Simple Transmission Line De-embedding Method for Accurate RF CMOS Noise Modeling

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***Abstract* —We propose a simple method to de-embed the transmission line and pads' parasitics from the measured RF noise of multi-finger MOSFETs with aggressive gate length scaling down to 80 nm and 65 nm respectively. Good agreement has been realized between measurement and simulation in terms of S-parameters and NF_{min} (minimum noise figure) for RF CMOS devices with various finger numbers by using this novel de-embedding method. The extracted NF_{min} after de-embedding matches well with the published noise correlation matrix method but is relatively simple without resort to complicated matrices calculation.**

Introduction

The aggressive CMOS device scaling has driven dramatic reduction of gate delay and remarkable increase of the unit-current-gain cut-off frequency (f_T) [1]-[2]. However, it turns out a difficult task to extract RF CMOS noise accurately while its scalability with device scaling is quite important for low noise RF circuit design. The challenges arise from the strong dependence of RF noise on parasitic and coupling effect associated with gate, substrate, interconnect, and pads, etc. [3]-[5] One of primary noise sources comes from gate resistance generated thermal noise and multi-finger layouts are generally used to reduce the gate resistance. In our study, excess noise was identified to be critically related to the lossy pad and transmission-line effects. The excess noise may dominate in sub-100nm CMOS devices. A noise correlation matrix method [6] was proposed to de-embed these effects but complicated matrices calculation is required. In this paper, we propose a simple method to de-embed pads' and transmission line's parasitic. We have established an equivalent circuit model to incorporate the lossy pad and transmission line effect. Good match with measured extrinsic characteristics like S-parameters and noise figure has been achieved by simulation for RF MOSFET with different finger numbers using this extrinsic equivalent circuit model. The intrinsic MOSFET model was obtained by subtracting all the parasitics from the extrinsic MOSFET. Our method can achieve not only agreement with the noise correlation matrix method [6] but also relatively simple without using complicated matrices calculation. In addition, our results suggest that the as-measured extrinsic minimum noise figures (NF_{min}) without de-embedding is dominated by the lossy pad and transmission line effect as evidenced from the particularly worse NF_{min} measured from smaller size MOSFETs with finger number as small as 6 (N_F=6). However, the de-embedded intrinsic NF_{min} do show a lower value of 1.0/0.9 dB at 10 GHz corresponding to N_F=6/72 for 65nm MOSEFT. This extraction method is simple and useful to achieve intrinsic noise model that's critically important to improve RF circuit simulation accuracy for low noise RF circuit design.

Experimental

To study the scaling effect, sub-100nm n-MOSFETs of gate lengths at 80 and 65 nm are used. Multi-finger structure is employed to reduce the gate resistance generated RF noise. The finger width is fixed at 4 μm and finger numbers of 6, 18, 36 and 72 are splits available for comparison. At first, I-V characterization was done to extract g_m that's a key parameter affecting f_T and RF noise. After that, S-parameters were measured by using HP8510C network analyzer up to 40 GHz. Open de-embedding was done on the measured two port S-parameters. The NF_{min} and associate gain were measured by ATN-NP5B system to 18 GHz that covers the important frequency band from handset to wireless LAN and future X-band communication. A thru line was proposed in the equivalent circuit to emulate the transmission line between RF probe pad and gate terminal and we modeled the thru line to de-embed its effect on RF noise. An intrinsic MOSFET model was obtained by subtracting the pad capacitance, the thru line series resistance and inductance from the original MOSFET characteristics. Then, the intrinsic transistor noise can be extracted by simulation to fit the intrinsic characteristics after the open pad and thru line de-embedding.

Results and Discussion

A. *Measured noise in 80nm and 65 nm MOSFETs with different finger numbers:*

Fig. 1 shows the measured NF_{min} for 65 nm and 80 nm MOSFETs with various finger numbers (N_F=6,18,36,72). It's demonstrated quite obviously that RF noise decreases with increasing N_F , that's part due to lower gate resistance (R_g) generated thermal noise. Fig.2 indicates R_g extracted from Z-parameters for 65 nm and 80 nm MOSEFTs and

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reveals the dramatic effect by increasing finger numbers. R_g can be reduced to below 3Ω for N_F=72. Regarding the much higher NF_{min} measured from smaller device with N_F=6, the increasing weighting factor played by the lossy pads is consider as another major cause. Fig.3(a) indicates the parasitic capacitances extracted from the GSG pads for open de-embedding and it's revealed that the lossy pads' parasitic capacitance is around 190fF, that's more than 5 times larger than the intrinsic gate capacitance of the smallest devices, around 35fF for 65 nm device with N_F=6 as shown in Fig.3(b). Fig.4 demonstrates f_T as high as 115 and 155 GHz for 80 nm and 65 nm devices with N_F=18, where f_{max} as high as 80 and 110 GHz are achieved simultaneously. These sub-100nm devices realize excellent RF performance in terms of f_T and f_{max} that's comparable with the best record reported for RF CMOS. However, the RF noise prior to de-embedding is abnormally high, particularly worse for smaller devices with N_F=6. To investigate the possible sources of the extra RF noise, an extensive analysis on the transistor layout has been done. We propose that the worse RF noise with scaling is due to the large pad parasitics and the transmission line may play some role in impedance matching. Our model suggests that the lossy pad parasitic must be de-embedded from the measured noise figure to achieve accurate NF_{min}.

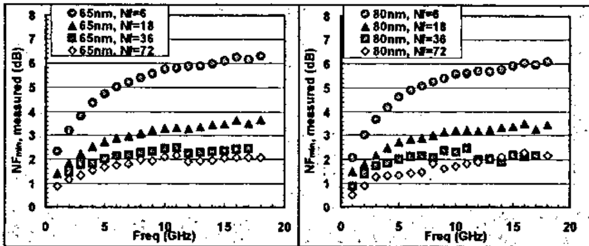


Fig. 1. The measured NF_{min} versus frequency for 65 nm and 80 nm n-MOSFETs with finger numbers of 6,18,36,72 (N_F=6,18,36,72)

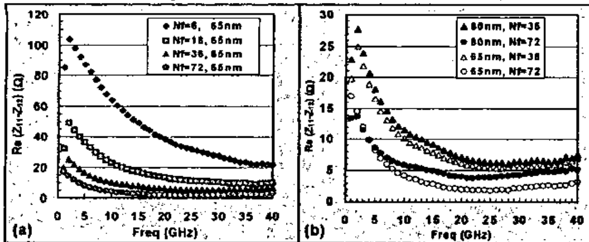


Fig. 2. The gate resistance R_g extracted from Z-parameters for 65nm and 80nm MOSFET with N_F= 6, 18, 36, 72 (a) 65 nm (b) comparison between 65nm and 80 nm MOSEFT with N_F= 36, 72

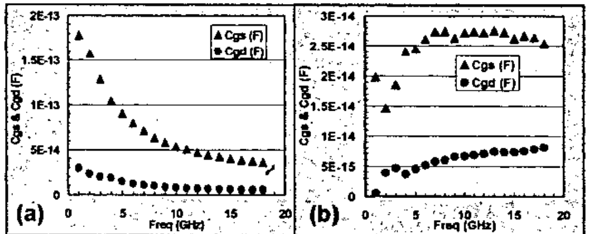


Fig. 3. The gate capacitances C_{gs}, C_{gd} extracted from Y-parameters for GSG pad and 65nm MOSFET with finger numbers of 6 (a) GSG pad (b) 65nm MOSEFT, N_F=6

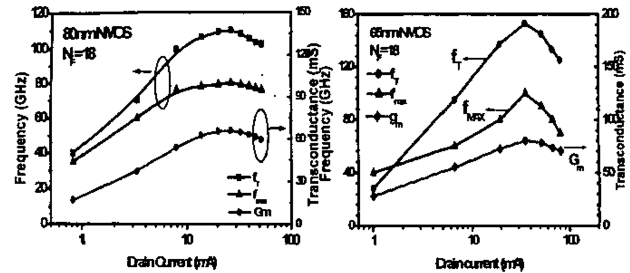


Fig. 4. The f_T, f_{max}, gm measured from 80nm and 65nm NMOSFETs with finger numbers of 18 (a) 80nm (b) 65nm MOSEFT, N_F=18, W=4μm

Fig.5 shows the equivalent circuit model of transmission line connected to gate electrode of MOSFET. The transmission line body is consisted of series resistor (R_{TML}) and inductor (L_{TML}). The shunt RC path to ground at two pads is used to simulate the substrate loss effect. An equivalent circuit model for sub-100 nm MOSFETs is shown in Fig.6, which includes the lossy pads, the gate transmission line, and the body of MOSFET. The MOSFET contains intrinsic part (modeled by BSIM3) and RLC parasitic at two ports as extrinsic part. Besides the gate resistance generally considered, pads' capacitive coupling to substrate is identified as one more important factor to worsen the original gate induced thermal noise. The transmission line (R_{TML}, L_{TML}) connected to gate is proposed in this study to account for the distributed gate network model. The R_g associated with intrinsic MOSFET represents the distributed gate and channel resistances. For devices with large finger number, e.g. N_F=72, R_g is effectively reduced and R_{TML} may play an important role in determining NF_{min}. Regarding ultra high frequency, e.g. up to 40 GHz in this study, inductive impedance ωL_{TML} becomes an important parasitic affecting the RF noise.

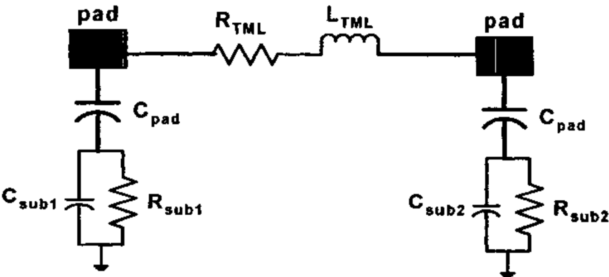


Fig. 5. The equivalent circuit model for transmission line connected to the gate of MOSFET. Note that the probe pad is de-embedded from an open measurement that is different from the shunt RC path to ground

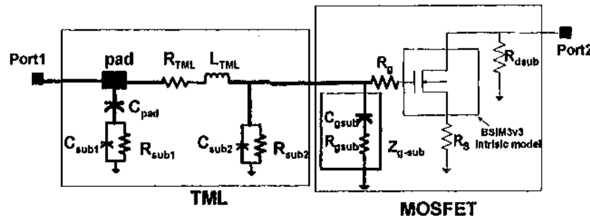
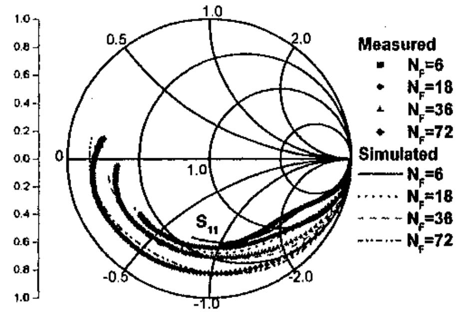


Fig. 6. The equivalent circuit model for RF MOSFET. Self-consistent solution among I_{DS}-V_{DS}, S-parameters, and NF_{min} can be simultaneously obtained.

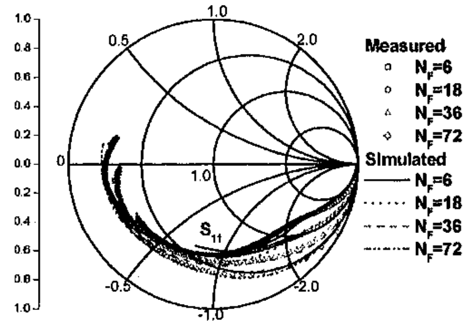
B. S-parameters and de-embedded noise modeling:

Figs.7(a) and (b) show the measured and modeled S-parameters for 65nm and 80nm n-MOSFETs with various finger numbers (N_F=6,18,36,72). Good agreement between modeled and measured S-parameters is obtained over the wide range of frequencies from 200 MHz to 40 GHz. It is noted that the S_{11} are translated from capacitive to inductive mode at higher frequencies for the devices with large finger number (N_F =72). It indicates the dominance of parasitic inductance existing in the transmission line connected to the gate terminals. This result suggests the gate transmission line effect plays a significant role particularly at high frequencies. The good agreement between measured and modeled S-parameters justifies the accuracy of our equivalent circuit model shown in Fig. 6.

Based on the equivalent circuit model that has been well verified by S-parameters, we further analyzed the intrinsic MOSFETs by de-embedding the pad and gate transmission line effect. The de-embedding procedure used in this work is simply abstracting the modeled pad coupling capacitance, RC shunt paths, and transmission line series resistance R_{TML} and inductance L_{TML} in Fig. 5 from the original MOSFET model shown in Fig. 6. This is justified by good fit to the de-embedded noise using our method and match with that calculated by noise correlation matrix method [6]. The de-embedded S-parameters have pure capacitive nature of S_{11} for both 65 nm and 80 nm n-MOSFETs (not shown) that is physically due to gate capacitances. The parasitic inductance originated from the transmission line also explains well the inductive behavior at higher frequencies before de-embedding. Fig.8(a) illustrates the inductive mode impedance extracted from Z-parameters for 65 nm devices with the mentioned splits of N_F (6,18,36,72). The less negative values at higher frequencies accounts for the gradual dominance of inductive mode impedance. Basically, transmission line in series with the gate behaves like an inductive mode impedance at higher frequency and the inductance obviously increases with increasing the gate finger number as shown in Fig.8(a). As for N_F=72, L_{TML}=30pH is extracted to fit the imaginary part of Z-parameters, i.e. $Im(Z_{11}-Z_{22})/\omega$ quite well as illustrated in Fig.8(b).



(a)



(b)

Fig. 7. The measured and simulated S-parameters of (a) 80nm and (b) 65nm n-MOSFETs with N_F=6,18,36,72. Good agreements between measured and modeled S-parameters are obtained to fit in the Smith chart. The inductive behavior at high frequencies is due to the parasitic inductance generated by the gate transmission line

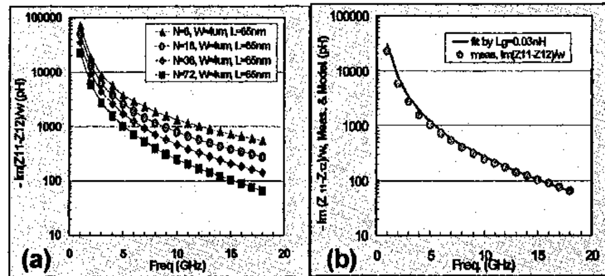


Fig.8 The gate inductive impedance extracted from Z-parameters for 65nm NMOS (a) different finger numbers, N_F=6,18,36,72 (b) good fit to $Im(Z_{11}-Z_{12})/\omega$ by L_{TML}=30pH as extracted

Using the simple transmission-line de-embedding method, we simulated the RF noise for the 65 nm and 80 nm MOSFET with various finger numbers (N_F =6,18,36,72). Fig. 9(a) and (b) show the measured and de-embedded results and the comparison between noise correlation matrix method and the proposed transmission line model (TML)

model. Agreement in terms of the de-embedded NF_{min} between our TML model and noise correlation matrix method is achieved in the frequencies from 1 to 18 GHz. Also, good match with the measured NF_{min} before de-embedding is realized by the TML model for the full structure shown in Fig.6 with all the proposed R, L, C parasitics included. Our study suggests that capacitive coupling effect played by the pad and RC shunt path representing the substrate loss becomes the major factor rendering the extra RF noise. The impact increases significantly with reducing the device size like finger number (N_F). As for the smallest devices in this study, i.e. N_F=6, extra noise of around 4~4.5dB at 10GHz was contributed by the pad parasitic and substrate coupling effect. The intrinsic NF_{min} extracted by our TML model can be as small as 1.0 dB at 10 GHz, even for the smallest devices with N_F=6 and largest R_g (>20Ω in Fig.2), which is comparable with the best record published in literature and suitable for wireless communication from handset to future X-band. Besides, matrix correlation method based on S-parameter de-embedding indicates quite consistent result that intrinsic NF_{min} can be reduced to around 1.0 dB at 10GHz as shown in Fig.9 (a) and (b) for 65 nm and 80 nm devices respectively.

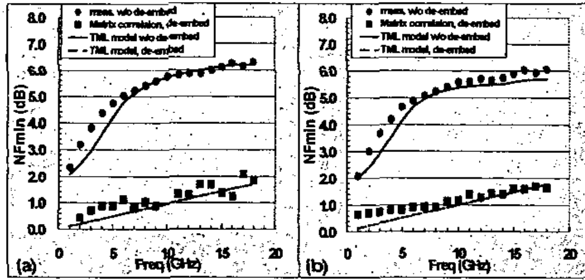


Fig.9 Comparison of NF_{min} among measured, de-embedded by correlation matrix method, and TML model for the smallest devices with N_F=6 (a) 65nm (b) 80nm NMOS

Regarding the gate length scaling effect on NF_{min}, comparison was done as shown in Fig.10 for 65 nm and 80 nm devices after de-embedding by using our TML model. The smaller NF_{min} achieved by 65 nm as compared to 80 nm devices at higher frequency is attributed to the higher f_T (155 GHz vs. 115 GHz) suggested by Fukui formula in eq.(1). The smaller R_g achieved by 65 nm as shown previously in Fig.2(b) is considered one more contributor. The advantage of our proposed method compared to the noise correlation matrix method [6] is the easier simulation without resort to complicated matrices calculations.

$$F_{min} = 1 + K\sqrt{g_m(R_g + R_s)}\frac{f}{f_T} \qquad (1)$$

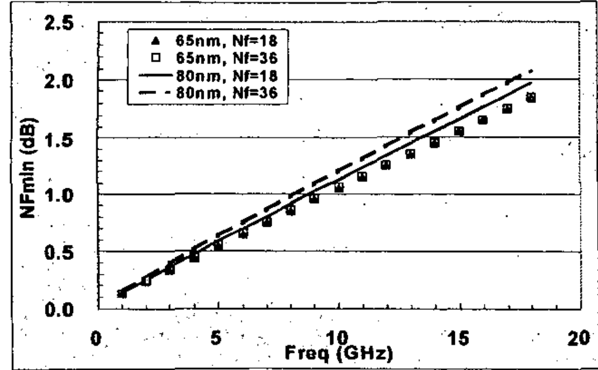


Fig.10 Gate length scaling effect on intrinsic NF_{min} extracted by TML model and ADS simulation. Comparison between 65nm and 80nm NMOS with N_F=18, 36 shows lower NF_{min} for 65nm than 80nm device at higher frequencies

Conclusion

We have successfully extracted the intrinsic RF noise for multi-fingered MOSFETs with aggressively scaled gate lengths (80 nm and 65 nm) by using a simple transmission line de-embedding method. Our proposed method can achieve close agreement with the published noise correlation matrix method but without using complicated matrices calculation.

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