Fabrication of Thin-Film Transistors on Plastic Substrates by Spin Etching and Device Transfer Process

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Abstract –This work presents a novel method to transfer thin-film transistors from a Si wafer to another flexible plastic substrate. First, high-performance poly-Si TFTs were fabricated on 1-μm thick SiO_2 of a Si wafer and then adhered to a flexible plastic substrate by the optical adhesive. Next, the spin-etching process was utilized to remove the backside Si with SiO_2 as a stopping layer. We have established a qualitative model to explain the relation between the chemical flow rate/rotation speed to the etching rate and the uniformity of Si removal. The Si etching rate is higher than 200 μm/min while maintaining Si to SiO_2 selectivity of 250 under optimized spin-etching parameters. Compared to that before transference, no degradation or yield loss was found due to substrate bonding and Si spin-etching steps. Additionally, extrinsic stress shows little effect to the properties of poly-Si resistors on the flexible plastic substrate.

Keywords: poly-Si Thin-Film Transistor, spin etching, plastic substrate, stress

I. Introduction

Thin film transistors (TFTs) on flexible plastic substrates were of considerable interest due to their light weight, thinness, flexibility, shock resistance, and low cost for large area electronics such as active matrix liquid crystal display (AMLCD), "smart" labeling of consumer items, smart cards and sensors [1-5]. However, the fabrication of high performance TFTs on plastics is extremely challenging for the following reasons: First, the maximum process temperature must be lower than the glass transition temperature T_g so that many conventional high temperature process such as oxidation, recrystallization or activation should be modified. Second, since the thermal expansion coefficient of plastic substrate (6.2×10^{-5}/℃) is greatly larger than that of Si (2.4×10^{-6}/℃), the misalignment during lithography or film cracking may contribute to process issues. Finally, reproducibility and manufacturability on flexible substrates should also be addressed.

Two kinds of approaches have been investigated to overcome these preceding obstacles. One method utilized various low temperature processes including excimer laser annealing, metal-induced lateral crystallization, PECVD, and sputtering, etc. to fabricate TFTs on plastic substrates directly [1,5]. The other method, indirectly, fabricated TFTs first on a glass or quartz substrate and then transferred the devices to the plastic substrate by etching or laser ablation [6-7]. Furthermore, we had proposed a novel device transfer by backside etching (DTBE) technique that combined both chemical-mechanical polishing (CMP) and wet chemical etching processes to fabricate TFTs on a thick glass or plastic substrate [8]. Comparing to the other methods, the DTBE technique requires no expensive excimer laser equipment and is compatible with matured CMOS process with the highest process temperature up to 1100℃.

In this work, the CMP step in the previous DTBE method was replaced by the spin-etching process. In contrast to CMP, the spin-etching process obtains little mechanical stress or thermal stress to the sample, so that the device transference to a thin flexible backplane can be realized. Besides, the chemical consumption of spin-etching is more economic than that of conventional wet etching process. Including spin-etching properties, the mechanism, and the electrical characteristics of transferred thin-film devices were investigated in this research.

II. Experiment

A. Spin etching process

Before transferring the thin-film devices to the plastic substrate, the properties of spin-etching process including etching rate, uniformity and selectivity, etc. should be clarified. The schematic diagram of our spin etching equipment was shown in Fig.1, where the etching chemicals were filled in a funnel and dropped into the spinner through a manual valve with an adjustable flow rate. The spinner was composed of Teflon and was manufactured by Laurell Technologies Corp. Besides, we utilized a mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and some acetic acid

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(CH_3COOH) as the main etchant for silicon. The spin speed of samples varies from 1000 to 4000 rpm, while the flow rate of etchant ranges from 100 ~ 333 ml/min.

The etching rate of silicon was calculated from the variation of sheet resistance R_S of a 4-inch wafer before and after spin-etching process, i.e. the change of wafer thickness can be expressed as

$$\Delta \text{thickness (T)} = \rho/R_{S\text{-before}} - \rho/R_{S\text{-after}}$$

where ρ is the resistivity of a Si wafer.

In order to test the etching selectivity of Si to silicon nitride or silicon dioxide, a layer of 2300 Å Si_3N_4 or a 6000 Å thick SiO_2 was formed on a Si substrate by LPCVD and wet oxidation, respectively. Not only the etching selectivity but also the etching uniformity can be accurately measured by ellipsometer.

B. Fabrication of thin-film devices

For DTBE process, both poly-Si resistors and thin-film transistors were fabricated on the 4" wafers as shown in Fig.2(a). First, a 1.5-μm thermal oxide layer was grown on a Si substrate as the etching-stop layer to poly etchant. Next, a 1000 Å amorphous Si layer were deposited by LPCVD at 550℃ and patterned as an active region. Following was a gate oxide of 1000 Å and a poly-Si layer of 250-nm for gate electrodes or resistors. A self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} at 60 keV was carried out to form the source/drain areas.

After depositing the passivation oxide by PECVD and opening the contact holes, a 50-nm Ni layer was evaporated at the contact windows and then a 550℃ furnace annealing for 48 hrs was performed to recrystallize the channel region and to active the dopants simultaneously. Afterward the samples followed a standard backend process to form the source/drain and gate electrodes. Finally a passivation process with NH_3 plasma for 1 hour was accomplished. Before transferring thin-film devices to the plastic substrate, the electrical characteristics of TFTs and poly-resistors were measured by Agilent 4156.

C. Device Transfer Process

After measuring the device characteristics, a 3000 Å TEOS-oxide was deposited on the surface to protect the TFTs from being damaged by the organic adhesive. Next, as shown in Fig.2(b), the device wafer was bonded to the plastic substrate by the optical adhesive and then cured at 80℃ for 3 hours on a hot plate. Afterward, we utilized spin-etching process with Si etchant to remove the backside Si. As the thickness of backside Si reduces, the flexible plastic substrate tends to deform due to its low Young's modules. Therefore, it is required to attach a supporting glass substrate below the plastic substrate to prevent the sample from cracking during Si backside etching process.

The spin etching step would automatically stop because the Si etchant has a high etching selectivity of 250 to the etching stop layer, SiO_2. Finally, a photo lithography process was performed to open the contact pads as shown in Fig.2(c). Again the electrical characteristics of TFTs or poly resistors were measured to examine the influence of DTBE.

II. Results and Discussion

A. Spin etching process

For isotropic etching of silicon, the most commonly used etchants are mixtures of hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH), the so-called HNA system [9] or poly etcher. The reaction is initiated by promoting Si from its initial state to a higher oxidation state:

$$Si + 2h^+ \rightarrow Si^{2+}$$

The holes are produced by the following autocatalytic process:

$$HNO_3 + HNO_2 \rightarrow 2NO_2^- + 2h^+ + H_2O$$

$$2NO_2^- + 2H^+ \rightarrow 2\,HNO_2$$

Si^{2+} combines with OH^- (from the dissociation of H_2O) to form $Si(OH)_2$, which subsequently liberates H_2 to form SiO_2. SiO_2 then dissolves in HF:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + H_2O$$

The overall reaction can be rewritten as

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2$$

Here the acetic acid acts as a buffer agent, which controls the dissociation of the nitric acid and preserves the oxidizing ability of HNO_3 for a wide range of dilution during the etching process.

The most serious problem encountered during backside etching is the process temperature. Since the thermal expansion coefficients of Si and the polymeric materials are significant, the plastic substrate will easily roll up and cause the Si to peel off the plastic due to the exothermic reaction of backside etching process. Moreover, many plastic substrates and adhesives would be eroded by hydrofluoric or nitric acid, so the conventional wet etching process is not suitable. For spin-etching process, however, the sample is being spun at a high speed, while the fresh cool chemicals supply continuously to the wafer surface; therefore, the influence of temperature is greatly eliminated and the plastic substrate or adhesives are not damaged, either.

Figure 3(a) and (b) illustrate the curves of etching rate versus flow rate and rotation speed, respectively. From Fig.3(b), it can be found that the etching rate increases with the rotation speed, and the maximum etching rate exceeds 200 μm/min, occurring at the

highest spin speed of 4000 rpm with a chemical flow rate of 167 ml/min. Consequently, spin etching is a very efficient process compared to conventional wet etching (~2 μm/min @ 25℃). For a 4-inch wafer with thickness of 550 μm, the DTBE process can be fulfilled within 3 ~ 5 min. Nevertheless, Fig.3(a) shows that there is no apparent relationship between the etching rate and flow rate under a fixed spin speed. Specifically, the etching rate reaches a maximum value at the flow rate of 167 ml/min and reduces notably above the flow rate of 200 ml/min.

In order to further explain the observed phenomenon, we proposed a simple mechanism about the spin-etching process as shown in Fig. 4. The etching procedure contains three steps:

(a) First, a boundary layer was formed near the silicon surface where the etching species were consumed rapidly. All of the reactants should diffuse through this boundary layer to support the reaction (mass transport control).
(b) The reaction species at the surface, e.g. HNO_3 and HF, will react with Si. This process is highly dependent on the temperature (surface reaction control).
(c) The reaction byproducts diffused through the boundary layer and returned to the bulk of liquid (byproduct diffusion control).

For spin-etching process, the spin speed mainly affects the step (a) and step (c), because a higher rotation speed would result in a thinner boundary layer and thus a faster diffusion rate for both reactants and byproducts. Accordingly, as shown in Fig.3(b), the etching rate keeps increasing with spin speed for every condition of flow rates and gradually saturates when the rotation speed larger than 3000 rpm, implying that the system is now in the surface reaction control regime. In this regime, more etching chemicals (a large flow rate) may cool down the sample surface and slightly affects the reaction rate.

At a slow rotation speed (<2000 rpm), however, the total process looks more like a conventional wet etching rather than a spin etching process. With little help from the centrifugal force, the reaction byproducts near the silicon surface would now be repelled by the supplying chemicals so that the etching rate increases with flow rate from 100 to 167 ml/min as shown in Fig.3(a), indicating that the system is in the diffusion control regime. Moreover, the system will leave the diffusion control regime and enter the surface reaction control regime as the flow rate increases. The etching speed decreases significantly owing to the cooling effect of chemicals.

Figure 5 exhibits the etching rate with respect to the etching uniformity for Si_3N_4. A 4-inch wafer with Si_3N_4 of 2300 Å was spun and etched by the poly etchant for totally 360 sec; every 120 sec, we stopped the etching process and measured the film thickness by ellipsometer. The process condition about the rotation speed is 4000 rpm and the flow rate is 100 ml/min. From Fig.5, we can find that not only the etching rate from wafer center to edge is very uniform, but the etching repeatability is also satisfactory (the information of film thickness near the wafer edge cannot be acquired by our equipment). The etching selectivity of Si to Si_3N_4 is larger than 10^4, showing that the silicon nitride formed by LPCVD is an ideal etching stop layer for poly etchant.

The etching characteristics of poly etchant to SiO_2 were also investigated. As shown in Fig.6, the etching rate increases with flow rate and gradually saturates when the flow rate exceeds 200 ml/min. Since the relative concentration of hydrofluoric acid is low in our poly etchant and consumed very fast during etching process, the etching mechanism is diffusion control, depending on the chemical refresh rate. Additionally, the rotation speed has insignificant influence to the etching rate except that at 1000 rpm. It is notable that the etching rate greatly increases at the lowest flow rate (100 ml/min) and rotation speed. We presumed that the temperature at the surface had arisen, resulting in the increment of surface reaction rates. The etching selectivity of Si to SiO_2 is larger than 150. Although this value is inferior to that of silicon nitride, a thick SiO_2 stop layer can be formed through wet oxidation and patterned easily with HF. Thus we chose SiO_2 rather than Si_3N_4 as an etching stop layer in DTBE process.

Figure 7(a) and (b) compares the etching uniformity for SiO_2 with different rotation speed. From Fig.7(a), we can observe an U-shape curve about etching uniformity, which can be further alleviated by increasing the rotation speed. Similar phenomenon can also be found during DTBE. Figure 8 shows a photograph of devices after being transferred to another plastic substrate by DTBE technique with spin speed of 4000 rpm and flow rate of 167 ml/min. The patterns were originally fabricated on a 4-inch (10 cm in diameter) wafer. During the spin-etching process, because the etching rate near the wafer edge and that at the wafer center is higher than the other area, patterns at these regions had been destroyed by poly etcher even with a protection of oxide stop layer. Finally, the transferred devices formed a ring-shape pattern with a diameter of 5 cm. To solve this problem, the nozzle structure should be modified to spray the etchant more evenly so that the etching rates all over a wafer are equal. The efforts for transferring larger samples with DTBE technique are still in progress.

B. Fabrication of Thin-Film Devices by DTBE

Since the devices were not directly fabricated on the plastic substrate with DTBE method, the requirements for the characteristics of plastic substrates are less strict. Nevertheless, the following properties for an optimal polymeric backplane are suggested:

(a) The glass transition temperature T_g of a plastic substrate higher than 130℃: The samples after transferring would undergo a photolithography process with hard baking temperature of photo resist at 120℃.
(b) Good chemical resistance, especially to HF, HNO_3, development (TMAH) and acetone (ACE)
(c) Low thermal expansion coefficient to ensure the accuracy of alignment during lithography process
(d) High transparency and low reflectance of the substrate for a transmission-type image display
(e) Low moisture absorption

Many conventional plastic substrates including polyethersulfone (PES), polyarylate (PAR), polycarbonate (PC) and polyethylene terephthalate (PET) meet the above criteria, but we utilized a new kind of cyclic olefin polymers (COP) named ARTON™ film in this work [10]. ARTON™ film, purchased from JSR corp., possesses several advantages such as good light transmittance above 93%, high T_g of 170℃, low water absorption and good adhesion to hard coatings, etc. Besides, the requirements for optical adhesives are similar to that for plastic substrate.

Figure 9(a) shows a flexible ARTON™ substrate with a die size of 3 cm × 3 cm that the TFT arrays had been transferred successfully. The optical microscope image of these devices observed with back light source is shown in Fig.9(b). The dark regions are aluminum pads, poly-Si gates and S/D electrodes, which are all opaque, while the white area is transparent plastic substrate/adhesive/SiO_2. The backside Si had been removed thoroughly during spin-etching process and no physical damage was found.

C. Electrical Characteristics of Thin-Film Devices after DTBE

Figure 10 illustrates the I_D-V_{GS} and field-effect mobility curves of a TFT before and after DTBE process. Notably, the DTBE process does not degrade the electrical characteristics of TFTs such as threshold voltage, mobility, ON/OFF current ratio and subthreshold swing. The field-effect mobility is 24 cm^2/Vs, extracted from the following equation [11]:

$$\mu_{FE} = \frac{L}{C_{ox} \cdot W \cdot 0.1} \times g_m$$

where L is channel length, W is channel width, C_{ox} is gate oxide capacitance and g_m is transconductance. The ON/OFF current ratio is larger than 10^6 while the threshold voltage is around 4 V. The variation of electrical properties found in our previous work is not observed, because this time the samples were all passivated by NH_3 plasma and the trap states in the grain boundary wouldn't be affected by the oxide capping layer [8].

For the application of flexible display, the electrical characteristics of devices on a bending substrate should not be deteriorated. To examine the influence of mechanical stress on the device performance, several testing bases with various radius of curvature were made; the poly resistors after transferring were fixed on the testing base and the electrical characteristics were measured, as shown in Fig.11. Figure 12 exhibits the plot for the confidence interval (CI) of average resistance with different bending cases. Since the average resistance before and after DTBE are quite similar even at the smallest bending curvature of 2 cm, we can conclude that the mechanical stress will not damage the thin-film devices for our test conditions.

III. Conclusions

Fabricating high performance thin-film transistors on plastics is extremely challenging. In this work, we proposed an indirect process for transferring thin-film devices on a silicon wafer to another polymeric backplane. The spin-etching process was applied to solve the issues resulted from heat. Moreover, the electrical characteristics of poly-Si resistors or TFTs don't change after transfer process and bending measurement, verifying the DTBE technique a practical method for fabricating thin-film devices on a flexible plastic substrate. Since the DTBE technique is highly compatible with modern CMOS process, an integration of image display and complex logic circuits on the plastic substrate can be expected.

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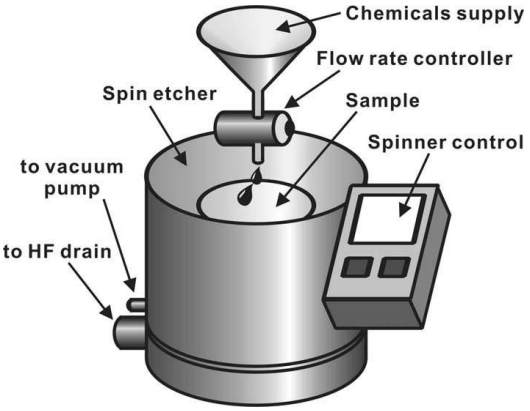


Fig. 1 The schematic diagram of spin-etching equipment

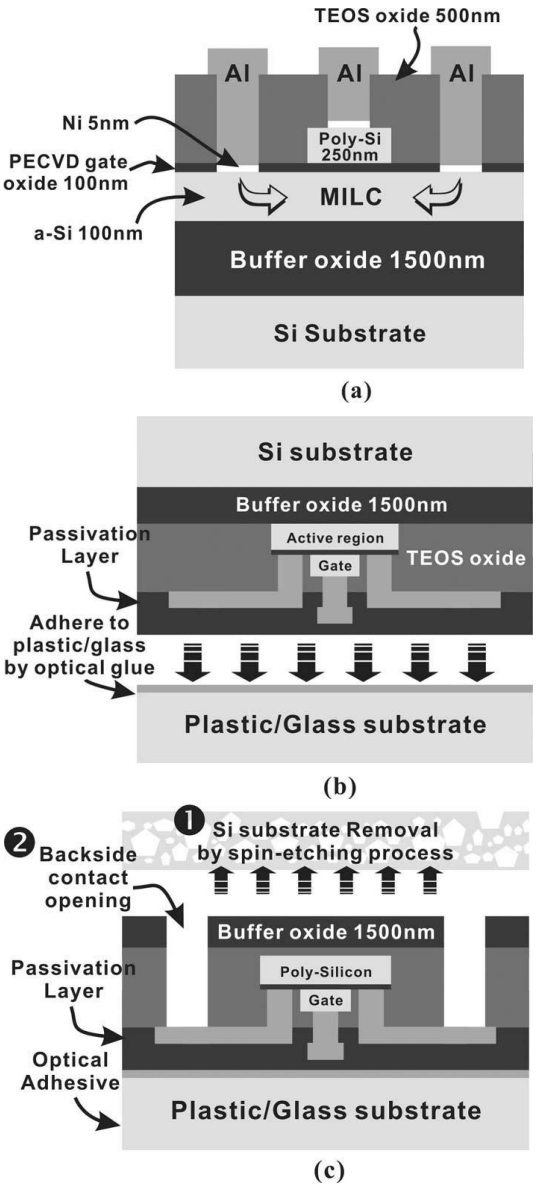


Fig. 2 The process flow of device transfer by backside etching (DTBE) technique

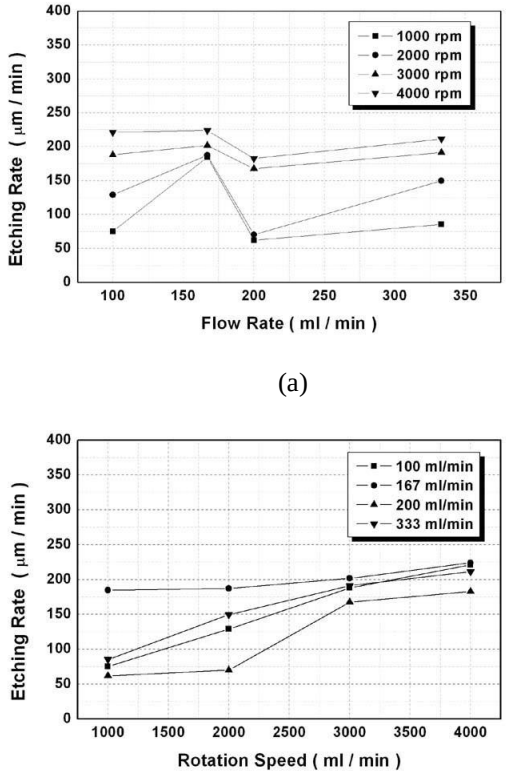


Fig. 3 Etching rate versus (a) chemical flow rate and (b) rotation speed

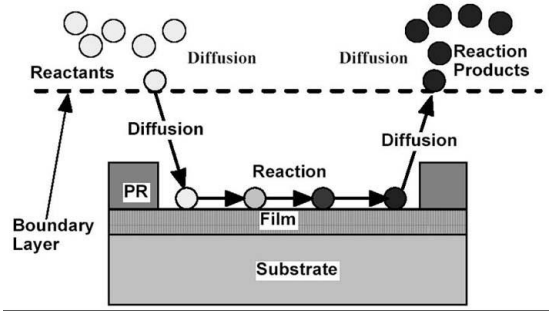


Fig. 4 The mechanism of spin-etching process

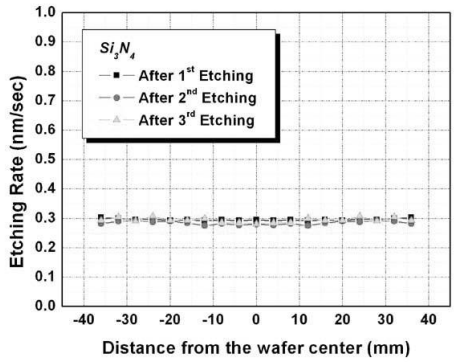


Fig. 5 Spin etching uniformity by poly etchant for silicon nitride film

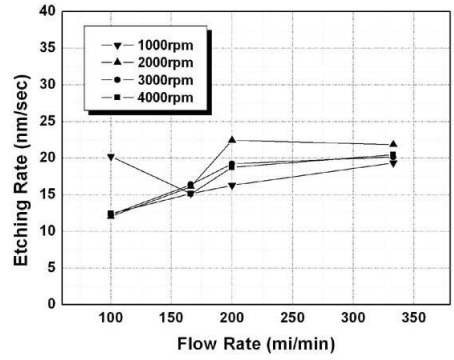
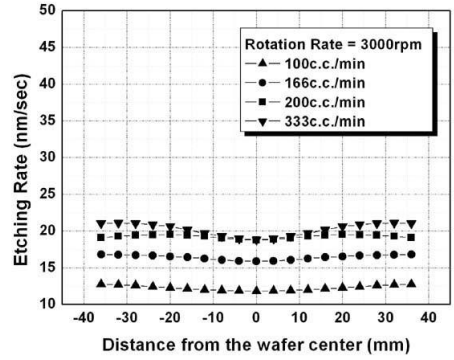
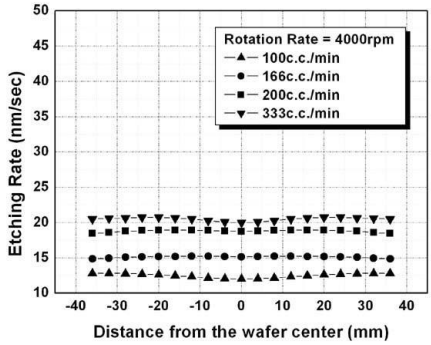


Fig. 6 Spin etching rate versus flow rate with various spin speed for silicon dioxide



(a)



(b)

Fig. 7 Spin etching uniformity by poly etchant for silicon dioxide with (a) 3000 rpm, and (b) 4000 rpm

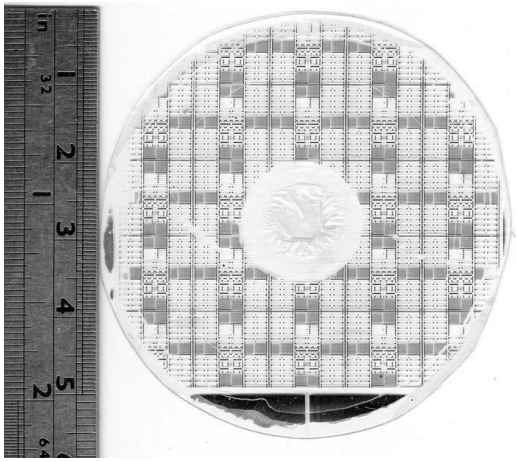
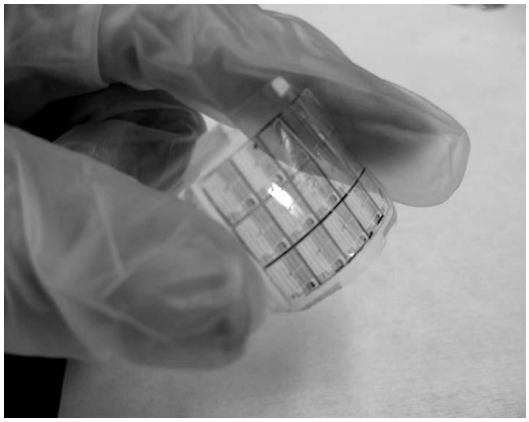
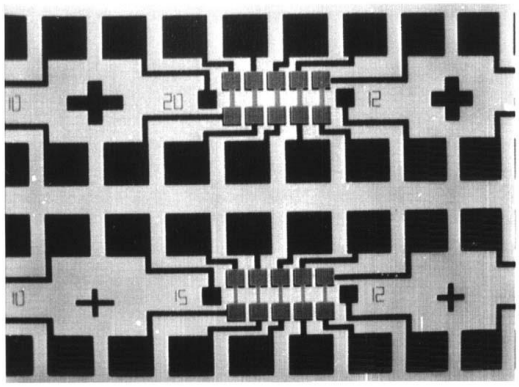


Fig. 8 A ring-type pattern with a diameter of 5 cm fabricated by DTBE technique



(a)



(b)

Fig. 9 (a) Photograph of several TFT arrays being transferred to a flexible plastic substrate, and (b) photograph of optical microscopy being observed with backside light source

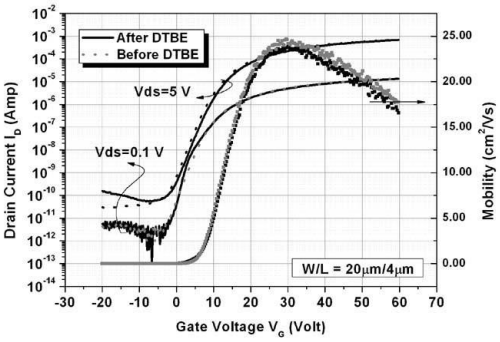


Fig. 10 Id-Vg curves as well as mobility curves of TFTs before and after DTBE process

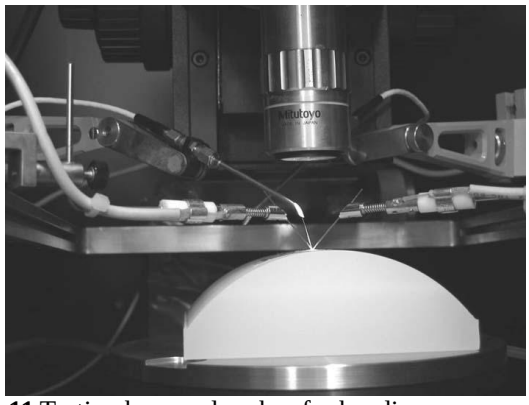


Fig. 11 Testing base and probes for bending measurement

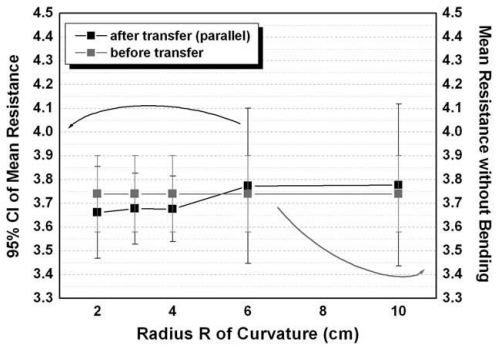


Fig. 12 Resistance of poly resistors under different extrinsic stress