Low-Temperature Processed MOSFET's with Liquid Phase Deposited $SiO_{2-x}F_x$ as Gate Insulator

Ching-Fa Yeh, Shyue-Shyh Lin, and Tzy-Yan Hong

Abstract—**Device performances of MOSFET's with $SiO_{2-x}F_x$ gate oxides prepared by an extremely low-temperature (15°C) liquid phase deposition (LPD) method were investigated. The electrical characteristics, including threshold voltage of 2.1 V, peak effective mobility (μ_{eff}) of 525 $cm^2/V \cdot s$, and subthreshold swing of 134 mV/decade, show the devices exhibit comparable performance to other low-temperature processed MOSFET's. This demonstrates that LPD $SiO_{2-x}F_x$ can be a suitable candidate for future gate insulators in low-temperature processed MOSFET's.**

I. Introduction

CURRENT demand for reduced device dimensions, and increasingly complex device structures, have stressed the need for low-temperature processing [1]–[5], while high-temperature processing can redistribute impurities and thus generate defects. This is especially true during MOSFET gate oxide formation where many defects in high-temperature thermally grown SiO_2 film are responsible for early breakdowns [6], [7]. To date, a few MOSFET studies have looked at deposition of gate oxide at low temperatures [2]–[5]. Although they demonstrated some benefits, some of the methods still required high-temperature post-deposition treatment to improve device performance [2], [4]. In addition, all needed expensive apparatus and complex processing to prepare the low-temperature gate oxide.

Recently, a novel room-temperature liquid phase deposition (LPD) technique using inexpensive apparatus was developed for silicon oxide ($SiO_{2-x}F_x$) [8], [9], where the fluorine will be naturally incorporated into the film during deposition. The LPD $SiO_{2-x}F_x$ also showed comparable performance of breakdown field and leakage current to other low-temperature prepared oxides. Because it had been reported that the fluorine incorporated in the MOSFET gate oxide evidently improves the interface characteristics and increases immunity to hot-electron induced stress [10]–[12]. Thus, we were interested in applying this low-temperature $SiO_{2-x}F_x$ processing method to MOSFET gate insulators. This paper presents the electrical characteristics of MOSFET's made with such a new LPD gate oxide, and compares them with those of other types of low-temperature processed MOSFET's.

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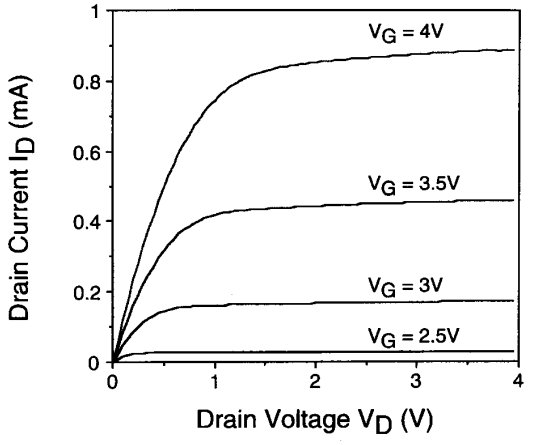
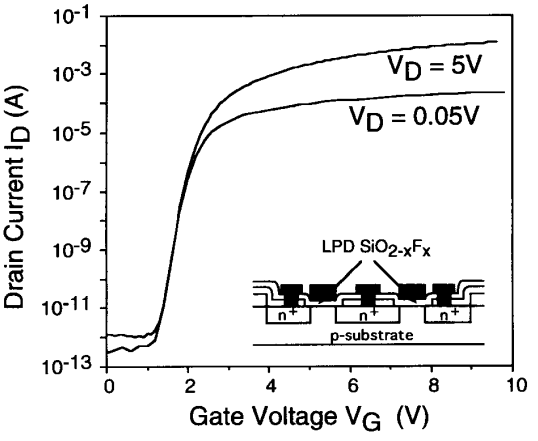


(a)



(b)

Fig. 1. The typical (a) I_D–V_D, and (b) I_D–V_G characteristics of MOSFET's with LPD $SiO_{2-x}F_x$ gate oxide. The inset in (b) shows the cross-sectional view of the fabricated device.

II. Experimental

N-channel MOSFET's with aluminum gates were fabricated on 1–5 $\Omega \cdot$cm, (100), p-type silicon substrates. A typical cross-sectional view of the fabricated device is shown in the inset of Fig. 1(b). The channel length (L) and channel width (Z) are 20 μm and 942 μm, respectively. The fabrication used conventional four-mask processes without channel implantation. 100 nm-thick LPD $SiO_{2-x}F_x$ formed at 15°C was first

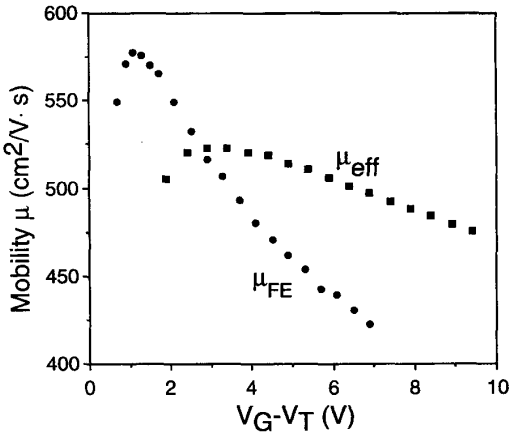


Fig. 2. Effective mobility (μ_{eff}) and field-effect mobility (μ_{FE}) versus V_G–V_T of MOSFET's with LPD gate oxide.

used as gate insulator. Specifics concerning the deposition process of LPD oxide were the same as those in our previous works [8], [9]. Because the fluorine disappeared and the film became denser as the LPD $SiO_{2-x}F_x$ was treated at a temperature over 700°C [8], the processing temperature had to be carefully controlled to avoid affecting the LPD oxide. So in our MOSFET processes, thermal diffusion of phosphorus for the source and drain regions was adopted and performed before gate oxide deposition. In addition, we adopted an aluminum gate to replace the polycrystalline silicon gate, because aluminum evaporation has hardly any thermal effect on LPD oxide. Post-metal annealing at 400°C was the only high temperature process used after LPD oxide deposition. The resulting MOSFET electrical characteristics, such as drain-current (I_D) versus drain-voltage (V_D) or gate-voltage (V_G) were measured, and the device parameters including threshold voltage (V_T), subthreshold swing (S), and mobility (μ) were all analyzed. The interface state density (D_{it}) was also investigated with MOS capacitors by high-frequency method [13].

III. Results and Discussion

An Auger electron spectroscopy (AES) depth-profile of LPD oxide film has revealed that fluorine is uniformly distributed in the film [14]. The mechanism of fluorine incorporation has also been proposed [14]. Fig. 1(a) shows the typical I_D–V_D characteristics of our MOSFET with V_G varied in the range from 2 V to 4 V in 0.5 V steps. The I_D–V_D curve exhibiting triode characteristics and current saturation phenomena well, reveals a typical drain characteristic for a long-channel MOSFET. Because there is no current flowing at $V_G = 2$ V, we know that the V_T will be larger than 2 V. With accurate plotting of transconductance (g_m) versus V_G, the 2.1 V of V_T was obtained to confirm the above result. The fact that this value of V_T is lower than the 4 V of in other studies [2] indicates that there are fewer fixed oxide charges contained in the LPD oxide. The typical I_D–V_G characteristics of our MOSFET with $V_D = 0.05$ V and 5 V, are also shown in Fig. 1(b), shown the drain current varies exponentially with V_G in the subthreshold region. And the curves in the subthreshold region show virtually no dependence on the drain voltage. The peak transconductance calculated at $V_D = 0.05$ V is 3.68×10^{-5} s. Moreover, the subthreshold slope calculated from the I_D–V_G curve is 134 mV/decade, which reveals superior to the 170 mV/decade recorded in other studies [2]. Although above results shows that our devices exhibit worse electrical characteristics than those conventional ones with thermal oxide, they exhibit comparable performance to other low-temperature processed MOSFET's.

TABLE I
Summaries of Device Performances for MOSFET's Utilizing Various Gate Oxide Deposition Methods

	LPD gate oxide	O_2-Ar sputter-deposited gate oxide [2]	PECVD gate oxide [5]
Gate electrode	Aluminum	Polysilicon	Aluminum
Deposition temperature	20°C	200°C	350°C
Post-annealing Temperature	400°C	800°C	400°C
Midgap D_{it} ($eV^{-1}cm^{-2}$)	1.8×10^{11}	5.0×10^{10}	2.7×10^{11}
Threshold voltage V_T (V)	2	4	—
Subthreshold slope (mV/decade)	134	170	—
Peak mobility μ_{FE} ($cm^2/V \cdot s$)	580	700	413

Since the MOSFET mobility is strongly influenced by the surface states at or near the interface and by the morphology of Si/SiO_2 interface, it is essential to evaluate the mobility when investigating the interface quality. Fig. 2 shows the effective mobility (μ_{eff}) and field-effect mobility (μ_{FE}) versus the V_G–V_T. The μ_{eff} and the μ_{FE} are given by $\mu_{\text{eff}} = g_D \cdot L/Z \cdot C_{ox} \cdot (V_G–V_T)$ and $\mu_{\text{FE}} = g_m \cdot L/Z \cdot C_{ox} \cdot V_D$, respectively, where g_D is the channel conductance, C_{ox} is the gate capacitance per unit area. The mobility curves are highly consistent with those of MOSFET's with thermal gate oxide [15]. The peak μ_{eff} is 525 $cm^2/V \cdot s$, while the peak μ_{FE} is 580 $cm^2/V \cdot s$. The μ_{FE} is lower than μ_{eff} over almost the entire gate voltage region, because the derivation of μ_{FE} neglects the dependence of gate voltage [16]. The fact that mobility decreasing with gate voltage can be attributed to the enhanced surface roughness scattering with increased gate voltage [15]. In comparison with other words, our peak μ_{FE} is larger than 413 $cm^2/V \cdot s$ [5] but is less than 700 $cm^2/V \cdot s$ [2] of other works. These results show that the interface properties of Si/LPD $SiO_{2-x}F_x$ are superior to those of Si/PECVD SiO_2 but inferior to those of Si/O_2–Ar sputter-deposited oxide. As compared in Table I, the D_{it} of our device is lower than that of sputtered oxide device, but higher than that of PECVD oxide device. The least D_{it} for the sputter-oxide device may be attributed to a high-temperature annealing, which was performed at 800°C after oxide deposition. And our devices having less D_{it} may be due to fluorine incorporation. It is because fluorine can passivate some interfacial dangling bonds, as well as remove some weak Si–Si or Si–O bonds, via Si–F formation [10]. However, it is impossible to directly prove the fact because we can not prepare any LPD oxide without fluorine incorporation. It is expected that the reliability of our

devices will show better than other devices without fluorinated gate insulator. The study has been in progress.

IV. Conclusion

We have applied a novel room-temperature LPD $SiO_{2-x}F_x$ to low-temperature processed MOSFET without high-temperature annealing. Its I_D–V_D and I_D–V_G curves exhibit excellent triode-like characteristics and subthreshold characteristics, respectively. All the device parameters were compared well to those of other low-temperature processed MOSFET's. These results reveal the great possibility of applying LPD $SiO_{2-x}F_x$ as a gate insulator in low-temperature processed MOSFET's in the future.

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