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Effect of Oxygen Impurity on Microstructure and Boron Penetration in a BF_2^+ Implanted LPCVD Stacked Amorphous Silicon p^+ Gated PMOS Capacitor

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ABSTRACT

Secondary ion mass spectroscopy (SIMS) and transmission electron microscopy have been used to characterize microstructure and boron penetration in BF_2^+ implanted amorphous silicon p^+ gated metal oxide semiconductor (PMOS) capacitors, in which oxygen is inadvertently introduced in the gate area during the low pressure chemical vapor deposition (LPCVD) process. Oxygen impurity is found to be incorporated in the LPCVD deposited amorphous silicon film by SIMS. During the break between the two successive depositions for the stacked amorphous silicon (SAS) gate, an ultrathin oxide layer is formed at the interface between the two LPCVD amorphous silicon layers. The two thinner layers lead to smaller grains in the SAS structure. The interfacial oxide layer is a diffusion barrier for oxygen, which causes a higher oxygen concentration and, in turn, retards the crystallization in the SAS structure. Both the interfacial oxide layer and the gate oxide can dissolve a significant amount of fluorine after annealing. Reduction of free fluorine near or in the gate oxide due to fluorine dissolution in the interfacial oxide layer plays a crucial role for suppressing the boron penetration in the SAS capacitor.

Introduction

It has been proposed to use p^+ polysilicon as a substitute for n^+ polysilicon as the gate material of a p-channel metal oxide semiconductor field effect transistor (MOSFET).[1] However, the p^+ polygate PMOS with a BF_2^+ implant suffers from boron penetration through the gate oxide to the silicon substrate causing electrical degradation. The boron penetration effect is enhanced in the presence of fluorine.[2,3] The p^+-PMOS capacitor with a gate using a single amorphous silicon layer (SAL) structure has been reported to be able to activate boron more efficiently, and hence less boron could penetrate into the channel.[4] In some other works, a stack structure was adopted for the p^+ gate to alleviate boron penetration. A p^+ gate which was fabricated by depositing an amorphous silicon film on the as-deposited polysilicon film is reported to have a better ability to suppress boron penetration in the p^+-PMOS device than a gate which was fabricated by two successive depositions of two polysilicon films.[5] The better suppression effect was attributed to the larger grain size in the top amorphous silicon film of the p^+ gate. On the other hand, a stacked amorphous silicon (SAS) gate structure, in which the gate is composed of two as-deposited amorphous films, was also proposed for the p^+ gate of PMOS devices to reduce the boron penetration effect, and better electrical characteristics were reported.[6] It was suggested that fluorine diffusion was retarded in the SAS gate due to a more complex grain boundary network because of a smaller grain size in the SAS gate. In this work, we used secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) to investigate the impurity distribution and the microstructure of the SAS and SAL gates of p^+-PMOS capacitors. A thin oxide layer is present at the interface between the two amorphous silicon layers in the SAS structure. The presence of the oxide layer can alleviate the fluorine-enhanced boron penetration effect.

Experimental

p^+ Polygate PMOS capacitors were fabricated on n-type <100> Si wafers with a resistivity of 2 ~ 3 Ω-cm. To improve the gate oxide quality, a 350 Å thick sacrificial oxide at 925°C was first grown on the wafers. The sacrificial oxide was stripped and an RCA clean was performed immediately prior to the growth of the gate oxide. The wafers were then dipped into a dilute HF solution to remove the native oxide before being loaded into the furnace. An 80 Å thick gate oxide was grown at 900°C in diluted O_2 (N_2/O_2 = 6/1). Undoped amorphous silicon was deposited by the low pressure chemical vapor deposition (LPCVD) technique using SiH_4 right after the gate oxide formation. The deposition pressure and the deposition rate were set at 135 mTorr and 16.7 Å/min at 550°C, respectively. The SAS structure gate was prepared by two successive LPCVD amorphous silicon depositions on the gate oxide. The thicknesses of the bottom layer and the top layer were 50 and 200 nm, respectively. Between the two sequential depositions, the SiH_4 gas flow was stopped for 15 min. During the break, the wafer temperature was still kept at the deposition temperature and the system was purged with nitrogen at 570 mTorr. The SAL structure gate had a thickness of 250 nm. After deposition of the gate materials, the gate received a single BF_2^+ implantation at 60 keV. After the ion implantation, the wafer was covered with a low temperature oxide (LTO) at 400°C to prevent boron out-diffusion and to protect the surface of the film from the ambient during subsequent annealing cycles. After LTO capping, the p^+ gate was annealed in a dry nitrogen ambient at various temperatures. SIMS analysis was carried out with a Cameca IMS 5f system. The oxygen ion source with an impact energy of 8 keV was used for boron and fluorine analyses, and a cesium ion source with an impact energy of 14.5 keV was used for oxygen analysis.

Results and Discussion

Figure 1 shows SIMS depth profiles of oxygen, boron, and fluorine of the SAS and SAL p^+ gate PMOS capacitors having received a BF_2^+ implant dose of 5×10^{15} cm^{-2} and a subsequent postimplantation thermal treatment at 900°C for 30 min. The flatband voltage shift for the SAS and the SAL capacitor is less than 0.4 eV. According to the depth profiles, oxygen distributes through the gate region for both gate structures. Since oxygen concentration varies

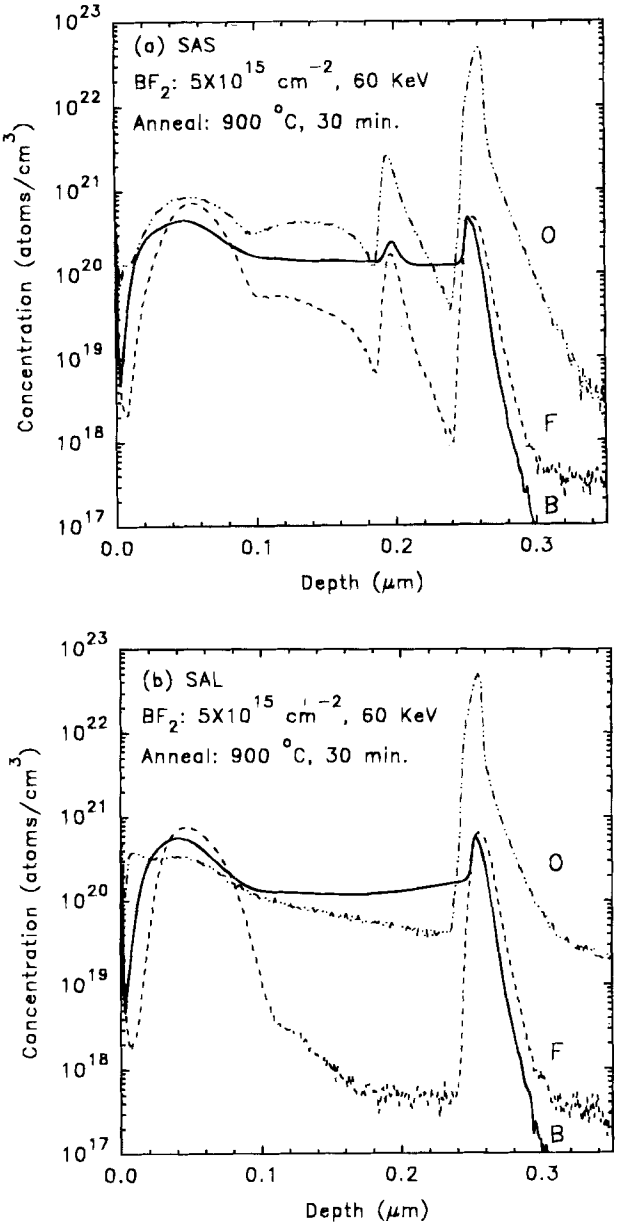

Fig. 1. SIMS depth profiles of oxygen, boron, and fluorine in (a) the SAS gate and (b) the SAL gate. Both gates have received a BF_2^+ implantation with a dose of 5×10^{15} cm^{-2} at 60 keV and a postimplantation anneal at 900°C for 30 min. The oxygen profile was obtained with a cesium ion source, and the depth profiles of boron and fluorine were obtained with an oxygen ion source.

widely within the capacitor studied in this experiment, it is difficult to select a proper relative sensitivity factor for oxygen which can faithfully quantify the oxygen depth profile over the whole sputtering depth. The oxygen concentration expressed in the depth profiles cannot reflect the true concentration if the oxygen concentration is far less than that of the gate oxide. Hence the oxygen concentrations described below are only for qualitative comparision. The oxygen concentration in the SAS gate is around 8×10^{20} atom/cm^3, except for the interface area between the two amorphous silicon layers, which has an oxygen concentration higher than 2.7×10^{21} atom/cm^3. The SAL gate has a smaller oxygen content, and the oxygen concentration is about 8×10^{19} atom/cm^3 over the range from 0.1 to 0.25 μm. Oxygen incorporation in the LPCVD polysilicon film is difficult to avoid because of residual oxygen containing gas species in the LPCVD system, and typical oxygen concentrations in the bulk of the LPCVD film vary from 10^{17} to 10^{19} cm^{-3}.[7] Oxygen containing gas species desorbed from components of the LPCVD system or inadvertently mixed in the reactant gas were possible sources for the oxygen impurity in the as-deposited LPCVD silicon film. The presence of oxygen may retard crystallization of the deposited amorphous silicon films and inhibit large polysilicon grain growth.[7,8] Cross-sectional TEM micrographs of the SAS and SAL structures after 900°C annealing are shown in Fig. 2. In the SAS gate, an abrupt narrow stripe with a thickness of ~1 nm between the two amorphous layers is clearly observable. An interfacial thin stripe is also observed in the cross-sectional TEM micrograph of the as-implanted SAS capacitor suggesting that the sharp boundary between the two polysilicon layers is not produced by thermal annealing. (The TEM micrograph of the as-deposited SAS gate is not shown here, but the image is similar to the one shown in Fig. 3a.) As shown in Fig. 1, the oxygen ion signal peaks at the interface region between the two polysilicon layers in the SAS capacitor indicating the narrow stripe is probably a thin oxide layer. Although oxygen is incorporated in both gate structures during the LPCVD process, only the SAS gate has the thin oxide layer. This suggests that the thin oxide layer is formed during the deposition break. Because of the lack of competition with the CVD reactant gas and deposition products for adsorption sites on the substrate surface during the deposition break, residual oxygen containing gas species will find more reaction sites for oxidation on the first amorphous silicon layer. The quality of the thin interfacial oxide layer is probably not as perfect as that of the gate oxide because of the inferior oxidation condition. The maximum oxygen concentration in the interfacial oxide layer is smaller than that of the gate oxide as shown in the SIMS depth profile of oxygen. This is likely due to the smaller thickness of the interfacial oxide layer, which leads to a smaller SIMS peak height because of the limited depth resolution under the fast sputtering condition. As shown in Fig. 3a, the oxide layer is about 2 nm thin, which is about one-quarter of the gate oxide thickness. Both gates have higher oxygen concentrations near the surface suggesting that oxygen out-diffusion occurs under the annealing condition. The much smaller oxygen concentration in the SAL gate implies out-diffusion is more complete in the SAL gate after the thermal treatment. Diffusion of oxygen in silicon

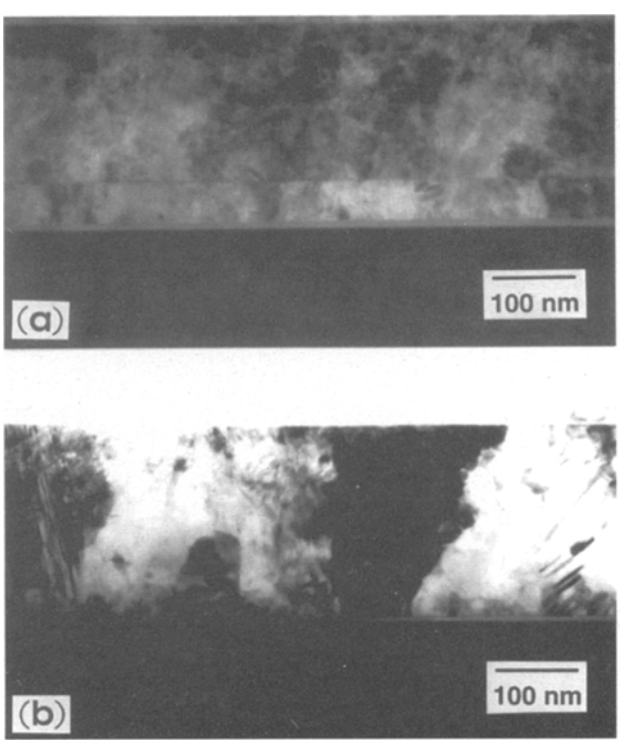

Fig. 2. Cross-sectional TEM micrographs of (a) the SAS gate and (b) the SAL gate both having received a BF_2^+ implantation with a dose of 1×10^{16} cm^{-2} at 60 keV and a subsequent postimplantation anneal at 900°C for 30 min.

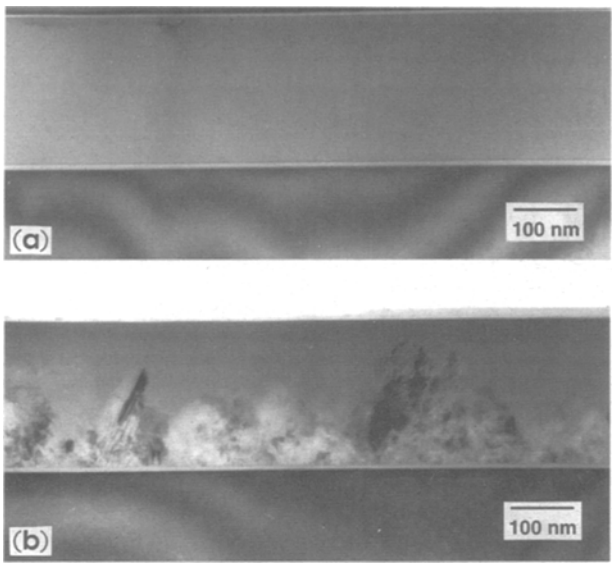

Fig. 3. Cross-sectional TEM micrographs of (a) the SAS gate and (b) the SAL gate both having received a BF_2^+ implantation with a dose of 5×10^{15} cm^{-2} at 60 keV and a subsequent postimplantation anneal at 600°C for 30 min.

occurs via an interstitial mechanism.[9] The more effective crystallization process and the larger grain size in the SAL gate, as is discussed later, are likely to enhance interstitial and grain boundary diffusion of oxygen in the SAL gate.

Besides, the higher level of the oxygen content in the SAS gate can significantly impede polysilicon grain growth in the amorphous silicon gate, and the interfacial oxide barrier limits the final size of grain growth. The interfacial oxide layer in the SAS gate separates the as-deposited amorphous silicon film into two parts with a thickness smaller than that of the SAL gate. This results in a smaller grain size in the SAS gate after crystallization. Based on the same reason, the grain size in the bottom layer of the SAS gate is smaller than that in the top layer. The interfacial oxide layer also hampers the nucleation process of the amorphous silicon. Figure 3 shows cross-sectional TEM micrographs of the two PMOS capacitors after having received a thermal treatment at 600°C for 30 min. An ultrathin stripe at the interface region between the two amorphous silicon layers can be clearly seen in Fig. 3a. After 30 min anneal at 600°C, the surface induced crystallization (SIC) phenomenon is evident for the SAL capacitor as shown in Fig. 3b. The grains in crystallized amorphous silicon usually have ellipsoidal shape.[10] An ellipsoidal grain can be clearly seen in the left portion of Fig. 3b. Grains are directly grown on the gate oxide surface, and the gate oxide is completely covered by a layer of polysilicon grains. This observation is in agreement with other reports regarding the SIC behavior of amorphous silicon.[11,12] In contrast to the SAL gate, the SAS gate did not show any perceivable grain growth under the same annealing condition as shown in Fig. 3a. We think that the SIC mechanism should occur in the SAS capacitor during crystallization as well. However, the presence of the thin interfacial oxide layer might make the crystallization behavior of the SAS capacitor more complex during the thermal treatment. In addition to the gate oxide surface of the SAS capacitor, nucleation and grain growth can possibly be launched on the interfacial oxide surface. The sharp boundary between the two polysilicon layers of the SAS gate shown in Fig. 2a suggests that two separate crystallization processes occur in the two layers under the annealing condition. However, since the interfacial oxide layer is not as perfect as the gate oxide as described previously, SIC occurring on the interfacial oxide surface is unlikely to be exactly the same as that on the gate oxide surface. Although nucleation rate and grain growth rate are temperature dependent, the longer incubation time for nucleation and grain growth at 600°C might imply that, even at higher annealing temperatures, the SAS gate is likely to take a longer time to accomplish crystallization compared to the SAL gate. Since it takes more time to complete the grain boundary network in the SAS gate, diffusion of impurities in the SAS gate is expected to be less effective than that in the SAL gate.

The smaller grain size in the SAS gate increases the grain boundary area and the length of the diffusion path to the gate oxide. For the SAL gate, because of the short diffusion path, fluorine will quickly diffuse to the gate oxide from the ion-implanted region once the grain boundary network is established by the crystallization processes. As shown in Fig. 1b, the fluorine concentration in the SAL gate is very low compared to the SAS gate over the range from ~0.1 to 0.25 μm. On the contrary, the fluorine profile for the SAS gate shows a hump between the interfacial oxide layer and the fluorine peak near the gate surface, which indicates a highly damaged region after crystallization of the implanted amorphous silicon gate.[13] Between the interfacial oxide layer and the gate oxide, a similar but narrower hump is also present. The complex feature of the fluorine depth profile for the SAS capacitor is likely due to a complex crystallization behavior during the thermal treatment. Fluorine can diffuse much faster in grain boundaries than in grains. A larger grain size for the as-deposited amorphous silicon gate has been suggested to reduce grain boundary area available for fluorine diffusion, and therefore the diffusion rate is smaller in the amorphous silicon gate.[4,5] However, in this work, fluorine diffusion in the SAL gate is much more efficient although its grain size is larger than that of the SAS gate. The retarded crystallization process in the SAS gate induced by the thin interfacial oxide layer may be responsible for the slower fluorine diffusion. In addition, the thin interfacial oxide layer and the gate oxide can dissolve a significant amount of fluorine as shown in the SIMS depth profiles. Fluorine accumulation at the interface between the two polysilicon layers in a stacked structure gate was also observed in other works.[5,6] However, the origin of the large quantity of fluorine accumulated at the interface was not explained. Fluorine can diffuse to silicon oxides and replace oxygen in the oxide resulting in additional oxide growth.[14] It is very likely that the high fluorine concentration in the interfacial oxide layer impedes further fluorine diffusion from the implanted region. Therefore, the amount of fluorine diffusing through the interfacial oxide layer to the gate oxide region is reduced, and thus reduces the fluorine concentration in the gate oxide. Although it is not clear presently how fluorine mediates boron diffusion in the silicon gate and the gate oxide, many studies show that the presence of fluorine indeed enhances boron penetration into the substrate.[2,3] Therefore less fluorine near or in the gate oxide region is likely to alleviate the boron penetration effect. In order to exhibit the effective suppression effect of the SAS gate for boron penetration, a more rigorous thermal treatment for the p^+ gate was performed. Figure 4 shows SIMS depth profiles of the SAS and SAL gates, which received a BF_2^+ implant with a dose of 5×10^{15} cm^{-2} and a subsequent thermal treatment at 950°C for 30 min. After the annealing, the fluorine peak near the surface region is broader for the SAS structure than the SAL structure. This is probably due to a more efficient out-diffusion behavior of fluorine in the SAL structure under the annealing condition. Both structures have a similar fluorine profile in the gate oxide area while a distinct difference in the boron profile is found. This is probably due to a slower diffusion behavior of fluorine in the crystalline silicon substrate. Therefore the position of the fluorine peak can be referred to the gate oxide region. For the SAL gate, boron has seriously penetrated into the silicon substrate. On the other hand, boron diffusion is almost stopped at the interface between the SAS gate oxide and the substrate. Only very little boron penetrates through the gate oxide. Although both gate structure capacitors show a large flatband voltage shift, the SAS structure can suppress boron penetration more effectively as far as material characteristics are concerned.

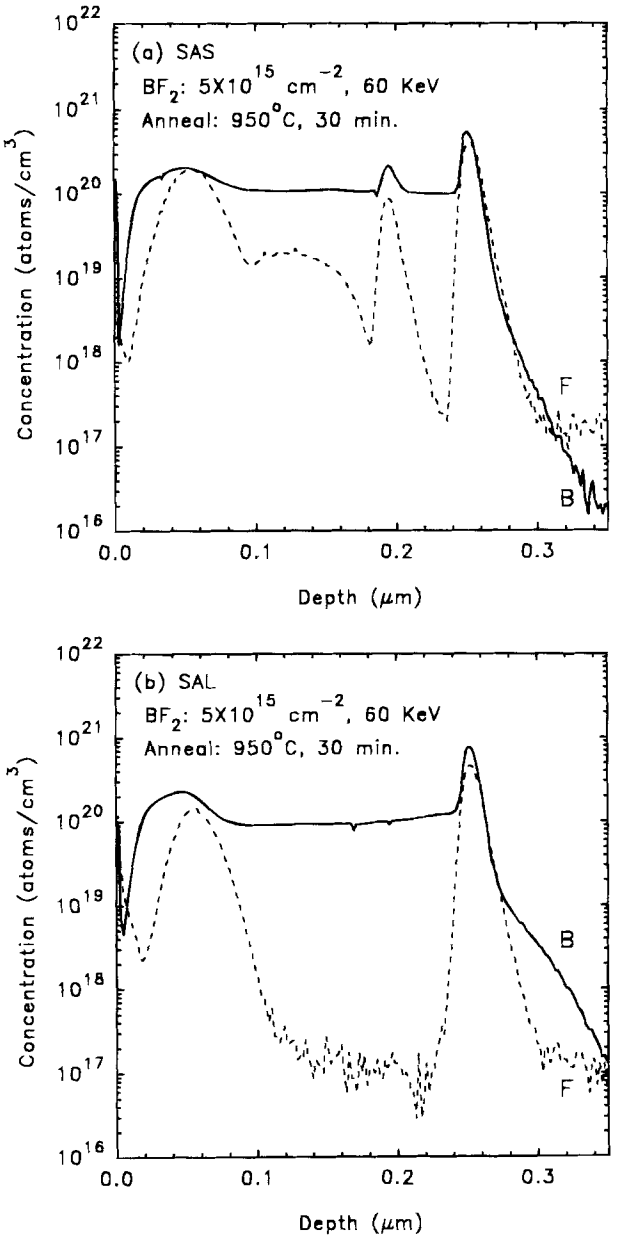

Fig. 4. SIMS depth profiles of boron and fluorine in (a) the SAS gate and (b) the SAL gate. Both gates have received a BF_2^+ implantation with a dose of 5×10^{15} cm^{-2} at 60 keV and a postimplantation anneal at 950°C for 30 min.

Conclusion

We have studied the effect of oxygen impurity on crystallization behavior of BF_2^+ implanted p^+ gate PMOS capacitors and boron penetration from the capacitors through the oxide to the substrate with TEM and SIMS. A large amount of oxygen is included in the LPCVD deposited amorphous silicon gates. For the SAS gate, an ultrathin oxide layer is formed during the break between the two successive LPCVD amorphous silicon depositions. The interfacial oxide layer in the SAS gate is a diffusion barrier for oxygen, and in turn the high oxygen concentration in the two thin amorphous silicon layers retards crystallization. The thinner layers also lead to smaller grains in the SAS structure after annealing. Fluorine can be dissolved in the interfacial oxide and thus reduces the concentration of fluorine diffusing to the gate oxide region during the postimplantation annealing. Hence the SAS gate structure suppresses boron penetration into the PMOS channel more effectively than the SAL gate.

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