A New Constant-Field Scaling Theory for MOSFET's

Jiin-Jang Maa, *Student Member, IEEE,* and Ching-Yuan Wu, *Member, IEEE*

***Abstract*—The constant-field scaling theory (CONFIST) is evaluated in this work. The persistence of the drain-induced barrier lowering characteristics is selected to be essential condition of the CONFIST. Assessment on the accuracy of various constraint equations for MOS device miniaturization is carried out and the application limitations of these equations are studied in detail. The intrinsic incompleteness of the original CONFIST is then revealed by scaling the constraint equation. It is found that the restriction of requiring invariant Poisson equation after scaling in the original CONFIST must be released to prevent the scaling from being limited by the *quasi-body effect*. The original CONFIST is revised accordingly, and the modified version (CONFIST-2) shows that the application limit of the original CONFIST is about 0.5 μm and the vertical dimensions must be scaled more than the lateral ones.**

NOMENCLATURE

B ($= 0.41\text{Å}^{1/3}$)	The empirical constant used in the constraint equation proposed by Brews *et al.*
$DIBL$ ($dibl$) ($\equiv \lvert dV_{TH}/dV_{DS}\rvert$)	The drain-induced barrier lowering (DIBL) factor (after scaling).
$L(l)$	The effective channel length (after scaling).
L_{min}	The minimum channel length above which the long-channel characteristics can be maintained.
$M(=(\pi^2/2\times\epsilon_s/\epsilon_{ox})^{1/2.8}\simeq 2.63)$	The proportional constant used in a new constraint equation.
m, n, a_{00} ($= 0.785/\mu$m, 0.80, 0.371)	The empirical constants used in the new constraint equation.
N ($= 2.2\ \mu\text{m}^{-2}$)	The empirical constant used in the constraint equation proposed by Ng *et al.*
N_A	The substrate doping concentration.
R_j	The source/drain junction depth.
R_1	The ratio of the DIBL factor after scaling to that before.
R_2	The ratio of the threshold voltage after scaling to that before.
T_{ox}	The thickness of the gate oxide.
V_{DS}	The drain to source bias voltage.
$V_{TH}(v_{th})$	The threshold voltage (after scaling).
W_{SD} ($= W_S + W_D$)	The summation of the depletion widths due to the source (W_S) and drain (W_D) junctions.
$Y_{DO}(y_{do})$	The depletion width under the gate without considering any two-dimensional effect (after scaling).
$Y_{JD}(y_{jd})$	The vertical depth of the depletion region at the drain end (after scaling).
$\epsilon_s(\epsilon_{ox})$	The dielectric permittivity of silicon (oxide).
$\phi(x, y)$	The two-dimensional potential distribution.
ϕ_{sinv}	The surface potential at the onset of heavy inversion.
ϕ_t	The thermal voltage.
λ	The scaling factor for lateral dimensions.
λ_d	The scaling factor for depletion depth.
κ	The scaling factor for potentials.
v	The scaling factor for vertical dimensions.

Manuscript received October 31, 1994. The review of this paper was arranged by Associate Editor K. Tada. This work was supported by the National Science Council, Taiwan, ROC, under Contract NSC-82-0404-E009-216.

The authors are with the Advanced Semiconductor Device Research Laboratory and Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, ROC.

IEEE Log Number 9411789.

I. INTRODUCTION

THE generalized scaling theory proposed by Baccarani *et al.* [1], which is usually called the constant-field theory (CONFIST), might be the most successful design guide for MOSFET miniaturization so far. The CONFIST decouples the Poisson equation and the current continuity equations for MOS devices operated in the subthreshold region. According to the CONFIST, the dimensions and the potentials are scaled separately to allow more flexible scaling as a qualified large device is scaled down, and the substrate doping concentration is constrained by requiring the invariance of the Poisson equation after scaling. In general, the unchanged Poisson equation implies unchanged solution to it, and the field configurations in the devices before and after scaling are supposed to be identical. The major assumption to guarantee the success of this theory is the concurrently proportional reduction of the boundary potentials with dimensions and power supply voltages. Obviously, we cannot expect the validity of this assumption due to the nonscalability of the built-in potentials. However, the original CONFIST [1] provides some valuable information about the scaling issues. In this paper, the limitations of the original CONFIST are carefully examined.

Some revisions will be suggested to make the CONFIST more appropriate for deep-submicrometer devices.

An alternative strategy was taken by Brews *et al.* [2], in which the subthreshold behaviors of devices within a certain range of structures were studied and an empirical formula to describe the relations among various structure parameters (e.g., T_{ox}, R_j, and N_A) was established. The acceptable minimum channel length $L_{\min}$ can be easily computed by this formula once T_{ox}, R_j, and N_A are given. Basically, $L_{\min}$ is a power function of T_{ox}, R_j, and W_{SD}. In general, a power function can be approximated by a linear one in a narrow window. Recently, Ng *et al.* [3] proposed a revised formula with the linear dependences of $L_{\min}$ on T_{ox}, R_j, and W_{SD}. Equivalently speaking, they take the Taylor expansion of the formula in [2] around the proximity of a center device, and the inflexible criterion used in [2] is replaced by the drain-induced barrier lowering (DIBL) factor.

In this paper, by simplifying the analytic threshold-voltage model developed in [4], a new constraint equation is developed to describe the behavior of the DIBL factor in terms of device structures. Comparisons among various constraint equations are given in Section II. Our constraint equation is then taken to be the basis for evaluating the CONFIST in Section III. The mathematical and physical problems of the original CONFIST are pointed out and the recommended improvement recipe will also be presented in the same section. A concluding remark is summarized in the final section.

II. Comparisons Among Various Constraint Equations

The schematic structure of a conventional MOSFET is shown in Fig. 1, where the physical meanings of the assigned parameters are given in the nomenclature. Based on Fig. 1, the first constraint equation for MOS miniaturization proposed by Brews *et al.* [2] is expressed by

$$L_{\min} = B[T_{ox}R_jW_{SD}^2]^{1/3} \tag{1}$$

where B is an empirical constant whose value depends on the units of each parameter used. Although (1) provides more flexible relationships among the corresponding structure parameters, its application is limited by some drawbacks which have been mentioned by Ng *et al.* [3]. The major weak points of (1) are a) the inappropriate limiting criterion (threshold current) used for determining $L_{\min}$, and b) the absence of the lower limit of $L_{\min}$ as one (or more) of the structure parameters vanishes. Point a) can be improved by replacing the limiting criterion with a more reasonable one, such as the magnitude of the drain-induced barrier lowering factor ($DIBL$) [3], [4]. On the other hand, the removal of the drawback b) must be achieved by performing some mathematical manipulations on (1). Equation (1) shows simple power relations among $L_{\min}$ and the structure parameters (i.e., T_{ox}, R_j, and W_{SD}). The independence among the three parameters allows the application of variable separation. We can then rearrange (1) to be

$$L_{\min} = f(T_{ox}) \times g(R_j) \times h(W_{SD}) \tag{2}$$

where

$$f(T_{ox}) = f_0 T_{ox}^{1/3} \tag{3a}$$

$$g(R_j) = g_0 R_j^{1/3} \tag{3b}$$

and

$$h(W_{SD}) = h_0 W_{SD}^{2/3}. \tag{3c}$$

Obviously, $B = f_0 \times g_0 \times h_0$ can be expected. If the devices under consideration are just small perturbations around a qualified center device with the parameters T_{ox0}, R_{j0}, and N_{A0}, which satisfy (2), the dependence of $L_{\min}$ on each parameter can be approximated by the Taylor expansions of $f(T_{ox})$, $g(R_j)$, and $h(W_{SD})$ around the center point (T_{ox0}, R_{j0}, N_{A0}). For example, around T_{ox0}, $f(T_{ox})$ can be approximated by

$$f(T_{ox}) \simeq \frac{f_0}{3T_{ox0}^{2/3}}(T_{ox} + 2T_{ox0}). \tag{4}$$

Thus, $L_{\min}$ varies linearly with T_{ox} and, furthermore, $L_{\min}$ becomes nonvanished even if T_{ox} approaches zero due to the addition of the term $2T_{ox0}$. Similar treatments can be applied to functions $g(R_j)$ and $h(W_{SD})$. Consequently, (1) can be rewritten as

$$L_{\min} \simeq B_T(T_{ox} + b_1)(R_j + b_2)(W_{SD} + b_3) \tag{5}$$

where

$$B_T = \frac{2B}{27(T_{ox0}^2 R_{j0}^2 W_{SD0})^{1/3}}. \tag{6}$$

The values of B_T, $b_1 (= 2T_{ox0})$, $b_2 (= 2R_{j0})$, and $b_3 (= W_{SD0})$ are detemined by the limiting criterion and the structure parameters of the selected center device. Recently, Ng *et al.* [3] proposed a new generalized miniaturization guide by revising (1) according to the above arguments. They obtain a linear relation like (5) from the induction of the systematically simulated device characteristics. For convenient discussions, their result is written below:

$$DIBL = \left[\frac{N}{L}(T_{ox} + n_1)(R_j + n_2)(W_{SD} + n_3)\right]^{1/0.37} \tag{7}$$

where $N = 2.2\ \mu\text{m}^{-2}$, $n_1 = 0.012\ \mu\text{m}, n_2 = 2.9\ \mu\text{m}$, and $n_3 = 0.15\,\mu\text{m}$. The mathematical basis of their analysis is evidently the termwise Taylor expansions of (1) as discussed above. It is noted that equation (7) is an approximation of (1) in a narrow window. The application range of (7) needs careful considerations.

Since the DIBL factor is a better criterion for determining $L_{\min}$, a constraint equation similar to (1) can be derived from an accurate threshold-voltage model. Based on the simplified two-dimensional threshold-voltage model developed in [4], a new constraint equation is expressed by

$$DIBL \simeq M\frac{T_{ox}}{L}\frac{Y_{DO}}{L}F_D(mY_{DO} + a_{00})\left(\frac{R_j}{L}\right)^n \tag{8a}$$

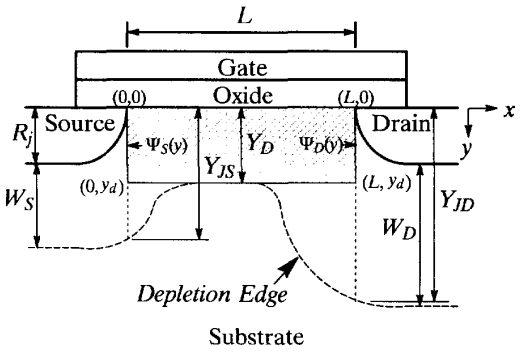


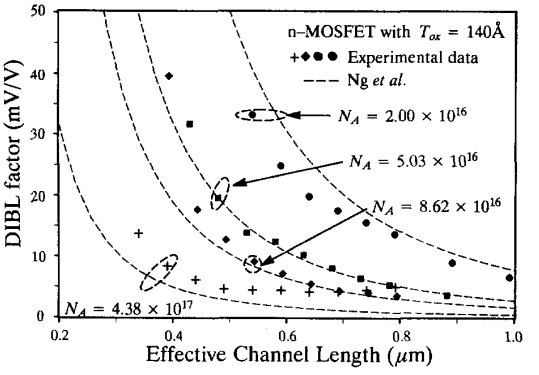
Fig. 1. The cross-section view of a conventional n-MOSFET.

where F_D is the integration result of the drain boundary potential and is given by

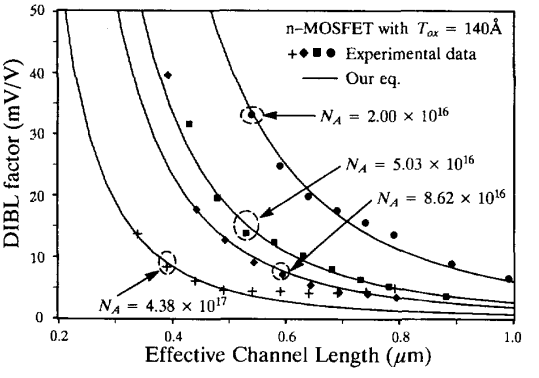
$$F_D \equiv \frac{1}{2} - \frac{1}{3}\frac{Y_{DO}}{Y_{JD}} + \frac{1}{12}\left(\frac{Y_{DO}}{Y_{JD}}\right)^2. \tag{8b}$$

Note that the $DIBL$ in (8) is closely related to the ratios T_{ox}/L, Y_{DO}/L, R_j/L, and Y_{DO}/Y_{JD}. Some similarities can be found between (7) and (8). For example, in (8), n is about 0.8 [4], and hence $DIBL \sim L^{-2.8}$, which is close to the one obtained by Ng *et al.* ($DIBL \sim L^{-2.7}$ in (7)). By the way (8) shows that the effect of R_j on the $DIBL$ is relatively weaker than those of T_{ox} and Y_{DO}, due to the sub-unity power n. Besides, the term a_{00} in (8a) is equivalent to the term n_3 in (7) because they represent the limited resistance to the $DIBL$ effect of the substrate doping concentration. That is, due to the existence of a_{00} and n_3, the $DIBL$ can never be completely eliminated by simply increasing the substrate doping concentration indefinitely. This is attributed to the perpetual charge sharing by the source/drain boundary potentials [4].

However, (7) and (8) still differ each other in other manners. To evaluate their differences, we compare (7) and (8) with the $DIBL$ values extracted from the current-voltage characteristics of a set of experimental test devices. The fabrication details of the test devices have been described in [4]. Note that the experimental test devices are conventional n-MOSFET's, which have different oxide thicknesses and uniform substrate doping concentrations with the source/drain junction depth of approximate $0.2\,\mu$m. For consistency, the definition of the $DIBL$ values follows that used by Ng *et al.* [3]. That is, the threshold voltages at V_{DS} ranging from 1–3 V are used. The normalized-current method [4] is used to determine the threshold voltages at various V_{DS}. The junction-related quantities (e.g., W_D and Y_{JD}) are calculated at $V_{DS} = 2$ V. In Figs. 2 and 3, the extracted $DIBL$ values (marks) and the calculated results using (7) (dashed curves) and (8) (solid curves) are plotted for comparisons. Fig. 2 illustrates the cases with different N_A's, in which N_A is extracted from the substrate sensitivity of the threshold voltage from a large device ($W/L = 150/100$). As mentioned previously, the validity of (7) is confined in the neighborhood of the center device, and any arbitrary extension cannot guarantee the accuracy of (7). It is clearly seen that the accuracy of (7)



(a)



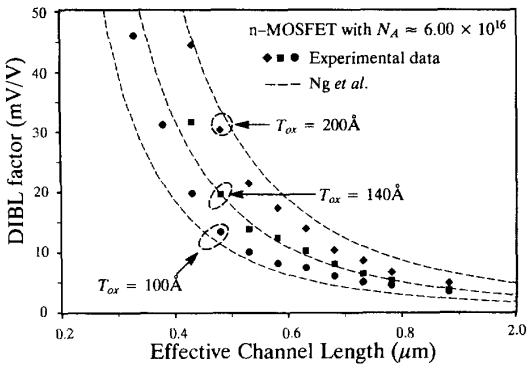
(b)

Fig. 2. Comparisons between the measured (● ■ ♦ +) drain-induced barrier lowering (DIBL) factors and the ones calculated by the constraint equations proposed by (a) Ng *et al.* [3] (— — —) and (b) Maa *et al.* [4] (———) with different N_A's and $T_{ox} = 14$ nm.

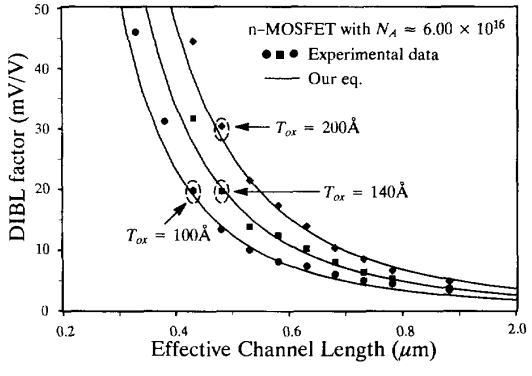
is relatively poor, especially in the range far away from the center device selected in [3] (i.e., $N_A \leq 10^{17}/\text{cm}^3$). Similar observation can be obtained from Fig. 3 for the dependence of the $DIBL$ on T_{ox}. On the other hand, the agreements between (8) and measurement results are excellent, and larger deviations can be noted as $DIBL \geq 20$ mV/V. Numerical simulations also show the same departure boundary [4], and this can be easily realized by recalling the assumptions made in deriving (8) [4]. In (8), the one-dimensional depletion depth Y_{DO} is used, and the two-dimensional effects causing the depletion depth broadening are neglected. This implies that (8) describes the threshold behavior before any strong two-dimensional effect becomes significant. Then, $DIBL \leq 20$ mV/V can be adopted to be the limiting criterion for determining $L_{\min}$. Actually, in [4], the criterion is $DIBL = 20$ mV/V, rather than 10 mV/V defined by Ng *et al.* [3].

III. The New Scaling Theory

The CONFIST is meant to maintain the same field configurations after device scaling. In the original theory proposed by Baccarani *et al.* [1], the Poisson equation and the current continuity equations were decoupled since only the subthreshold region was taken into consideration. The success of the CONFIST must be verified by the field-



(a)



(b)

Fig. 3. Comparisons between the measured (● ■ ♦) drain-induced barrier lowering (DIBL) factors and the ones calculated by the constraint equations proposed by (a) Ng *et al.* [3] (— — —) and (b) Maa *et al.* [4] (———) with different T_{ox}'s and $N_A \approx 6 \times 10^{16}/\text{cm}^3$.

dependent device characteristics. In the subthreshold region, the most important field-dependent characteristics are due to the punchthrough and DIBL effects. Generally, punchthrough is a more complicated phenomenon and is not desired under normal operation. Therefore, the DIBL effect is taken to be the major benchmark for evaluating the merits of the CONFIST. In principle, if the field configuration is indeed kept unchanged in the scaled devices, the DIBL values must remain constant. Our analyses are based on the argument: The invariance of the DIBL value is the essential condition of the CONFIST.

From the above interpretations, the original CONFIST proposed in [1], which is denoted by CONFIST-1 for convenience, is evaluated. Starting with the Poisson equation, Baccarani *et al.* [1] recognized the three degrees of freedom for scaling: dimensions, potentials, and doping concentrations. In the CONFIST-1, all the dimensions are scaled by a unique factor λ, and the potentials can be scaled by another independent factor κ. The power supply and the threshold voltage are scaled by κ simultaneously. Basically, λ and κ can be artifically assigned. The left one for doping, δ, is automatically detemined by requiring the invariance of the Poisson equation after scaling. $\delta = \lambda^2/\kappa$ was obtained in [1].

For clear distinction in the following paragraphs, the related notations are written in upper and lower case before and after scaling, respectively. For example, the channel length L and the threshold voltage V_{TH} become l and v_{th} after scaling, respectively.

The factor R_1 is defined to be the ratio of the $DIBL$ value after scaling to the one before, i.e.,

$$R_1 \equiv \frac{dibl}{DIBL}. \tag{9}$$

Then, $R_1 = 1$ is required by the CONFIST-1. After scaling (8), we have

$$dibl = M\frac{T_{ox}}{L}\frac{y_{do}}{l} f_d\,(my_{do} + a_{00})\left(\frac{R_j}{L}\right)^n \tag{10a}$$

where $l = L/\lambda$, $y_{do} = Y_{DO}/\lambda_d$ and

$$f_d \equiv \frac{1}{2} - \frac{1}{3}\frac{y_{do}}{y_{jd}} + \frac{1}{12}\left(\frac{y_{do}}{y_{jd}}\right)^2. \tag{10b}$$

λ_d can be found to be

$$\lambda_d = \frac{\lambda}{\sqrt{\kappa}} \times \frac{1}{1 + \ln(\lambda^2/\kappa)\phi_t/\phi_{sinv}}. \tag{11}$$

Substitution of (8) and (10) into (9) yields

$$R_1 = \frac{\lambda}{\lambda_d} \times \frac{f_d}{F_D} \times \frac{mY_{DO}/\lambda_d + a_{00}}{(mY_{DO} + a_{00})}. \tag{12}$$

Note that κ can be found by solving (12) with $R_1 = 1$ for a given value of λ. Fig. 4 shows the behavior of κ for continuous scaling. The curve in Fig. 4 is obtained by scaling a 1 μm device down to the submicrometer range. The device parameters before scaling are $T_{ox} = 25$ nm, $R_j = 0.25$ μm, and $N_A = 4.4 \times 10^{16}/\text{cm}^3$, which are typical for 1 μm technology. Some important features are revealed by Fig. 4. It is noted that the variation range of κ is much smaller than that of λ. Besides, the growth rate of κ with λ decreases rapidly as λ increases. This is used to account for the variation of the boundary ratio Y_{DO}/L of the shaded rectangle in Fig. 1 after scaling. According to (11), the reduction of the channel length is not proportional to that of the depletion depth, i.e., $y_{do}/l > Y_{DO}/L$ because $\lambda_d < \lambda$. The insert of Fig. 4 shows the shrinkage tendencies of l and y_{do}, and y_{do} is more persistent than l. It can be understood by an alternative viewpoint: As the channel length is scaled down, the depletion depth is, at first, scaled by λ, too; however, it will be enlarged subsequently by a pseudo-substrate voltage. The increase of the boundary ratio y_{do}/l after scaling is therefore called the *quasi-body effect.* It must be emphasized that the quasi-body effect is not a special result of our example. As long as scaling is executed (i.e., $\lambda > 1$ and $\kappa > 1$), the quasi-body effect is inevitable. Careful examination on the CONFIST-1 indicates that the quasi-body effect is mainly caused by the requirement of unchanged Poisson equation after scaling. Relatively, it results in longer boundaries at the source/drain ends and thus more serious charge sharing and the two-dimensional effects become stronger eventually. To meet the requirement of $R_1 = 1$, the value of κ must be kept small and this is equivalent to the necessity of higher N_A to guarantee $dibl = DIBL$.

The by-product of the quasi-body effect is the weak scalability of the threshold voltage. The values of κ in Fig. 4 are

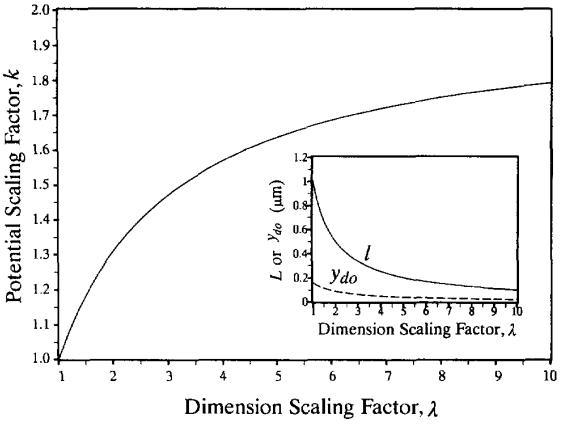


Fig. 4. The variations of the potential scaling factor (κ) with the dimension one (λ) generated by the CONFIST-1. The insert shows the shrinkage tendency of the channel length (l) and the depletion depth (y_{do}). The structures of the referenced device are $L = 1\ \mu$m, $N_A = 4.4 \times 10^{16}/\text{cm}^3$, $T_{ox} = 250$ Å, and $R_j = 0.25\ \mu$m.

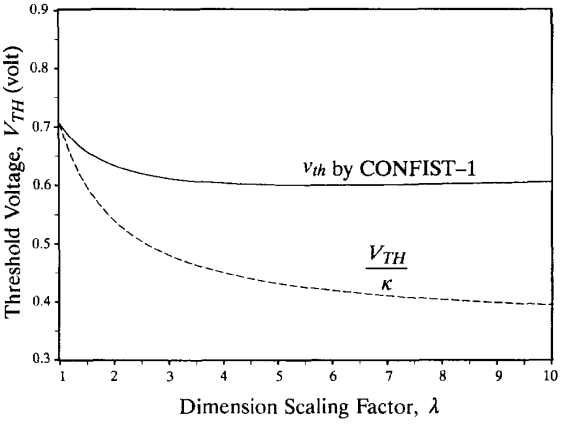


Fig. 5. The scaling behaviors of the expected threshold voltage (— — —) and the one generated by the CONFIST-1 (———). The referenced device is identical to the one used in Fig. 4.

obtained by assigning $R_1 = 1$. The quasi-body effect leads to the necessity of higher N_A. In the long run, the scaling of the threshold voltage will be sacrificed. This can be clearly seen from Fig. 5, where the v_{th} generated by the CONFIST-1 (the solid curve) and the one expected by V_{TH}/κ (the dashed curve) are plotted together. The CONFIST-1 always overestimates the scaled threshold voltage, and v_{th} is nearly too persistent to be scaled any further as the 1 μm device is scaled down to the level below 0.25 μm (i.e., $\lambda \geq 4$). The deviation of v_{th} from V_{TH}/κ is larger than 0.1 V below the level. Since so, the CONFIST-1 can never be categorized to be a successful miniaturization rule.

In summary, the scaling issues of the CONFIST-1 are

1) to find the scaling factor for all dimensions, λ,
2) to find the scaling factor for potentials, κ, and
3) to find the scaling factor for doping concentrations, δ, under the following given requirements:
   A) an artificially defined λ, depending on the goal of scaling (i.e., $\lambda = L/l$);
   B) scaled power supply and threshold voltage by κ (i.e., $v_{th} = V_{TH}/\kappa$);
   C) invariant Poisson equation (i.e., $\delta = \lambda^2/\kappa$); and
   D) unchanged field configuration (i.e., $R_1 = 1$).

According to the above discussion, ⟨1⟩ and ⟨3⟩ are satisfied by ⟨A⟩ and ⟨C⟩, respectively. Eventually, the goal ⟨2⟩ has to meet the requirements ⟨B⟩ and ⟨D⟩ simultaneously and it is mathematically impossible. Physically speaking, the CONFIST-1 is defeated by the inevitable quasi-body effect.

After the mathematical and physical mechanisms causing the limitations of the CONFIST-1 are well understood, a straightforward strategy can be proposed. To satisfy the mathematical self-consistency, the scaling issues of the CONFIST must be accomplished by providing the same number of requirments. Moreover, we have to release the intentional or unintentional restrictions existing in the original CONFIST. For simplicity, we concentrate on the problems of two-dimensional scaling. In the subthreshold region, the Poisson equation is

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_s}. \tag{13}$$

Obviously, the more generalized degrees of freedom for scaling are the lateral dimensions (i.e., the x-related terms, such as L), the vertical dimensions (i.e., the y-related terms, such as T_{ox} and R_j), the potentials (i.e., power supply and threshold voltage), and the doping concentrations (i.e., N_A). Concerning the basic requirements of the CONFIST the invariance of the Poisson equation must be abandomed in order to prevent the scaling from being constrained by the quasi-body effect. Then, the scaling factor δ for doping concentration becomes more independent and is not determined completely by λ and κ any more, and the requirement of ⟨C⟩ is removed subsequently. This can be substituted by another one introduced below.

Like R_1, another factor R_2 can be defined to be

$$R_2 \equiv \frac{v_{th}}{V_{TH}/\kappa} \tag{14}$$

where R_2 means the ratio of the scaled threshold voltage (v_{th}) to the expected one (V_{TH}/κ). A self-consistent CONFIST definitely demands $R_2 = 1$.

Again, based on the above discussions for the CONFIST-1, the new scaling strategy, which is designated by the CONFIST-2 for distinction, is summarized as follows:

The scaling issues of the CONFIST-2 are

1) to find the scaling factor for the lateral dimensions, λ,
2) to find the scaling factor for the vertical dimensions, v,
3) to find the scaling factor for the vertical dimensions, κ,
4) to find the scaling factor for the doping concentrations, δ, under the following requirements:
   A) an artifically defined λ, depending on the goal of scaling (i.e., $\lambda = L/l$);
   B) an artificially defined κ;
   C) exact scaling of V_{TH} (i.e., $R_2 = 1$); and
   D) unchanged field configuration (i.e., $R_1 = 1$).

The CONFIST-2 belongs to the CONFIST because the essential condition $R_1 = 1$ is required. However, it is different from the CONFIST-1 mainly in that it allows a more flexible selection of κ. The scaling of the power supply is a more subtle problem. Circuit performance and reliability considerations are crucial to the choice of power supply [5]. Basically, the CONFIST-2 provides independent selections of λ and κ.

To demonstrate the implementation practice of the CONFIST-2, we scale the 1 μm device used in Figs. 4 and 5 again. The scaling functions for λ and κ are assumed to be

$$\lambda = \frac{1}{l} \tag{15}$$

and

$$\kappa = \frac{7}{3} - \frac{4}{3} l. \tag{16}$$

The use of (15) is obvious since the referenced device is designed by the 1 μm technology. Equation (16) comes from the assumption that the power supplies are 5 V and 2.5 V for 1 μm and 0.25 μm devices [5], respectively, and can be linearly scaled with lateral dimensions. The merits of the CONFIST-2 are not assessed by the specific scaling functions for λ and κ. Various functions other than (15) and (16) can be designed without inducing any difficulty in the implementation of the CONFIST-2. The major computation efforts are then spent on the determinations of v and δ. To meet the requirements {C} and {D}, the scaling trends for the substrate doping concentration differ oppositely. Fig. 6 illustrates the solution procedure for v and δ. The solid curves represent the variations of δ with v constrained by {C}. Evidently, higher doping concentration is desired for the threshold voltage to reach the expected value as the oxide thickness is reduced. Meanwhile, on the contrary, relatively lower doping is enough to maintain the magnitude of the $DIBL$ with the aids of the shrinkage of oxide thickness, as shown by the dashed curves in Fig. 6. The compromise points for {C} and {D} indicate the optimum combinations of v and δ. Simple algorithms such as the bisection method can be invoked to solve v and δ simultaneously. The solutions of v and δ in our example according to the above approach are plotted in Fig. 7 (triangle marks), in which both the threshold voltage and the $DIBL$ value are calculated by the analytic model developed in [4]. Also shown in Fig. 7 are the results produced by the CONFIST-1 (the dashed curves). The CONFIST-2 recommends lower substrate concentrations than the CONFIST-1 does (as $\delta < \lambda^2/\kappa$). The resulted degradation of the $DIBL$ resistance is remedied by the larger scaling of the vertical dimensions (i.e., T_{ox} and R_j). Another interesting point is that the CONFIST-2 is nearly identical to the CONFIST-1 as $\lambda \leq 2$. It means that the CONFIST-1 is an acceptable miniaturization guide for devices larger than 0.5 μm. Fig. 8 summarizes the scaling guides obtained by the CONFIST-1 (dashed curves) and CONFIST-2 (solid curves). It is shown that the CONFIST-2 clearly separates the weight of each scaling factor. To meet the requirements of the CONFIST, the most scaled degree of freedom must be the vertical dimensions.

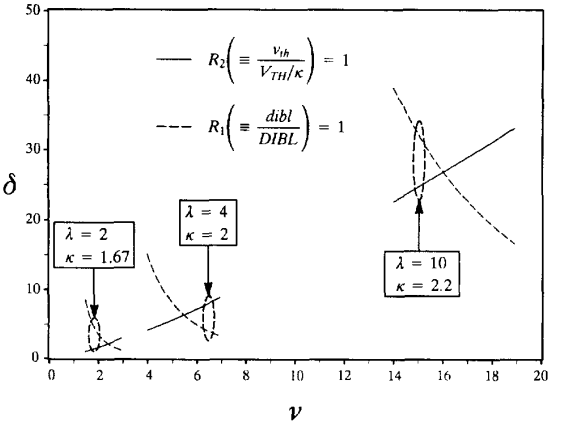


Fig. 6. Illustration of the method to solve the scaling factors for vertical dimensions (v) and doping concentrations (δ).

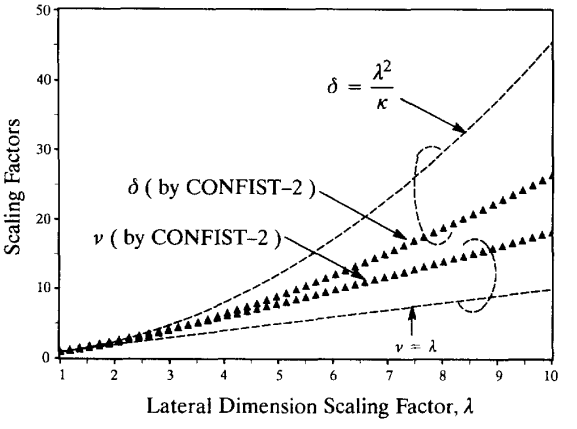


Fig. 7. The scaling factors generated by the CONFIST-1 (———) and CONFIST-2 (▲).

In this work, the constant-field scaling principle of conventional MOSFET's is examined, and the proposed scaling rule can be easily extended to the case of LDD MOSFET devices if the maintenance of constant field after the scaling of LDD MOSFET devices is the only important criterion. However, the channel field is reduced considerably due to the introduction of LDD structure, but the design of high-performance LDD MOS devices will be limited by other consideration such as the effects of the parasitic resistance in the n^--region on the saturation voltage and the drain current. The complicated design algorithm for high-performance LDD MOSFET devices is under investigation and will be addressed in the future publication.

IV. Conclusions

This work has investigated the generalized MOS miniaturization guide proposed by Brews *et al.* in detail. The $DIBL$ effect is selected to be the limiting criterion for determining $L_{\min}$. The mathematical basis of the strategy proposed by Ng *et al.* is found to be the termwise Taylor expansions of the original constraint equation proposed by Brews *et al.* and the

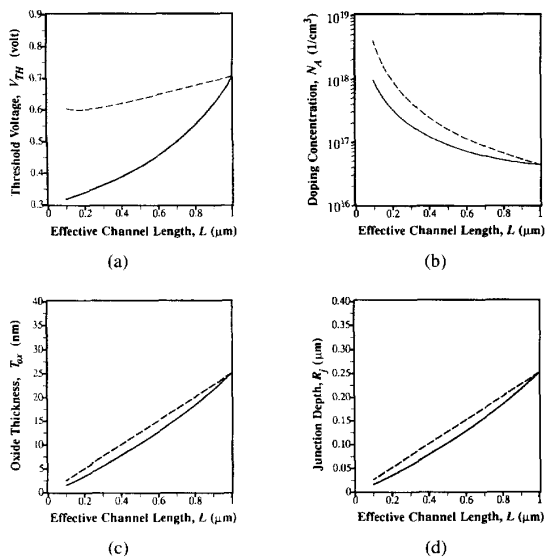


Fig. 8. The scaling trends obtained by the CONFIST-1 (— — —) and CONFIST-2 (——). (a) Threshold voltage. (b) Doping concentration. (c) Oxide thickness. (d) Junction depth.

revised equation proposed by Ng *et al.* is appropriate in a narrow window. The accuracies of various constraint equations are evaluated, and it is concluded that the agreements between the measured $DIBL$ and the proposed new constraint equation are better.

The verified (and qualified) new constraint equation is then utilized to assess a new constant-field scaling theory (CONFIST-2). By scaling the constraint equation, we note that the original CONFIST (CONFIST-1) is limited by the lack of mathematical self-consistency. Due to the inevitable quasi-body effect, the CONFIST-1 results in the weak scalability of the threshold voltage.

According to the two-dimensional Poisson equation, we generalize the degrees of freedom for scaling to be: the lateral dimensions, the verical dimensions, the potentials, and the doping concentration. The solution proposed to modify the CONFIST-1 (i.e., CONFIST-2) overcomes the problem caused by the quasi-body effect. The implementation practice is illustrated and the results show that the CONFIST-1 begins to deviate significantly below 0.5 μm device design. The CONFIST-2 also suggests that the vertical dimensions must be scaled more than the lateral ones.

ACKNOWLEDGMENT

The authors give special thanks to the Electronics Research and Service Organization (ERSO), Industrial Technology Research Institute (ITRI), Taiwan, Republic of China, for the fabrication of the test devices.

REFERENCES

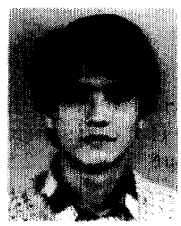
[1] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. ED-31, no. 4, p. 452, 1984.

[2] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, "Generalized guide to MOSFET miniaturization," *IEEE Electron Device Lett.*, vol. EDL-1, no. 1, p. 2, 1980.

[3] K. K. Ng, S. A. Eshraghi, and T. D. Stanik, "An improved generalized guide for MOSFET scaling," *IEEE Trans. Electron Devices*, vol. 40, no. 10, p. 1895, 1993.

[4] J.-J. Maa and C.-Y. Wu, "A new simplified threshold-voltage model for n-MOSFET's with nonuniformly doped substrate and its application to MOSFET's miniaturization," to appear in *IEEE Trans. Electron Devices*, August 1995.

[5] W.-H. Chang, B. Davari, R. Wordeman, Y. Taur, C. C. H. Hsu, and M. D. Rodriguez, "A high performance 0.25 – μm CMOS technology: I-design and characterization," *IEEE Trans. Electron Devices*, vol. 39, no. 4, p. 959, 1992.



Jiin-Jang Maa (S'88) was born in Hsinchu, Taiwan, Republic of China, on January 17, 1966. He received the B.S. degree from the Department of Material Science and Technology, National Tsing Hua University, Taiwan, in 1988. Since 1989, he has been working towards the Ph.D. degree at the Institute of Electronics, National Chiao-Tung University, Taiwan. His present research areas focus on characterization, modeling, and optimization techniques for deep-submicrometer CMOS devices.

Ching-Yuan Wu (M'72) was born in Taiwan, Republic of China, on March 18, 1946. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University, Taiwan, in 1968, and the M.S. and Ph.D. degrees from the State University of New York (SUNY) at Stony Brook, in 1970 and 1972, respectively.

During the 1972-1973 academic year, he was appointed as a Lecturer at the Department of Electrical Sciences, SUNY-Stony Brook. During the 1973-1975 academic years, he was a Visiting Associated Professor at National Chiao-Tung University (NCTU), Taiwan. In 1976, he became a Full Professor in the Department of Electronics and the Institute of Electronics, NCTU. At NCTU, he had been the Director of Engineering Laboratories and Semiconductor Research Center from 1974 to 1980; the Director of the Institute of Electronics from 1978 to 1984; and the Dean, College of Engineering, from 1984 to 1990. He was a principal investigator of the National Electronics Mass Plan-Semiconductor Devices and Integrated-Circuit Technologies from 1976 to 1979, and had been a Coordinator of the National Microelectronics Researches and High-Level Man-Power Education Committee, National Science Council, Republic of China from 1982 to 1988. He has been the Research Consultant of the Electronics Research and Service Organization (ERSO), ITRI; a member of the Academic Review Committee, the Ministry of Education; and the chairman of the Technical Review Committee on Information and Microelectronics Technologies, the Ministry of Economic Affairs. His research activities have been in semiconductor device physics and modelings, Integrated-circuit designs and Technologies. His present research areas focus on the developments of efficient 2D and 3D simulators for deep-submicrometer semiconductor devices, design rules and optimization techniques for deep-submicrometer CMOS devices, and key technologies for deep-submicrometer CMOS devices. He has published over 180 papers in the semiconductor field and has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES and *Solid-State Electronics*.

Dr. Wu is a member of the Honorary Editorial Advisory Board of *Solid-State Electronics* and is a board member of the Chinese Engineering Society. He received the Academic Research Award in Engineering from the Ministry of Education (MOE) in 1979 and the outstanding Scholar award from the Chinese Educational and Cultural Foundation in 1985. He received the outstanding research Professor fellowship from the Ministry of Education and the National Science Council (NSC), Republic of China, during 1982-1995 and the Distinguished Engineering Professor Medal Award from the Chinese Engineering Society in 1992.