The Performance and Reliability Enhancement of ETOX P-Channel Flash EEPROM Cell with P-Doped Floating-Gate

H. W. Tsai[1], P. Y. Chiang[1], S. S. Chung[1], D. S. Kuo[2], and M. S. Liang[3]
[1]Department of Electronic Engineering, National Chiao Tung University, Taiwa.
[2]Nexflash Inc., San Jose, U.S.A. *[3]Tsmc, Science-based Industrial Park, Hsinchu, Taiwan*

Abstract- In this paper, we proposed a simple approach for designing reliable and high performance p-channel Flash EEPROM cell from the floating-gate engineering point of view. In other words, a p-type doped floating gate used in a p-channel flash cell can achieve this goal. Results show that the programming speed, gate/drain disturb, read lifetime, and data retention in p-type floating-gate cell are much better than those of n-type floating-gate cell; except that p-type floating-gate cell has slower erasing speed. These results can be used as a guideline for designers to choose.

Introduction

In the past, n-channel flash cells [1] were widely used in the design of flash memory products. However, the requirement of high voltage operation for channel-hot-electron (CHE) programming results in a large power consumption. In order to improve it, the p-channel flash cell has been suggested for low voltage and low power applications [2]. A more matured p-channel cell using band-to-band tunneling induced hot electron injection (BBHE) has later been proposed [3]. However, in p-channel flash memory cells, there is a serious problem with the drain disturb [4].

On the other hand, quite few studies have been devoted to the study of floating-gate doping effects on the current-voltage characteristics as well as the program/erase characteristics in flash memories . We found in our previous work [5] that the usage of p-type floating gate in an n-channel flash cell is feasible for the high speed programing/erasing as well as better endurance. As a result, special interest for developing a p-channel cell with better reliability and high performance for this p-doped FG flash memory cell has been the focus of this work.

In this paper, performance and reliability enhancement for p-channel flash cells has been demonstrated. A comprehensive study of n- and p-type floating-gate (FG) in p-channel flash cells with performance and reliability was made. From the results, we will provide sufficient information on how and why the p-type floating-gate in p-channel flash cell can work well for future flash memory applications.

Device Preparation

The devices used in this study are conventional ETOX p-channel flash memory (Fig. 1), fabricated using 0.35μm triple well technology. The test sample has channel length and channel width of 0.6 and 0.7μm respectively. The thickness of the tunnel oxide is 90Å. The floating-gate dopants are split into in-situ doping with Phosphorus (n-type), undoped, medium and high doping with Boron (p-type) as given in Table 1. The test samples have gate length of 0.7μm, tunnel oxide thickness of 90Å, an equivalent interpoly dielectric thickness of 165Å, and a control-gate coupling coefficient of 0.63. In order to increase the gate coupling coefficient, the floating-gate is extended into the Local Oxidation of Silicon (LOCOS) region for enhancing the fringing capacitance between the control-gate and the floating-gate. Major device parameters are summarized in Table 1. In addition, the dummy cells with connected floating- and control-gates, are also used for cell performance and reliability measurements.

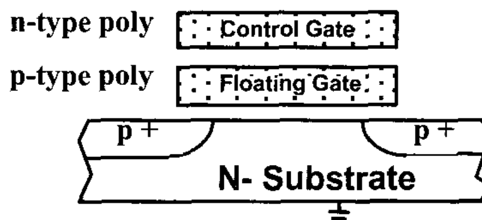

Fig. 1 A cross sectional view of a p-channel and p-type floating gate(FG) flash cell.

	U	P-	P+	N+
T_{ox}(Å)	90			
T_{ono}(Å)	T.O/Si_3N_4/B.O=65/90/55			
Floating Gate Doping	Undoped	BF_2 20KeV 1E13	BF_2 20KeV 5E13	In-situ

Table 1 The split table of stacked gate p-channel flash memory cells used in this study.

Results and Discussion

A. Comparison of the ONO Electric Fields

Figure 2 shows the I_{DS}-V_{GS} characteristics for dummy cells and flash memory cells. The dummy cells with different doping types of floating gates show a significant difference in V_{th} due to the flat-band voltage difference. However, for the flash memory cell, the device V_{th} is independent of the dopant type of the floating gate. Since the cells with different

0-7803-7765-6/03/$17.00 ©2003 IEEE.

floating gate doping type have identical drain currents, the flat-band voltage shift of dummy cells can be neglected. To verify the electric field across the ONO dielectric, theoretical derivations have been given in Table 2. Where V's, Ψ's, ϕ's represent the applied voltages, electrostatics potentials, and the flat-band voltages, respectively. C_{CG},C_S,C_D, and C_B are the capacitances between the floating-gate and control-gate, source, drain, and substrate regions, respectively. By comparing Eqs. (3) and (4), since $V_{FG}(p) > V_{FG}(n)$ as a result of the band bending, electrical field of the tunnel oxide for n-FG is smaller than that of p-FG. So, for a constant field between gate and the substrate, ONO field in p-FG cell is larger than that of n-FG cell.

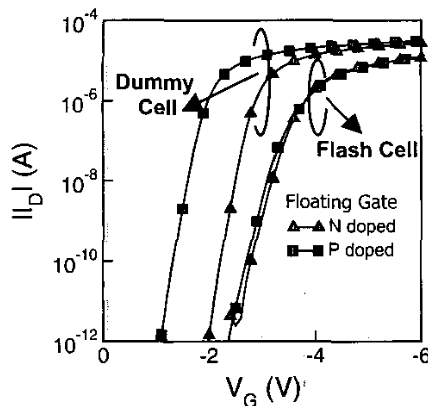

Fig. 2 Measured drain current characteristics for both dummy and p-channel flash cells with n-doped or p-doped floating gate.

$$Q_{FG} = C_{CG}(\Psi_{FG} - \Psi_{CG}) + C_S(\Psi_{FG} - \Psi_S) + C_D(\Psi_{FG} - \Psi_D) + C_B(\Psi_{FG} - \Psi_B) \quad (1)$$

$$\Psi_{FG} = \frac{C_{CG}}{C_{TOT}}\Psi_{CG} + \frac{C_S}{C_{TOT}}\Psi_S + \frac{C_D}{C_{TOT}}\Psi_D + \frac{C_B}{C_{TOT}}\Psi_B + \frac{Q_{FG}}{C_{TOT}} \quad (2)$$

For n-type floating-gate :

$$V_{FG} + \psi_{FG} = \alpha_{CG}(V_{CG} + \psi_{CG}) + \alpha_D(V_D - \psi_D) + \frac{Q_{FG}}{C_{TOT}} + \alpha_S\Psi_S + \alpha_B\Psi_B \quad (3)$$

For p-type floating-gate :

$$V_{FG} - \Psi_{FG} = \alpha_{CG}(V_{CG} + \psi_{CG}) + \alpha_D(V_D - \psi_D) + \frac{Q_{FG}}{C_{TOT}} + \alpha_S\Psi_S + \alpha_B\Psi_B \quad (4)$$

So $V_{FG(n)} < V_{FG(p)}$ (always)

During Programming $\Rightarrow$ $V_{TO(n)} < V_{TO(p)}, V_{ONO(n)} > V_{ONO(p)}$

During erase $\Rightarrow$ $V_{TO(n)} > V_{TO(p)}, V_{ONO(n)} < V_{ONO(p)}$

Table 2 Equations used to compare the oxide fields for both n-type and p-type floating gate p-channel flash cells.

B. Programming/Erasing Characteristics

In this work, the programming and erase in p-channel flash memory cells with different floating-gate materials are performed respectively by BBHE, and channel Fowler-Nordheim tunneling (CFN), respectively.

Figures 3(a) and (b) show the comparison of the programming and erase characteristics between various floating-gate cells, respectively. Obviously, the p-type floating-gate cell has faster programming speed and the n-type floating-gate cell has the fastest erasing speed. In short, p-type cell shows a fastest programming speed but a slowest erasing speed except the p^- doped cell. This can be also explained from the band diagram given in Figs. 4(a) and (b). Since the n-type floating-gate potential is always more negative than the p-type one, the tunnel oxide field of p-type floating-gate cell is larger than the n-type one during programming to enhance the programming speed.

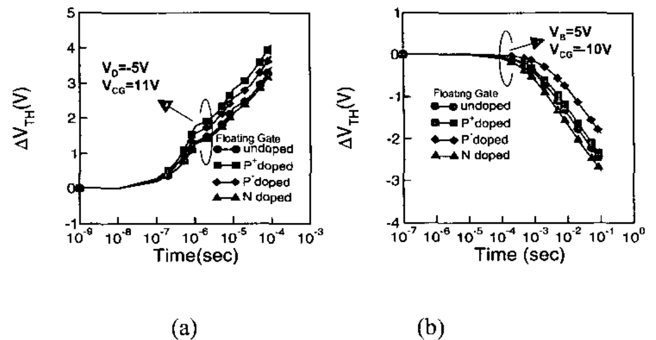

Fig. 3 (a) The comparison of the programming characteristics for flash cells with different dopant types in the floating gate.
(b) The comparison of the erasing characteristics for flash cells with different dopant types in the floating gate.

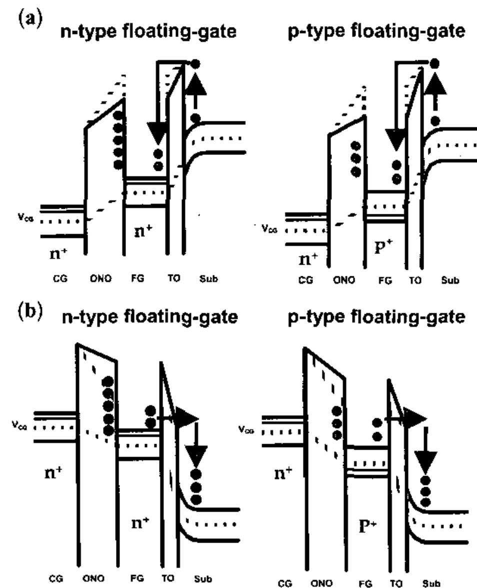

Fig. 4 (a) The energy band diagram for n-type and p-type floating gate p-channel flash memory cells during programming. (b) The energy band diagram for n-type and p-type floating gate p-channel flash memory cells during erase.

On the other hand, the n-type floating-gate cell has larger tunnel oxide electric field during erase such that it has a larger erasing speed. The p^- doped cell is a special case as a

result of the poly-depletion effect [6], in which the p^- doped cell has lower electric field and hence will decrease the erasing speed.

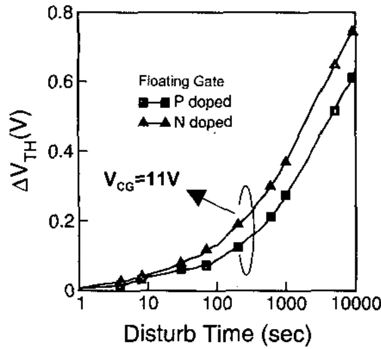

Fig. 5 The gate disturb characteristics for n- and p-type floating gate flash cells after 10^4 P/E cycles.

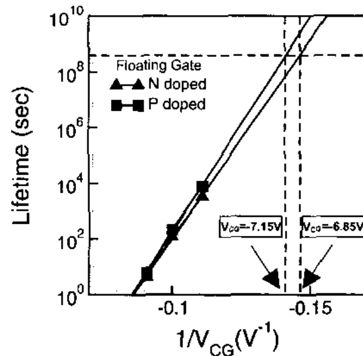

Fig. 6 The read disturb lifetime characteristics for n- and p-type floating gate flash memory cells. The control gate voltage for 10 year lifetime in p-type floating gate cell is larger than that of n-type ones.

C. Gate-disturb, Read-disturb, Drain-disturb

Figure 5 shows the gate disturb characteristics of n- and p-type cells after 10^4 P/E cycles. It was found that p-type floating-gate in p-channel flash cell has better gate disturb characteristic. It is well known that the disturb failure is mainly due to the P/E-stress induced excess oxide leakage current (SILC). Therefore, the p-type floating-gate flash cell has less oxide damage generated during the P/E cycles. According to the worst case for read-disturb time is of the same order of magnitude as that of the device lifetime. Using a threshold voltage shift of $-3.3V \times 10\%=-0.33$ V as our criterion, the read retention characteristics of the p-channel flash cell is shown in Fig. 6, from which we can see that the control gate voltage for 10 year life time is limited to less than −6.85 V and −7.15 V for n-type and p-type FG cells, respectively.

Although the p-channel flash cell has many advantages from the above results, it suffers a severe drain disturb at the high state. The ΔV_{TH} versus bit line stress time is shown in Fig. 7. As we can see that the p-type floating-gate has three-order improvement. Fig. 8 shows the gate currents for different floating-gate. Obviously, when the cell is disturbed by channel-hot-hole induced hot electron injection (CHH), the n-type one has larger areas than the p-type one. This can explain why the p-type one has better drain disturb characteristics. So, if the program scheme is CHH, the programming speed in n-type floating-gate cell might be faster than the p-type one.

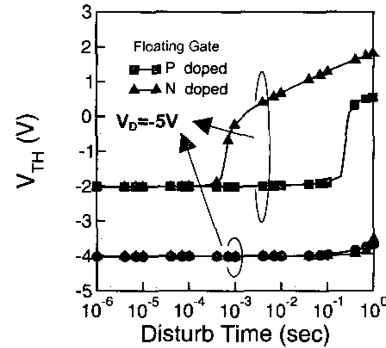

Fig. 7 The drain disturb lifetime characteristics for n- and p-type floating gate flash memory cells after 10^4 P/E cycles. The p-type floating gate cell has 3-order improvement.

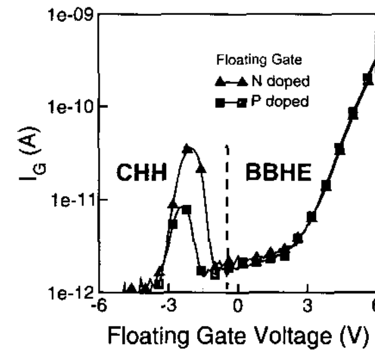

Fig. 8 The gate current characteristics of p-channel flash cells with n- and p-type floating gate. The p-type FG cell has less gate current injection during CHH injection.

D. Endurance and Data Retention

Figure 9 shows the endurance characteristics of both n- and p-type floating-gate p-channel flash cells after program/erase(P/E) cycling. Obviously, the endurance characteristics for both of them are similar.

Figures 10 and 11 show the charge loss characteristics with different floating-gate types memory cells before and after P/E cycling operations, at a baking temperature of 250

°C. Programming and erase operations are performed by BBHE and channel FN tunneling respectively. Obviously, The p-type one has better charge loss behavior at the same situation. Because when the flash memory cell was programmed to the high state, the electric field at tunnel oxide and the ONO layer in n-type floating-gate cell is larger than the p-type one. The electric field will enhance the charge loss behavior in a fresh cell since for the gate disturb characteristics as we have shown before, p-type floating-gate has superior disturb behavior, and less defects and traps occurred during P/E cycling. It is expected that p-type one has better extrinsic charge loss characteristics. Results also show that the charge loss difference between n- and p-type floating gate cells become larger with increasing P/E cycles.

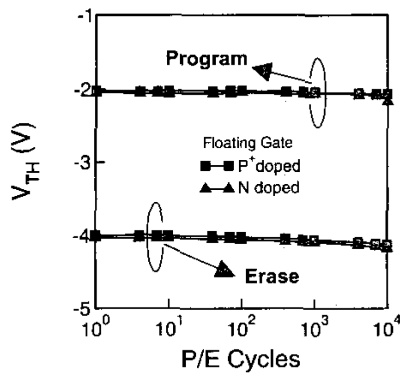

Fig. 9 The endurance characteristics of n- and p-type floating gate p-channel flash cells. Both characteristics are similar.

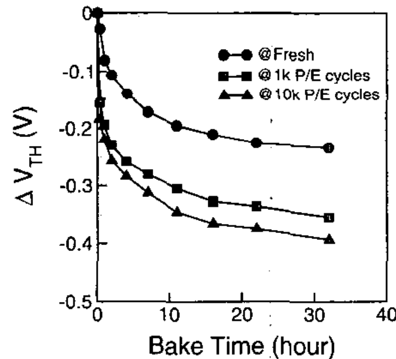

Fig. 10 Charge loss characteristics of n-type floating gate cell before and after P/E cycling at 250°C.

Summary

In summary, we provide a complete evaluation of reliabilities in n- and p-type floating-gate p-channel flash memory cells. The p-type floating-gate flash cell has much lower electric field in the ONO dielectric layer by comparing with that of conventional n-type floating-gate during programming. Therefore, fewer electrons will be injected into the ONO dielectric. This is the reason why p-type FG has much better data retention characteristics than that of n-type FG cell.

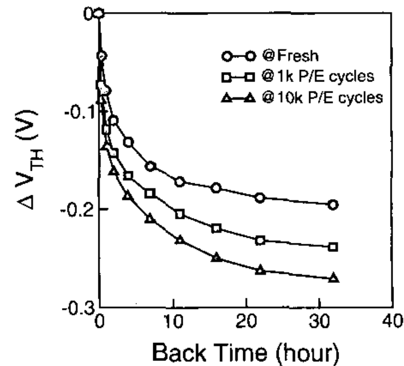

Fig. 11 The charge loss characteristics of p-type floating gate cells before and after the P/E cycling at 250°C.

In comparison, the p-type floating-gate cell has faster programming speed, but a slower erasing speed. However, the p-type floating-gate cell has much better reliabilities than those of n-type cell, in particular it features less gate disturb, larger lifetime tolerance voltage, three-order improvement in drain disturb, and better data retention characteristics etc. Therefore, the p-channel flash cell with appropriate floating gate materials is expected to be a promising candidate for improving the p-channel cell performance and reliability.

Characteristics \ Floating-gate	N-type	P-type
Program Speed	Slower	Faster
Erase Speed	Faster	Slower
Endurance	Similar	Similar
Gate Disturb	Worse	Better
Read Lifetime Voltage	Smaller	Larger
Drain Disturb	Worse	Better
Data Retention	Worse	Better

Acknowledgments This work was supported by the National Science Council, Taiwan, R.O.C. under contracts NSC87-2215-E009-051 and NSC88-2215-E009-040.

References

[1] H. Kume et al., in *IEDM Tech. Dig.*, p. 560, 1987.
[2] C. C. -H. Hsu et al., *Extended Abs. SSDM*, p. 140, 1992.
[3] T. Ohnakado et al., in *IEDM Tech. Dig.*, p. 279, 1995.
[4] S. S. Chung et al., in *Proc. IRPS*, p. 67, 2001.
[5] S. S. Chung et al., in *Symp. VLSI Tech.*, p. 19, 1999.
[6] A. Gupta et al., *IEEE EDL*, p. 580, 1997.