$La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs and Ni Germano-Silicide

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Abstract **— We have used $Si_{0.3}Ge_{0.7}$ to improve the hole mobility of La_2O_3 p-MOSFETs. A hole mobility of 55 cm^2/V-s in nitrided $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET is measured and 1.8 times higher than the 31 cm^2/V-s mobility in nitrided La_2O_3/Si control p-MOSFET. The Ni germano-silicide shows a low sheet resistance of 4-6 Ω/□ and small junction leakage currents of 3×10^{-8} A/cm^2 and 2×10^{-7} A/cm^2 for respective P^+N and N^+P junctions.**

I. INTRODUCTION

High-k gate dielectrics [1]-[5] have attracted much attention for possibly replacing SiON because of the lower gate leakage current, but the much poor mobility and small process window in high-k MOSFET is a still difficult challenge. The poor mobility is the main issue for advanced device design that may reduce the required high on-state drive current (I_{ON}). The mobility degradation in p-MOSFET is especially an important concern because the hole effective mass in p-MOSFET is larger than the electron effective mass in n-MOSFET. The mobility degradation is even worse after surface nitridation but the process is needed to preserve a large process window and maintain the small EOT during thermal cycle [2]. It is known that the hole mobility in Ge has nearly the lowest value among known the III-V and group IV semiconductors, therefore mobility improvement is expected for high-k/ SiGe p-MOSFET. However, the conventional UHVCVD grown SiGe has serious problem of the strain relaxation related poor surface, large junction leakage, and degraded device performance after subsequent thermal cycle [6]-[7]. Recently, we have developed a high temperature stable SiGe process using solid-phase epitaxy [8], and good device integrity of high gate oxide quality, small junction leakage, higher hole mobility, and better I_{ON} than Si control devices have been demonstrated [9]-[11]. In this paper, we have used this SiGe technology to improve the device performance of high-k La_2O_3 p-MOSFET. A hole mobility of 55 cm^2/V-s in nitrided $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET that is 1.8 times higher than the 31 cm^2/V-s mobility in nitrided La_2O_3/Si control p-MOSFET. High integrity silicide is another important factor to realize the SiGe MOSFET technology. We have also developed high quality Ni Germano-Silicide on $Si_{0.3}Ge_{0.7}$. The Ni germano-silicide shows a low sheet resistance of 4-6 Ω/□ on both P^+N and N^+P junctions and much lower than Co germano-silicide. Small junction leakage currents of 3×10^{-8} A/cm^2 and 2×10^{-7} A/cm^2 are obtained for Ni germano-silicide on P^+N and N^+P junctions, respectively. The improved mobility and good Ni Germano-Silicide quality are important to realize high-k dielectric integration into VLSI technology.

II. EXPERIMENTAL PROCEDURE

Standard 4-in (100) n- and p-type Si wafers were used in this study. After device isolation, the solid-phase epitaxy of $Si_{0.3}Ge_{0.7}$ is formed by depositing Ge on native oxide free Si surface and rapid thermal annealing at 900 °C. The formed single crystal $Si_{0.3}Ge_{0.7}$ in active region was confirmed by X-Ray Diffraction (XRD), electron diffraction pattern, and cross-sectional TEM [10]. For high-k $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs, the source-drain p^+ region was first formed by implantation followed by a 950 °C RTA. Then La_2O_3 gate oxide of ~60 Å was formed by depositing La and oxidation and measured by ellipsometer. More detailed $Si_{0.3}Ge_{0.7}$ and La_2O_3 characterization can be found in our previous study [4]-[5], [8]-[11]. Next, NH_3 nitridation was performed at ~550°C before gate electrode formation. The p-MOSFETs and MOS capacitors were fabricated using Al as gate electrode and characterized by I-V and C-V measurements. In addition to $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs, La_2O_3/Si control devices were also fabricated as references. For germano-silicide, 10 KeV B^+ or 50 KeV As^+ implantation is performed on the respective n- or p-type $Si_{0.3}Ge_{0.7}$/Si wafers followed by 900-950 °C RTA. Then 10 nm Co or 12 nm Ni was deposited. For Co germano-silicide, the first step silicidation was performed at 500 °C and the second phase transformation was excused at 750 to 1000°C by RTA [8]-[11]. For Ni germano-silicide, only one-step RTA at 350-700 °C was performed. The formed germano-silicide and junction diode were characterized by sheet resistance and leakage current measurements. The structure property of germano-silicide is investigated by cross-sectional TEM.

III. RESULTS AND DISCUSSION

A. $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs:

Fig. 1 shows the XRD and diffraction pattern of SiGe formed by solid phase epitaxy. Single crystalline material quality and composition of $Si_{0.3}Ge_{0.7}$ are confirmed.

We have further characterized the device quality of the formed La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs by C-V measurements shown in Fig. 2. The identical accumulation capacitance with EOT of ~1.6 nm and the same small 10 meV hysteresis measured for both devices indicate that the using SiGe does not have any side effect. The smaller flat band voltage in $La_2O_3/Si_{0.3}Ge_{0.7}$ devices may be due to the smaller energy bandgap, which gives additional flexibility to tune V_T.

Fig. 3 shows J_G-V_G characteristics of both

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$La_2O_3/Si_{0.3}Ge_{0.7}$ and La_2O_3/Si p-MOSFETs, respectively. The almost identical gate current suggests the $Si_{0.3}Ge_{0.7}$ channel has little negative effect as compared with Si case. A leakage current of ~1.5×10^{-4} A/cm^2 at 1V that is 4 orders of magnitude lower than SiO_2 at the same EOT. The same gate current is due to nearly the same work function of Si and SiGe and conduction band difference between La_2O_3 and Si or SiGe.

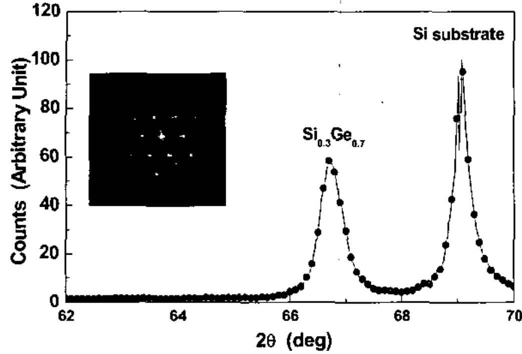

Fig. 1. XRD and electron diffraction patterns of $Si_{0.3}Ge_{0.7}$ after ion implantation and post annealing.

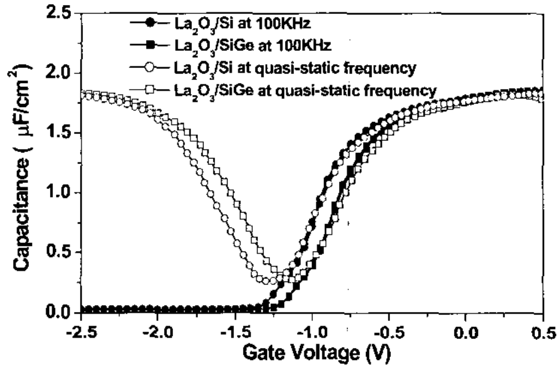

Fig. 2. C-V characteristics of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ MOS capacitors.

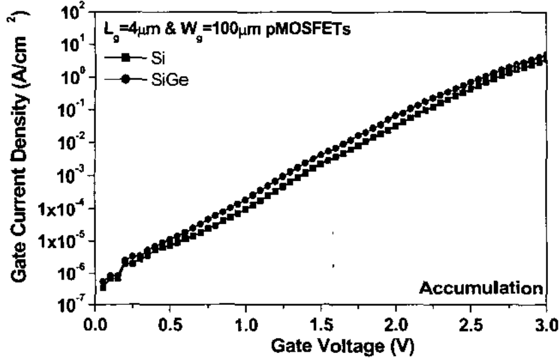

Fig. 3 The gate leakage current of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs under positive gate bias.

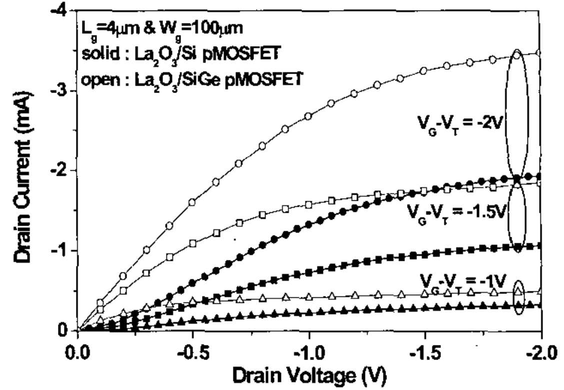

Fig. 4. The I_D-V_D characteristics of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs.

Fig. 4 shows the I_D-V_D characteristics of 4 μm La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs plotted at the same V_G-V_T. Although a relatively large junction leakage of 1×10^{-7} A/cm^2 is measured. Besides the good device I-V characteristics, the $Si_{0.3}Ge_{0.7}$ has ~2 times higher current driving capability than Si device at the same V_g of -2V. Because the La_2O_3 was formed on Si and $Si_{0.3}Ge_{0.7}$ on the same lot with identical inversion capacitance in Fig. 2, the higher hole current is not due to the different gate dielectric. The significantly higher hole current is especially important for high-speed circuit application, which is the fundamental motivation for continuously scaling down.

Because the improved hole current may come from both higher mobility and threshold voltage (V_T) difference, we have further measured the transfer I_D-V_G characteristics. Fig. 5 show the I_D-V_G and hole effective mobility for both La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs respectively, where the V_T difference is also included for the mobility extraction shown in Fig. 6.

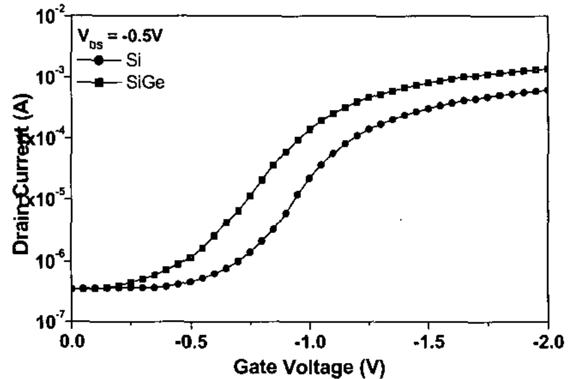

Fig. 5. The I_D-V_G characteristics of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs. The same I_{OFF} suggests no leakage degradation but with significantly higher I_{ON}.

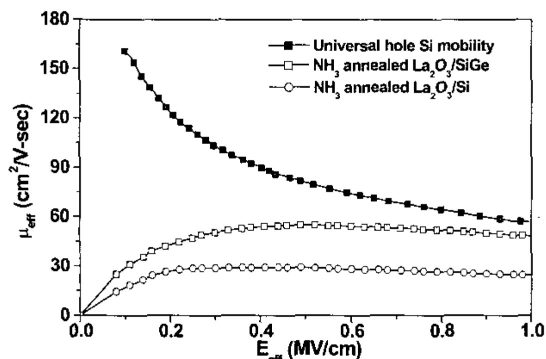

Fig. 6. The hole mobility of La_2O_3/Si and $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs.

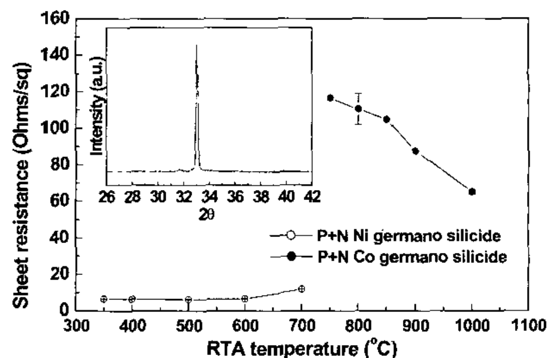

Fig. 7. Sheet resistance comparison of Co and Ni germano-silicide on P+N $Si_{0.3}Ge_{0.7}/Si$.

In additional to the higher saturation hole current than La2O3/Si devices, the $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs have the same off-state current (I_{OFF}) and lower V_T. The lower V_T in $La_2O_3/Si_{0.3}Ge_{0.7}$ device is due to smaller energy bandgap in $Si_{0.3}Ge_{0.7}$. Besides the small V_T difference of 0.2 V, the large hole current improvement is primary coming from the higher mobility using $Si_{0.3}Ge_{0.7}$. A peak hole mobility of 31 cm^2/V-s is obtained in nitrided La_2O_3/Si p-MOSFET that is comparable with nitrided HfO_2/Si [2]. In sharp contrast, the $La_2O_3/Si_{0.3}Ge_{0.7}$ device shown in Fig. 6 has a higher hole mobility of 55 cm^2/V-s that is 1.8 times higher than the La_2O_3/Si control devices without using SiGe. In additional to the comparable gate oxide integrity and I_{OFF}, the higher mobility and I_{ON} indicate the superior device performance can be realized in nitrided high-k La_2O_3 p-MOSFETs using solid-phase epitaxy formed SiGe.

B. Ni germano-silicide:

Figs. 7 and 8 show the sheet resistance of Ni and Co germano-silicide on N+P and P+N $Si_{0.3}Ge_{0.7}/Si$ junctions, respectively. The Ni germano-silicide exhibits superior sheet resistance than Co germano-silicide, and low sheet resistance of 6Ω/□ and 4Ω/□ are achieved on respective P+N and N+P junctions. From the XRD pattern inserted in Fig. 7, the formed phase is mono-germano-silicide that is the reason to achieve such low sheet resistance. The obtained low sheet resistance from 400 to 600 °C suggests Ni germano-silicide have good thermal stability and large process margin over this temperature range. We have used cross-sectional TEM to study the structure property of formed germano-silicide. Figs. 9 and 10 show the Ni and Co germano-silicide formed at 500 and 900 °C on N+/P $Si_{0.3}Ge_{0.7}/Si$ junction, respectively. A relatively uniform thickness and smooth surface of Ni germano-silicide is observed, which explains the measured good sheet resistance shown previously in Fig. 8. In contrast, much rougher thickness and strong agglomeration are observed in Co germano-silicide that gives the higher sheet resistance.

We have further studied the junction characteristics of Ni germano-silicide. Figs. 11 and 12 show the junction

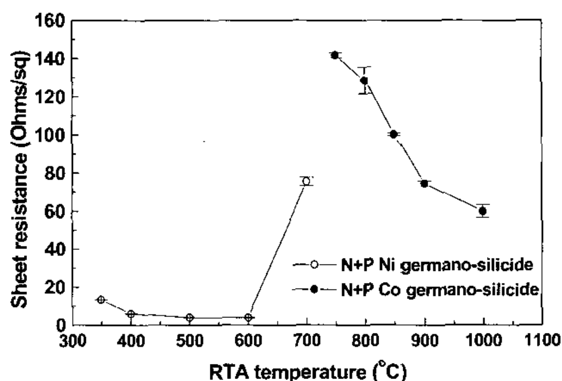

Fig. 8. Sheet resistance comparison of Co and Ni germano-silicide on N+P.

Fig. 9. Cross-sectional TEM of Co germano-silicide on N+P $Si_{0.3}Ge_{0.7}/Si$.

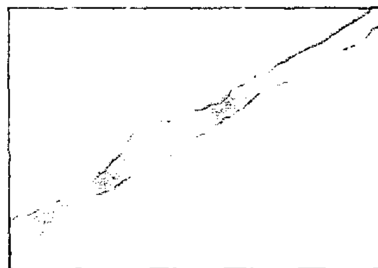

Fig. 10. Cross-sectional TEM of Ni germano-silicide on N+P Si0.3Ge0.7/Si

leakage current of Ni germano-silicide on P^+N and N^+P $Si_{0.3}Ge_{0.7}$/Si junctions, respectively. The possible reason may be due to the required higher silicidation temperature used for Co germano-silicide. The leakage current of P^+N Ni germano-silicide junction decreases as silicidation temperature increasing from 300 to 500 °C, and a minimum leakage current of $<3\times10^{-8}$ A/cm^2 is obtained at 500 °C formation temperature.

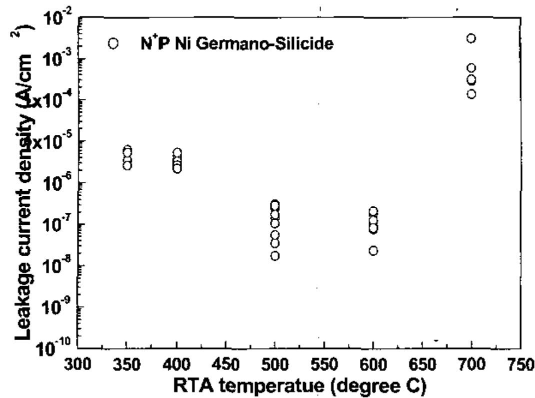

Fig. 11. Junction leakage current of Ni germano-silicide on N^+P $Si_{0.3}Ge_{0.7}$/Si.

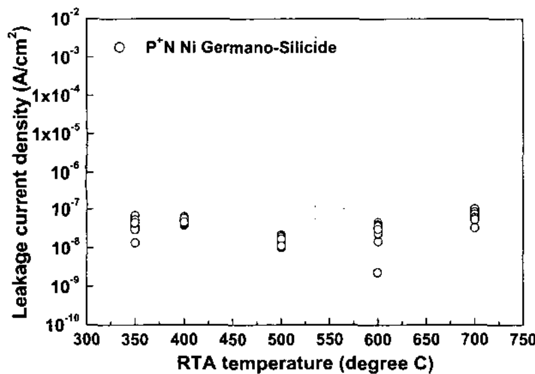

Fig. 12. Junction leakage current of Ni germano-silicide on P^+N $Si_{0.3}Ge_{0.7}$/Si.

Slightly raise of leakage current was then found with the increasing silicidation temperature. The leakage current of N^+P Ni germano-silicide junction shows the similar trend of temperature dependence to P^+N junction, but a slightly higher minimum leakage current of $<2\times10^{-7}$ A/cm^2 is obtained at 600°C. The drastically increase of leakage current at 700 °C may be due to the strong agglomeration at higher temperatures, which is also consistent with the rapid increasing sheet resistance at this temperature shown in Fig. 2.

IV. CONCLUSION

We have achieved ~2 times higher I_{ON} and high hole mobility of 55 cm^2/V-s in nitrided $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFETs with almost identical gate oxide leakage current, capacitance density and I_{OFF}. For SiGe MOSFET integration, Ni germano-silicide shows low sheet resistance of 4-6 Ω/□ is obtained on both P^+N and N^+P $Si_{0.3}Ge_{0.7}$/Si, and small junction leakage currents of $<3\times10^{-8}$ and 2×10^{-7} A/cm^2 are measured on respective junctions. The improved hole mobility in $La_2O_3/Si_{0.3}Ge_{0.7}$ p-MOSFET and high quality Ni germano-silicide give another step to realize high-k gate dielectrics for VLSI integration.

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