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Improved Lower Electrode Oxidation of High-κ TiCeO Metal-Insulator-Metal Capacitors by Using a Novel Plasma Treatment

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We have fabricated high-κ Ir/TiCeO/TaN metal-insulator-metal (MIM) capacitors using a dual plasma treatment on bottom electrode. The novel plasma treatment suppresses the growth of bottom interfacial layer to reduce the degradation of capacitor performance under 400°C PDA. A low leakage current of 1.7×10^{-7} A/cm^2 at -1 V and capacitance density of ~18 fF/μm^2 at 1 MHz were obtained for 21 nm thick TiCeO MIM devices; moreover, a 37 nm thick TiCeO film has a capacitance density of 11 fF/μm^2, which gives a κ value of 45. Consequently, the excellent device performance is due to the combined effects of the dual plasma treatment, high-κ TiCeO dielectric and a high work-function Ir metal.

Introduction

There is a continuing demand to increase the capacitance density ($\varepsilon_0\kappa/t_\kappa$) of the Metal-Insulator-Metal (MIM) capacitors (1)-(13). To achieve this, the MIM devices have evolved by using high κ dielectrics such as SiN (1)-(2), Al_2O_3 (3)-(4), Ta_2O_5 (5), HfO_2 (6)-(8), Nb_2O_5 (9). Titanium oxide (TiO_2) is an attractive material, which has a higher dielectric constant (κ ~50-80) depending on the crystal phase. However, a small band gap, conduction band offset (ΔE_C) and poor thermal stability will lead to a large leakage current and unwanted interfacial layer. In order to improve these issues, TiO_2-based dielectrics with a wider band gap and larger conduction band offset have been developed, such as TiTaO (10)-(11), TiLaO (12) and TiHfO (13). Although ZrO_2 dielectrics with a dielectric constant of > 40 for 50nm DRAM technology were demonstrated, the Zr-based crystalline ternary oxides still leave some concerns about the film uniformity and device reliability, compared to amorphous dielectrics (14). A low leakage current and small capacitance variation ($\Delta C/C$) dependence of the applied voltage are also necessary for high-density DRAM application, except for the limited thermal budget (>400°C) required for BEOL integration.

The low-κ interfacial layer formed between the dielectric and the bottom electrode after a 400°C-PDA process will degrade the capacitance density and increase the leakage current. Using the NH_3 plasma interface treatment on the bottom electrode to improve the leakage current has been proved (15). This suggests that the NH_3 plasma treatment nitrifies the bottom TaN surface, which suppresses the formation of bottom interfacial layer. Here, we reported a dual plasma treatment on the bottom electrode to suppress the growth of bottom interfacial layer and improve the capacitor performance further.

CeO_2 is one of attractive rare earth metal oxides that has many merits such as a high

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dielectric constant (~26), moderate conduction band offset (~0.75 eV) (16) and high scaling capability. It is worth noting that CeO_2 is partially reduced to Ce_2O_3 due to oxygen deficiency under post deposition annealing (PDA) (17), while the Gibbs free energy of Ce_2O_3 (+105 kcal/mol) (18), larger than that of Ta_2O_5 (-52 kcal/mol) and HfO_2 (+47 kcal/mol), can avoid metal/oxide interdiffusion or chemical reaction caused by oxygen exchange. Although TiTaO capacitors published previously exhibit a good performance, the TiTaO dielectric reacts easily with the bottom electrode to form a thicker interfacial layer due to negative Gibbs free energy of Ta_2O_5.

Here, a high-κ (~45) TiCeO film, which mixed a high-κ TiO_2 and CeO_2 dielectric, combine a high work-function Ir metal (~5.27 eV) as a MIM capacitor has been fabricated. A capacitance density of ~18 fF/μm^2 at 1 MHz and leakage current of 1.7×10^{-7} A/cm^2 at -1 V were measured for a 21 nm thick TiCeO MIM capacitor, respectively. A quadratic voltage coefficient of capacitance (α) of 3192 ppm/V^2 was obtained at 1 MHz, which can also be improved rapidly with a decreased capacitance density (19) used for analog/RF application. The good performance is attributed to the dielectric properties, the high work-function metal and a novel interface plasma treatment.

Experimental Procedure

The high-κ TiCeO MIM capacitors were fabricated on standard Si wafers. To permit VLSI backend integration, the process began with depositing a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then a 50 nm TaN was deposited on a 200 nm Ta layer by PVD and the Ta/TaN bi-layers used as a bottom electrode, where the thick Ta was chosen to reduce the parasitic resistance of the electrode. After patterning the bottom electrode, the TaN surface was given a NH_3 plasma treatment at 100W first to increase the oxidation resistance (5) and then was exposed to an O_2 plasma treatment at 50W before the high-κ deposition and post-deposition annealing. Sequentially, the 21 nm and 37 nm thick $Ti_xCe_{1-x}O$ (x~0.67) films were deposited by PVD, followed by a 400°C PDA in an oxygen ambient to reduce the defects and the leakage current (3). (The TiCeO thickness was later measured by cross-sectional SEM.) Finally, a 20 nm Ir was deposited and patterned to form the top electrode. The cross-sectional Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) were used to identify the thickness of dielectric and the interface of bottom electrode, respectively. A large capacitor size of 180-μm×180-μm was chosen to avoid any variations in dimensions arising from lithography. The fabricated devices were characterized by *C-V* and *J-V* measurement using an HP4156C curve tracer and HP4284A precision LCR meter, respectively.

Results and Discussion

The *C-V* characteristics of Ir/TiO_2/TaN capacitors in Figure 1(a) show a capacitance density of ~15 fF/μm^2 at 100 kHz. However, the capacitance density presents a drop while increasing the applied voltage up to 1V. From the *J-V* characteristics in Figure 1(b), a small leakage current of 1×10^{-7} A/cm^2 at -1 V can be obtained under gate injection condition by using a high-work-function metal Ir as a top electrode. But a large leakage current of ~1.7×10^{-2} A/cm^2 at 1 V was obtained under bottom injection condition, even though the bottom electrode has been treated by a NH_3 plasma. This implies that the

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small band gap of TiO_2 dielectric will lead to a high leakage current, and its poor thermal stability will also lead to a thicker interfacial layer between the high-κ dielectric and the bottom electrode under a thermal budget of 400°C-PDA. As stated above, the both two properties will cause a large degradation of capacitance performance. This is why we mixed TiO_2 with other dielectrics with a wider band gap and good thermal stability.

Since the interfacial layer is a serious problem for the scaled EOT, the nitrified TaN electrode by using NH_3 plasma for the suppression of bottom interfacial layer is not already enough to meet the requirement for sub-1 nm EOT DRAM technology. To improve the effect of interfacial layer growth further, the conventional NH_3 plasma treatment will be replaced by a dual plasma treatment, which adds an additional oxygen plasma on the surface of bottom electrode after conventional NH_3 plasma treatment. In the present case, the bottom electrodes of the MIM capacitors were treated by a dual plasma treatment. Subsequently, we introduce the TiCeO dielectric instead of the TiO_2 dielectric to fabricate MIM capacitors. The TiCeO MIM capacitors were characterized by current-voltage and capacitance-voltage measurements and shown in the following content.

The Figure 2(a) shows the *C-V* characteristics of Ir/TiCeO/TaN capacitors at a 21 nm thickness, fabricated under the optimal conditions of a 400°C PDA and dual plasma treated TaN. A high capacitance density of 17.7-18.4 fF/μm^2 was measured for the TiCeO MIM capacitors. A comparison with other capacitors reported previously is summarized in Table I. In addition, the VCC-α is an important parameter of MIM capacitors for analog applications. The VCC-α characteristics can be obtained by fitting the measured *C-V* characteristics with a second order polynomial equation:

$$C(V)=C_0\ (\alpha V^2\ +\beta V) \qquad [1]$$

Here C_0 is the capacitance at 0 V, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Since the linear−β term can be compensated by circuit design, the quadratic-α is the main factor in the voltage dependence. The Figure 2(b) shows the *ΔC/C-V* charateristics of TiCeO MIM capacitors with a capacitance density of ~18 fF/μm^2. A quadratic-α value of 3192 ppm/V^2 at 1 MHz was measured. From our previous works (10)-(12), the quadratic VCC-α can be improved greatly with increasing the dielectric thickness and a decreased capacitance density used for analog and RF applications.

In Fig 3(a), we show the *J-V* characteristics of TiCeO MIM capacitors with or without O_2 plasma treatment on the bottom electrode. A low leakage current of 1.7×10^{-7} A/cm^2 at -1V under gate injection condition was measured for the samples with O_2 plasma treatment. The comparable leakage currents indicate that the samples with an additional O_2 plasma treatment can be improved by two orders of magnitude effectively. This may be attributed to an additional oxygen plasma to increase the anti-oxidation properties after NH_3 plasma on bottom TaN electrode. Besides, the leakage current from bottom injection is apparently lower than that of the Ir/TiO_2/TaN MIM capacitors described above. This improved leakage current, at a comparable capacitance density, is due to the TiCeO dielectric with a larger ΔE_C and band gap, which lowers the leakage current exponentially. In this work, our TiCeO MIM capacitors exhibit a good performance, compared to th TiTaO and TiHfO capacitors. Under the similar high-κ values, a lower leakage current at -2V was measured for the TiCeO MIM capacitors than

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that of the TiHfO capacitors at a lower capacitance density of 14.3 fF/μm^2. The AFM pictures in Figure 3(b) show the rms roughness of 0.415 nm for only nitrogen plasma and 0.391 nm for both oxygen and nitrogen plasma, respectively. We observed that a smoother bottom surface can be obtained via a dual plasma method. It is well known that a smoother surface can reduce the defect density in the interface between dielectric and bottom electrode. Besides, it is generally believed that the surface roughness effect can be explained in terms of an image force, which lowers the barrier height from gate or bottom injection (20).

The Figure 4(a) shows the leakage current of 1×10^{-6} A/cm^2 at -1 V for the 21 nm thick TiCeO MIM capacitors at 125°C, which is approximately one order of magnitude higher than that at 25°C. The low leakage current at 125°C may be due to the larger ΔE_C and higher work-function electrode, which form a higher Schottky barrier height to lower the thermal leakage. Therefore, the top electrode of high work function Ir not only lowers the leakage current at 25°C, but also reduces the number of gate-injected charges at elevated temperature. To more deeply investigate the current conduction mechanism, we plot *ln(J)* versus $E^{1/2}$ for the Ir/TiCeO/TaN MIM capacitors shown in Figure 4(b),:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \tag{2}$$

$$\gamma = \left(\frac{e^3}{\eta\pi\varepsilon_0 K_\infty}\right)^{1/2} \tag{3}$$

Here K_∞ is the high-frequency dielectric constant (= n^2). The refractive index n is 2.5 or 2.3 for TiO_2 or CeO_2 (21), and η is 1 or 4 for Schottky emission (*SE*) or Frenkel-Poole (*F-P*) conduction, respectively. From the *ln(J)*-$E^{1/2}$ plot, the conduction mechanism of leakage current seems to be dominated by Schottky emission at low electric field and *F-P* emission at high electric field. From the *ln(J/E)*-$E^{1/2}$ plot in Figure 4(c), the extracted linear-β values are the slopes at 25°C and 125°C. The refractive index of 1.8~2.0 for TiCeO dielectric can be deduced at 25°C-leakage current under the conduction mechanism of *F-P* emission from the range of 0.64 MV/cm to 1.21 MV/cm. Since the deduced refractive index is close to the theoretical value of 2.3~2.5, the conduction mechanisms we suggested at low or high electric filed were demonstrated.

Finally, a capacitance density of 11 fF/μm^2 was obtained for a 37 nm thick TiCeO MIM capacitors and the Cross-sectional SEM image of the TiCeO MIM capacitors, inserted in Figure 5, gives a high-κ value of ~45. Therefore, the high-κ TiCeO dielectric may be used as a dielectric for DRAM or RF capacitors.

Conclusions

In this study, a high capacitance density and low leakage current have been achieved in Ir/TiCeO/TaN MIM capacitors. We point out the importance of proper surface treatment on the bottom electrode for the fabrication of MIM capacitors. We also demonstrated that the novel dual-plasma treatment can improve the capacitor performance largely at a processing temperature of 400°C, which could be integrated into DRAM BEOL.

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TABLE I. Comparison of MIM capacitors with various dielectrics and metal electrodes.

	HfO_2 (6)	**Tb-HfO_2 (8)**	**Al_2O_3-HfO_2 (7)**	**TiTaO (10)-(11)**	**TiHfO (13)**	**TiCeO**
Top Electrode	Ta (4.2 eV)	Ta (4.2 eV)	TaN (4.6 eV)	Ir (5.27 eV)	Ni (5.1 eV)	Ir (5.27 eV)
Cap. Density (fF/μm^2)	13	13.3	12.8	23	14.3	18
J (A/cm^2) @25°C	6×10^{-7} (2V)	1×10^{-7} (2V)	8×10^{-9} (2V)	2×10^{-6} (-1V)	8.4×10^{-8} (-1V) 5×10^{-5} (-2V)	1.7×10^{-7} (-1V) 1×10^{-5} (-2V)
α (ppm/V^2)	607	2667	1990	2289	3392	3192
κ	~15	~20	~18	~45	~45	~45

Acknowledgment

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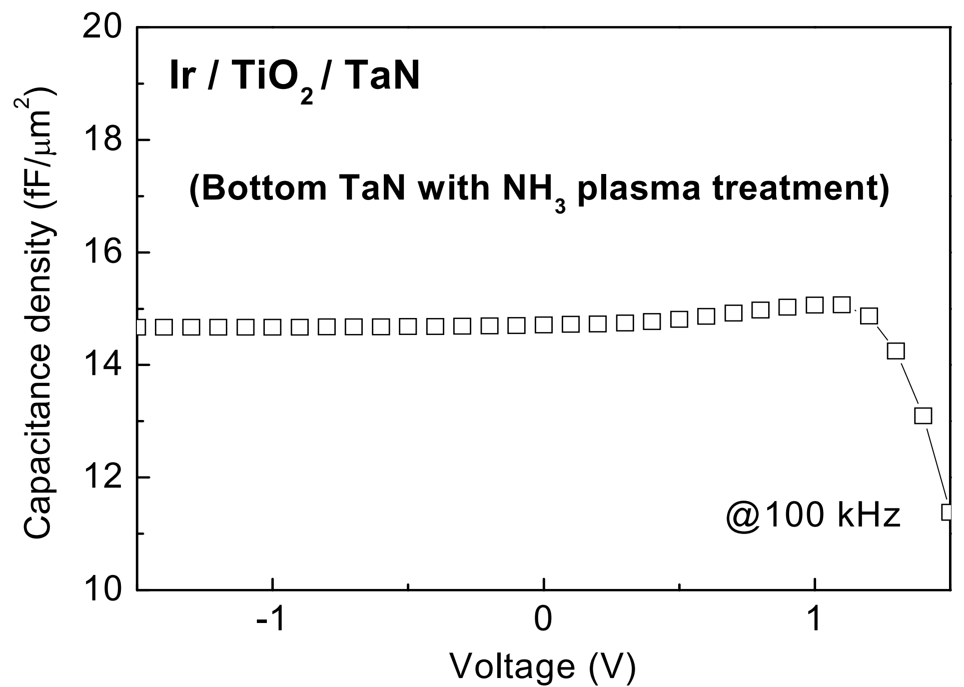
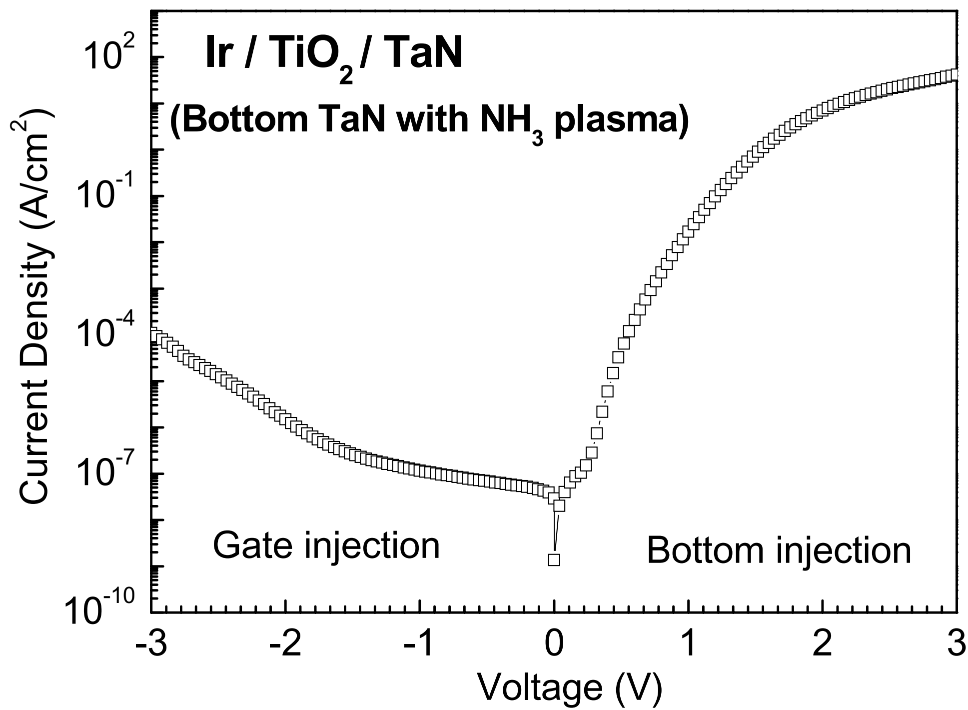


(a)



(b)

Figure 1. (a) *C-V* and (b) *J-V* characteristics of Ir/TiO_2/TaN MIM capacitors processed at 400°C.

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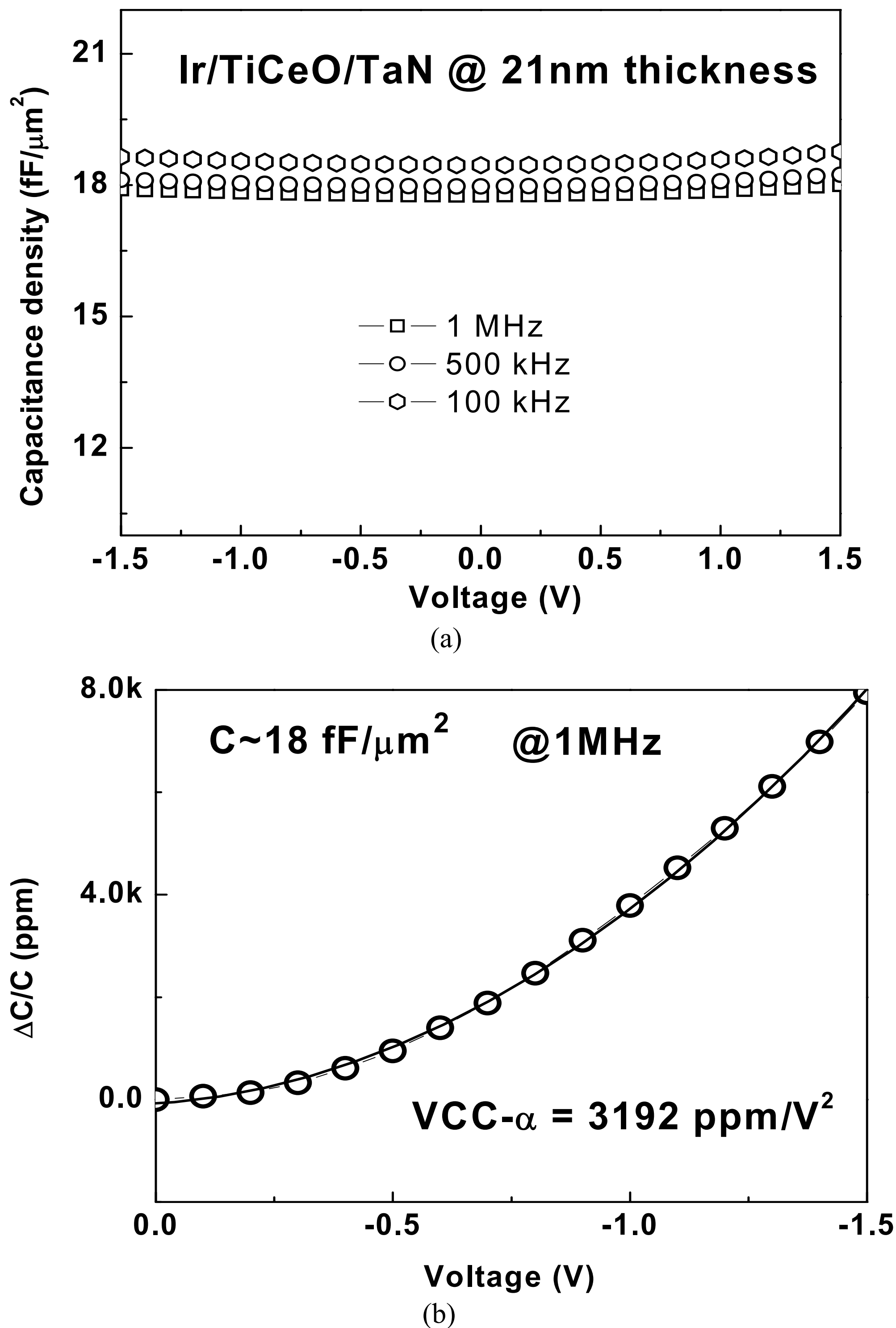

(a)

(b)

Figure 2. (a) *C-V* characteristics of Ir/TiCeO/TaN MIM capacitors with a 21nm thickness measured at various frequencies. (b) The VCC-α characteristics at negative gate bias.

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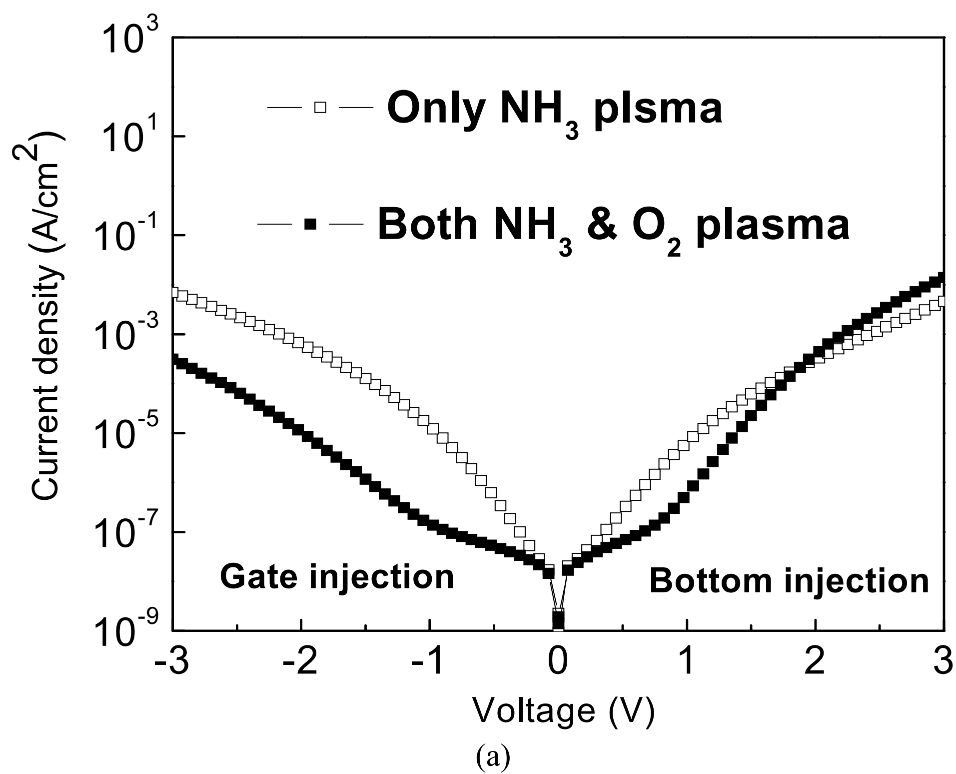
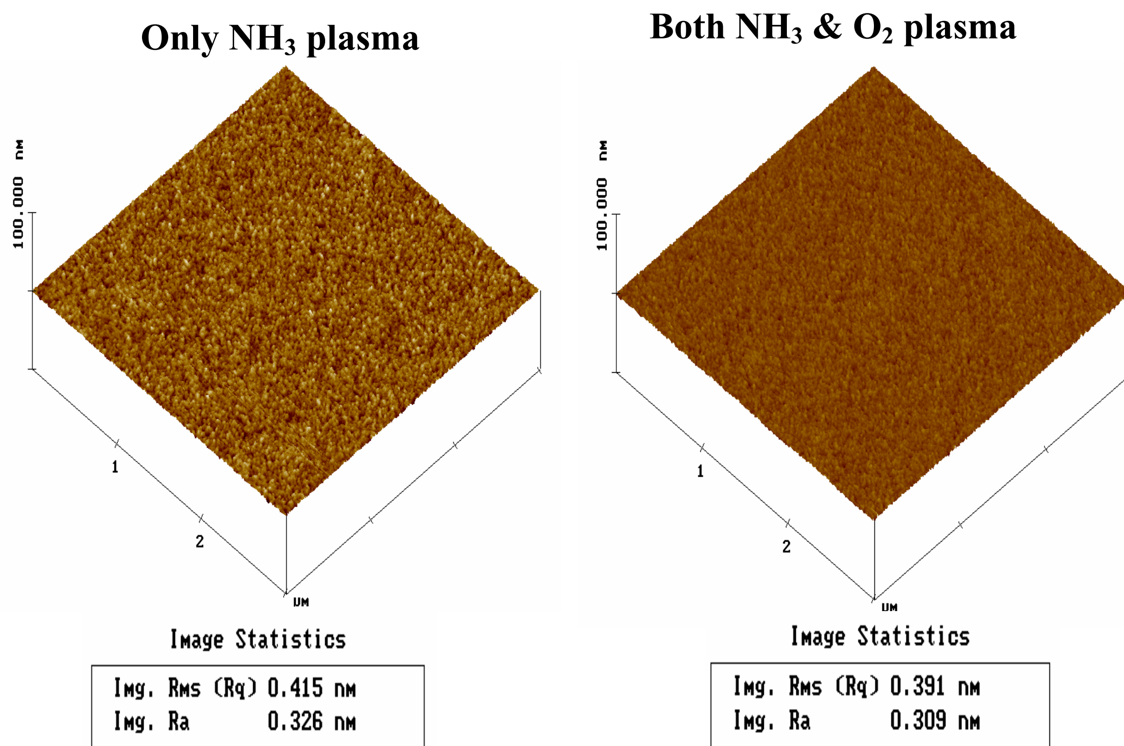


(a)



(b)

Figure 3. (a) The *J-V* characteristics of Ir/TiCeO/TaN MIM capacitors for a 21nm thickness with or without O_2 plasma (b) The surface roughness of bottom electrode by AFM spectroscopy.

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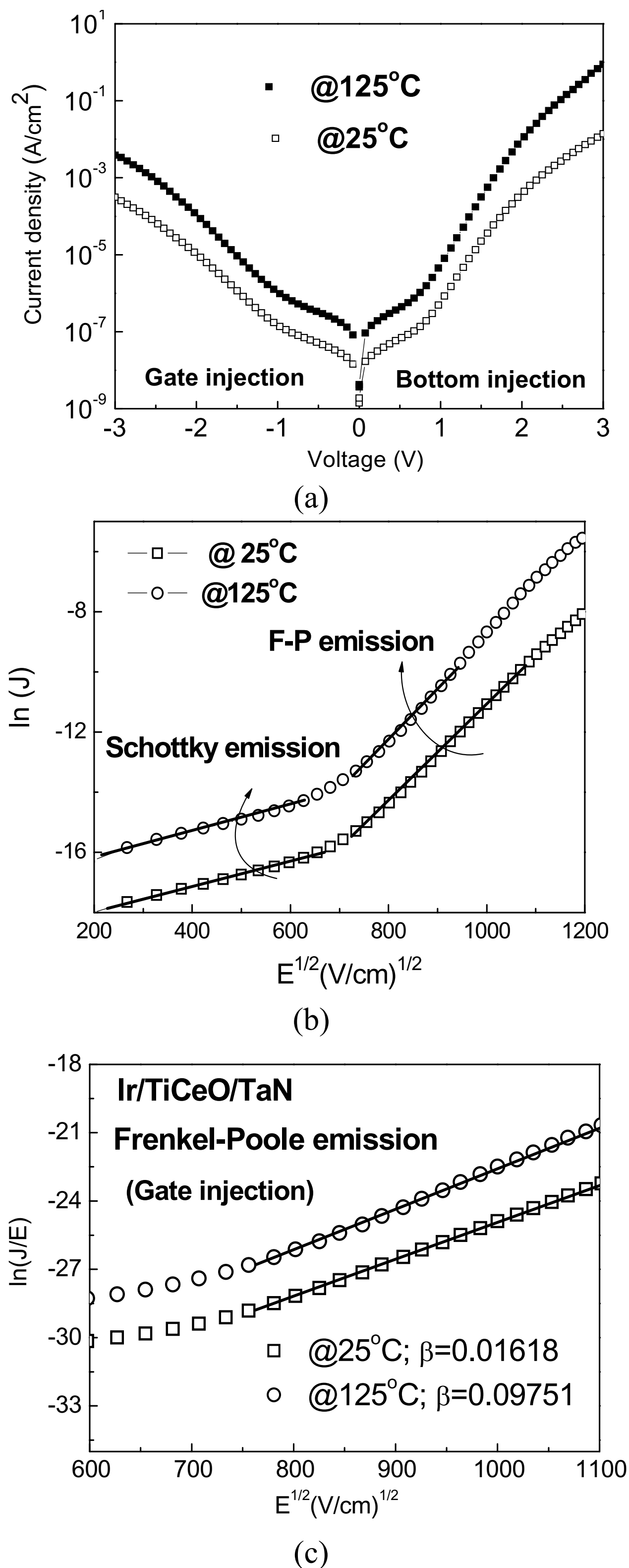

Figure 4. (a) The J-V characteristics of Ir/TiCeO/TaN MIM capacitors with a 21nm thickness at 25°C and 125°C (b) Measured and simulated $lnJ\text{-}E^{1/2}$ of an Ir/TiCeO/TaN capacitor (c) The lnJ versus $E^{1/2}$ plot for Frenkel-poole emission.

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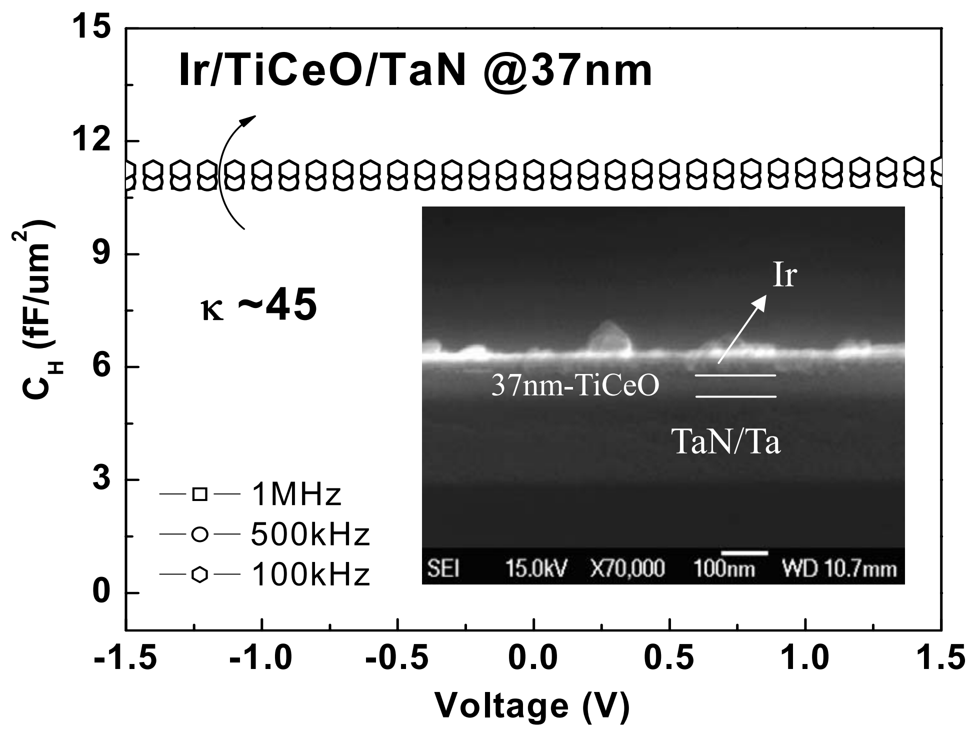

Figure 5. *C-V* characteristics of Ir/TiO_2/TaN capacitors with a 37 nm thickness. The SEM cross-section is shown in the insert.

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