A New Approach to Modeling the Substrate Current of Pre-Stressed and Post-Stressed MOSFET's

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***Abstract*—In this paper, we propose a closed form expression of a new and accurate analytical substrate current model for both pre-stressed and post-stressed MOSFET's. It was derived based on the concept of effective electric field, which gives a more reasonable impact ionization rate in the lucky-electron model. This effective electric field, composed by two experimentally determined parameters, can be regarded as a result of *nonlocal* heating effects within devices. This model shows a significant improvement to the conventional *local field* model. One salient feature of the present model is that it allows us to characterize the time evolution of the substrate current of stressed MOSFET's *for the first time*. Experimental verification for a wide variety of MOSFET's with effective channel lengths down to 0.3 μm shows that the new model is very accurate and is feasible for any kind of MOS device with different drain structures. The present model can be applied to explore the hot carrier effect in designing submicrometer MOS devices with emphasis on the design optimization of a device drain engineering issue. In addition, the present model is well suited for device reliability analysis and circuit level simulations.**

I. Introduction

It is well known that the substrate current I_B can be used as a good monitor of the hot carrier effect [1]. Therefore, accurate prediction of the substrate current is crucial in designing reliable MOS devices and for analyzing circuit level reliability in VLSI/ULSI design [2], [3]. In modeling the substrate current, the widely used form [4]–[6] for device analysis and circuit simulation utilizes the maximum electric field (E_m) in the local electric field for the specific device structure as the dominant factor in hot carrier generation. This local field model for the substrate current agree reasonably well for large devices (e.g., $L_{\text{eff}} > 1.0$ μm). However, for the short channel MOS devices, the local field model fails to model the I_B especially at high gate biases. To improve modeling accuracy, the impact ionization rate has to be modeled nonlocally by considering the two-dimensional (2-D) electric field effects as well as the heating effects [7], [8] (i.e., the solution by considering the nonisothermal effect).

In addition to the drain current degradation in stressed devices, hot carrier induced oxide damages will in turn affect the inner channel electric field distribution which then alter the substrate current characteristics [9]. Due to the difficulty in knowing the exact information about the amount and distribution of interface states or oxide charges, none has been made to model the substrate current characteristics of stressed MOSFET's in analytical form. Undoubtedly, an accurate I_B model for degraded devices is also essential for device and circuit level reliability studies.

To deal with the aforementioned problems, in this paper, we will propose a new analytical substrate current model based on the so-called *effective electric field* instead of the E_m concept to calculate the impact ionization rate as well as the substrate current. Section II describes the new substrate current model and the new approach for modeling both the pre-stressed and post-stressed I_B characteristics. Discussion and the comparison with reported models are also given. Section III presents a major application of this new model to study the hot carrier reliability of a new class of LATID (Large-Angle-Tilt Implanted Drain) MOS devices. Conclusions are given in Section IV.

II. A New Analytical Substrate Current Model

In this section, a self-consistent analytical substrate current model for pre-stressed (fresh) and post-stressed MOSFET's was derived by combining the concept of Lucky-Electron (LE) model and nonlocal field effect within devices. A series of LDD and LATID MOS [10] devices with a wide range of process and device parameters, such as gate oxide thickness (T_{ox}), spacer width (X_{sp}), n$^-$ implantation dosage and implantation angle, are used to justify the accuracy of the present model. All the devices in this study have drawn channel width (W) 20 μm.

A. A New Substrate Current Model for MOSFET

Based on the concept of the effective electric field, an improved I_B model can be expressed as

$$I_B = \frac{\alpha}{\beta} I_D \cdot l_d \cdot E_{\text{eff}} \cdot \exp(-\beta/E_{\text{eff}}) \tag{1a}$$

$$= \frac{\alpha}{\beta} I_D \cdot (V_{\text{DS}} - V_{D\text{hot}}) \cdot \exp(-\beta/E_{\text{eff}}). \tag{1b}$$

Here, the impact ionization rate $\alpha_i = \alpha \cdot \exp(-\beta/E_{\text{eff}})$ is used, in which E_{eff} is used instead of E_m in the conventional LE model. In the LE model, E_m is expressed as $(V_{\text{DS}} - V_{D\text{sat}})/l_d$ [4], where $V_{D\text{sat}}$ is the saturation voltage. We define $E_{\text{eff}} = (V_{\text{DS}} - V_{D\text{hot}})/l_d$ as the effective electric field inside a device

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that is decisive for hot carrier behaviors. l_d is regarded as the effective hot carrier distribution length. $(V_{\rm DS} - V_{D\rm hot})$ is considered as the hot carrier driving force, in which $V_{D\rm hot}$ is the hot carrier starting force. In developing this model, two-dimensional nonlocal field effect or the electron heating effect is included in the $E_{\rm eff}$ term which can be experimentally determined. To extract $E_{\rm eff}$, (1b) is rearranged to obtain another $E_{\rm eff}$ expression which gives

$$E_{\rm eff} = \frac{V_{\rm DS} - V_{D\rm hot}}{l_d} \tag{2a}$$

$$= \frac{\beta}{\ln\left(\frac{I_D \cdot \alpha \cdot (V_{\rm DS} - V_{D\rm hot})}{I_B \cdot \beta}\right)}. \tag{2b}$$

For a given gate bias $V_{\rm GS}$ and from the measured $I_{\rm DS}$-$V_{\rm DS}$ and I_B-$V_{\rm DS}$ curves, two important parameters, $V_{D\rm hot}$ and l_d, can be uniquely obtained by taking the following steps:

1) To calculate saturation voltages $V_{D\rm sat}$ from $I_{\rm DS}$-$V_{\rm DS}$ data, the method described in [11] was adopted here. In this method for determining $V_{D\rm sat}$, a function G is defined as

$$G = g_{\rm ds} \cdot \frac{\partial}{\partial V_{\rm DS}} \cdot \left(\frac{1}{g_{\rm ds}}\right) \tag{3}$$

where $g_{\rm ds} = \partial I_{\rm DS}/\partial V_{\rm DS}$ is the conductance of the device. The first peak values of the G versus $V_{\rm DS}$ curves correspond to the saturation point where $V_{\rm DS} = V_{D\rm sat}$. The $V_{D\rm sat}$ value will be used as the initial guess for undetermined parameter $V_{D\rm hot}$.

2) The surface impact ionization coefficients, α and β, adopt the values by Slotboom et al. [12] and are treated as fixed values in this model. With $V_{D\rm hot}$ initially guessed as $V_{D\rm sat}$, doing iteration between (2a) and (2b) using fixed point algorithm, $V_{D\rm hot}$ and l_d can be found. As (2a) implies, the relationship between $E_{\rm eff}$ versus $V_{\rm DS}$ exhibits a straight line. The intercept of the line with the $V_{\rm DS}$ axis and the slope give $V_{D\rm hot}$ and l_d values.

For different gate voltages, Fig. 1 shows the linear relationship between $E_{\rm eff}$ and $V_{\rm DS}$ for an LDD device, in which L_m and $L_{\rm eff}$ represent the drawn channel length and effective channel length, respectively. $V_{D\rm hot}$ and l_d are found to be increasing functions of $V_{\rm GS}$ and can be expressed as an empirical form easily. The comparison of the I_B characteristics given in Fig. 2 between the modeled and measured results for different channel length devices shows excellent agreements for wide range biases. Fig. 3 shows excellent agreements between modeled and experimentally measured I_B characteristics for both LDD and LATID MOS devices with wide range of gate oxide thickness, n$^-$ implantation dosage and angles. In particular, the effective channel length of the device in Fig. 3 (marked with solid triangle) with n$^-$ dosage 6E13 cm^{-2} and 45° implantation angle is 0.3 μm (extracted using the method described in [13]). One distinct feature of this new approach is that $V_{D\rm hot}$ and l_d are self-consistently extracted from experimental data so that very accurate modeled results can be achieved. Moreover, no additional fitting procedure is needed.

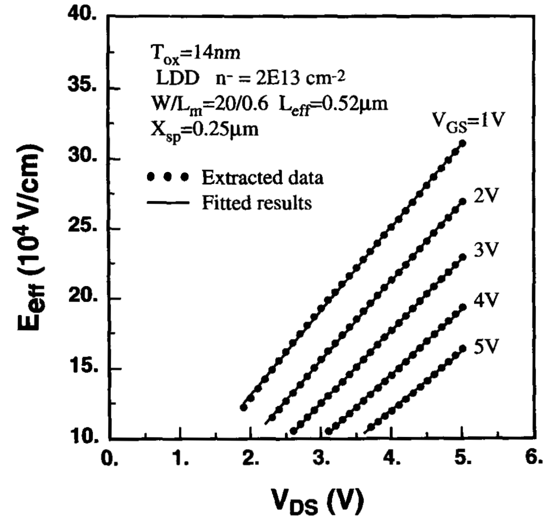

Fig. 1. The extracted effective electric field versus the drain voltages of an LDD device.

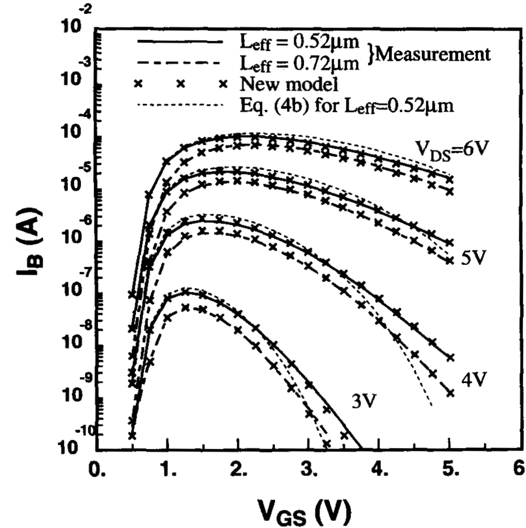

Fig. 2. Comparison of the substrate current between measured and modeled results for two different channel length LDD devices. Dash lines are the results of (4b). Cross marks are the results of the new I_B model. The device parameters are $T_{\rm ox}$ = 140 Å, n$^-$ dose = 2E13 cm^{-2} and $X_{\rm sp}$ = 0.25 μm.

B. Substrate Current Characteristics for Degraded MOSFET's

Owing to the existence of oxide trapped charges and interface states after hot carrier injection, the electric field in the surface depletion area changes. As a result, the $E_{\rm eff}$ varies and then modulates the magnitude of the substrate current. Through the charactization of the time evolution of $V_{D\rm hot}$ and l_d, the substrate current of post-stressed MOSFET can be adequately modeled. To examine the effects of different types of trapped charges and interface states on the variations of $V_{D\rm hot}$ and l_d in n-channel devices, we designed a two-step dc hot carrier

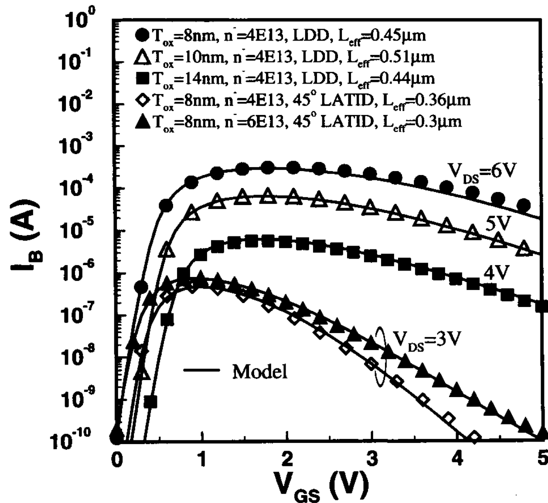

Fig. 3. Comparison of the substrate current between measured and modeled results for LDD and LATID MOS devices with wide range of gate oxide thickness, n$^-$ implantation dosage and angle. Symbols are measured data. Solid lines are modeled results. The L_m and X_{sp} of all devices are 0.6 μm and 0.15 μm, respectively. 45° LATID means the n$^-$ implantation angle is 45° (as illustrated in Fig. 7).

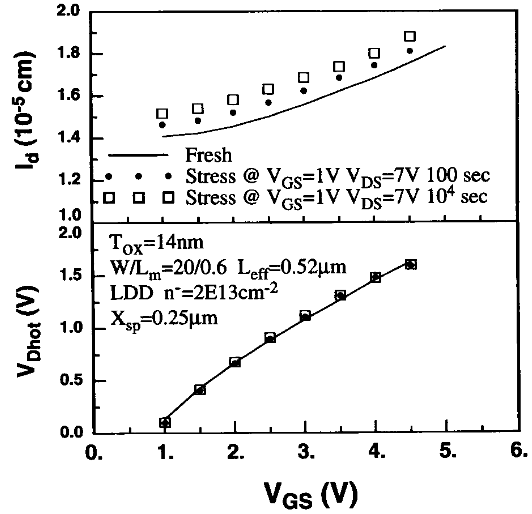

Fig. 4. Time evolution of $V_{D\text{hot}}$ and l_d during hot hole injection at $V_{GS} = 1$ V and $V_{DS} = 7$ V for the same device in Fig. 1. The l_d curve shifts upward.

stress on devices. The device was first biased at $V_{GS} = 1$ V and $V_{DS} = 7$ V for 10^4 seconds stress, then, subsequently biased at $V_{GS} = V_{DS} = 7$ V for another 10^4 seconds stress. The device characteristics were measured during certain period of the stress time. A fixed base level charge pumping measurement [14] was also performed to identify the types of the oxide damages after carrier injection.

1) E_{eff} Variation During Hot Hole Injection: Divices stressed at $V_{GS} = 1$ V and $V_{DS} = 7$ V will cause hole injection, since the direction of the momentum of holes is toward the gate while electron is to the drain. The hole injection generates hole traps in the oxide as identified by charge pumping method, similar measurement results were also observed and well explained in [9]. The time evolution of parameters $V_{D\text{hot}}$ and l_d for a LDD device during hot hole injection are shown in Fig. 4. $V_{D\text{hot}}$ values vary slightly, while the l_d values increase with stress time and the l_d-V_{GS} curve shift in parallel, the resultant E_{eff} decreases. In other words, hole traps reduce the I_B current. Using the extracted parameter values, the modeled I_B characteristics of a post-stressed device and the comparison with experiment for two successive stress time are given in Fig. 5 which shows excellent agreement. The new model successfully characterizes the E_{eff} variations.

2) E_{eff} Variation During Hot Electron Injection: The same device was continuously biased at $V_{GS} = V_{DS} = 7$ V for additional stress to generate hot electron injection. Judging from charge pumping measurement, the latter electron injection generates large amount of negative charges, which can be negative oxide traps and acceptor-type interface states as explained in [9]. The time evolution of $V_{D\text{hot}}$ and l_d during hot electron injection was evaluated and a similar result to Fig. 4 was obtained. The l_d-V_{GS} curve shifts parallelly, however, the l_d values decrease with stress time in contrast to the effect of aforementioned hole injection. The $V_{D\text{hot}}$-V_{GS} curve merely increasingly shifts to a relatively large value (0.03 V in this case) in a very short time (less than 50 seconds) stress and then almost unchanges in the following stress, the resultant E_{eff} increases with stress time. In other words, negative oxide traps and acceptor-type interface states enlarge I_B.

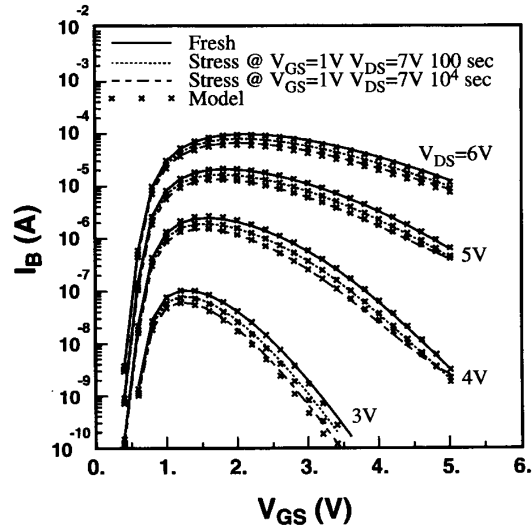

Fig. 5. Comparison of the post-stressed substrate current between measured and modeled results for the same device as in Fig. 1. The lines are the measured data for fresh, after 100 sec stress and after 10^4 sec stress, respectively. Cross marks are the modeled results.

3) The E_{eff} Variation of Post-Stressed MOSFET's in Reverse Mode Operation: The reverse mode I_B characteristics (exchanging source and drain electrodes) were also characterized to study the influence of source side oxide damages on the

hot carrier behaviors. The stress was done at $V_{GS} = 1$ V and $V_{DS} = 7$ V for 10^4 seconds. The parameters V_{Dhot} and l_d show very different variations with stress time and V_{GS} as compared with the aforementioned two forward mode cases. V_{Dhot} values increase especially at higher V_{GS} biases. On the contrary, l_d values decrease gradually with increasing V_{GS}. Higher gate bias magnifies the oxide damage effect at the source side. Longer stress time has larger variations. The resultant effect of the source side oxide damages reduce E_{eff}, and thereby giving rise to the decrease of I_B with stress time. The reverse mode E_{eff} of LDD devices has larger degradation than that of LATID devices which will be explained later.

C. Discussion

Several implications from the comparison of the present model with the conventional ones [4]–[6] can be drawn as follows:

1) In modeling the substrate current of a conventional single drain MOS device, the following form of the conventional approach [5] based on the local field concept is widely used

$$I_B = \frac{\alpha}{\beta} I_D \cdot l_d \cdot E_m \cdot \exp(-\beta/E_m) \tag{4a}$$

$$= \frac{\alpha}{\beta} I_D \cdot (V_{DS} - V_{Dsat}) \cdot \exp(-\beta l_d/(V_{DS} - V_{Dsat})), \tag{4b}$$

in which $E_m = (V_{DS} - V_{Dsat})/l_d$ is generally considered as the maximum electric field along the channel. Two approaches are commonly used to calculate E_m. (a) V_{Dsat} is extracted experimentally by utilizing the idea implied in (4b) as first described in [5], and the l_d is presumably formulated related to the device geometry [15] which is treated as the characteristic length that is bias independent. In this appraoch to model I_B, α and β values can be extracted experimentally from (4b) as long as V_{Dsat} and l_d have been calculated. (b) The E_m value and its expressions are obtained or fitted from device simulation or analytical electric field models [4], [6]. The modeled results of (4b) using approach (a) are compared with the new model and the measured data as shown in Fig. 2. Since the model parameters are not all directly extracted from experimental data self-consistently, the above approaches more or less require adjustable parameters (e.g., α and β) to reasonably match their models with measured data. However, their results often mismatch the I_B values at higher V_{GS} values since their E_m expressions fail to reflect the complicated electric field variations over wide biases. In the new approach here, E_{eff} really reflects the 2-D electric field effect so that the overall impact ionization rate $\alpha \cdot \exp(-\beta/E_{eff})$ accurately determines the I_B value.

2) One salient feature of the new approach is that it can be applied to any kind of MOS devices with different drain structures (e.g., LDD, LATID devices). However, the conventional approaches to obtained E_m were derived based on the conventional single drain MOS devices only, and needs individual modification for different LDD structures.

3) The extracted V_{Dhot} is smaller than its initial guess V_{Dsat}. For the first time, this model suggests that the hot carrier driving force should be $(V_{DS} - V_{Dhot})$ instead of widely used value $(V_{DS} - V_{Dsat})$ which reflects only maximum electric field. In other words, the E_m concept is not adequate to present 2-D effect inside devices. Fig. 6 compares the positions of V_{Dsat} and V_{Dhot} on the I_{DS}-V_{DS} curves of a LDD device. This implies that the drain biased at a point below saturation region has already significantly contributed to the impact ionization. Moreover, the effective hot carrier distribution length is an increasing function of V_{GS} and is independent of the drain bias. For circuit simulation use, V_{Dhot} and l_d can be well formulated as $V_{Dhot} = V_{D0} + V_{D1} \cdot V_{GS} + V_{D2} \cdot V_{GS}^2$ and $l_d = l_{d0} + l_{d1} \cdot V_{GS} + l_{d2} \cdot V_{GS}^2$, respectively. From the new I_B model and the extracted E_{eff}, the carrier energy distribution inside a device can be figured out as follows. (a) For a given V_{DS}, a higher V_{GS} bias results in a smaller hot carrier driving force $(V_{DS} - V_{Dhot})$ and longer effective distribution length, reflecting the profile that the carrier energy in such biases has a more slower variation and wider distributions. (b) For a given V_{GS}, larger V_{DS} results in a higher $(V_{DS} - V_{Dhot})$ value across the same distribution length so that gives a higher peak electric field.

4) Various stress experiments performed at different biases and devices show that the hot carrier induced oxide damages have minor effect on the overall apparent hot carrier driving force $(V_{DS} - V_{Dhot})$. However, l_d is sensitive to the net amount of total trapped oxide charges. The parallel shift of l_d curves in Fig. 4 can be characterized and empirically formulated as a function of time given by

$$\Delta l_d = 3.0712 \times 10^{-7} \cdot \log(t)\,(\text{cm}). \tag{5}$$

With V_{Dhot} approximately unchanged, the stressed I_B characteristics (Fig. 5) can be predicted by employing (5) with very high accuracy.

5) During the hot carrier injection, large amount of interface states are generated below the sidewall spacer at the drain side which then in reverse mode operation electrically deplete mobile carriers at the source side and thus induce additional series resistance there. The variations of $(V_{DS} - V_{Dhot})$ and l_d in reverse mode are caused by an extra voltage drop at the source side due to the increased series resistance which effectively decreases drain bias and gate bias. This resistance effect is more obvious at higher V_{GS} biases, since the larger drain current enhances more larger voltage drop across the damaged region. Assume $\Delta V(V_{GS})$ is the voltage dropped at source region, the effective gate bias excluding resistance effect reduces to $(V_{GS} - \Delta V(V_{GS}))$, which reduces the drain current. Owing to less amount of conducting carriers in the channel, the carriers in the

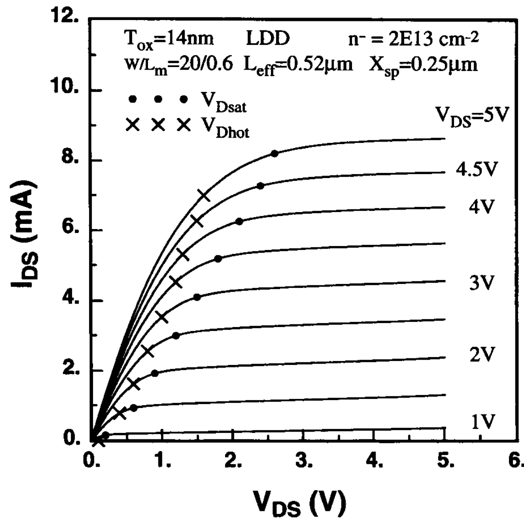

Fig. 6. Comparison of $V_{D\mathrm{sat}}$ and $V_{D\mathrm{hot}}$ on the I_{DS}-V_{DS} curves for the same device in Fig. 1.

drain side are easily to be depleted by the lateral electric field, the device thus exhibits a smaller l_d value. The effective drain bias excluding resistance effect is also reduced to $(V_{\mathrm{DS}} - \Delta V(V_{\mathrm{GS}}))$. The hot carrier driving force across the impact ionization region becomes

$$V_{\mathrm{DS}} - \Delta V(V_{\mathrm{GS}}) - V_{D\mathrm{hot,0}} = V_{\mathrm{DS}} - V_{D\mathrm{hot}}, \quad (6)$$

where $V_{D\mathrm{hot}} = (V_{D\mathrm{hot,0}} + \Delta V(V_{\mathrm{GS}}))$ and $V_{D\mathrm{hot,0}}$ is the hot carrier starting voltage without oxide damages at source side. Because the drain bias applied at drain electrode is still V_{DS}, the characterized resistance effect is emerged into $V_{D\mathrm{hot}}$, which makes the overall $V_{D\mathrm{hot}}$ values larger at higher V_{GS}. In summary, the influence of source side oxide damages on the I_B characteristics comes from the lowering of the hot carrier driving force and the narrowing of the effective distribution length. The degree of the variations of $V_{D\mathrm{hot}}$ is larger than that of l_d, the resultant E_{eff} within devices is reduced. The E_{eff} degradation of LDD devices is larger than LATID devices since LDD devices suffer greater hot carrier effect (see Fig. 8). Large amount of interface states are generated which mostly located outside the gate edge [10], [16] in LDD device. Therefore, the resistance effect of LDD devices is more significant.

III. Hot Carrier Analysis of Various LDD-Structure Devices Using E_{eff}

By applying the present I_B model to a set of n-channel LATID MOS devices [10] and evaluating the performance degradation of these devices under hot carrier effect, we will demonstrate that E_{eff} can be also used as a good monitor of the hot carrier reliability. The LATID MOS device samples were fabricated using the standard poly-silicon gate CMOS technology. The gate oxide is 140 Å. After the conventional gate etching step of CMOS process, a phosphorus n^- tilt angle implantation of dosage 2E13 cm^{-2} with energy 80 kev was performed with tilt angle θ (0° to 60°) from the source and drain sides by rotating the wafer automatically. Then heavy Arsenic n^+ implant was done by a 0.25 μm vapor-deposited oxide spacer width offset from the gate edge for all devices. The drawn channel length of all devices discussed here is 0.6 μm.

The extracted effective electric fields of LATID MOS devices with various tilt angles are compared in Fig. 7. Smaller effective electric field is observed for devices with larger implantation angle although their drain current is larger as presented in our reported results [17]. Due to gate control over the longer n^- region and the separation of main current path away from maximum heating points within device formed by large tilt angle implantation, the resultant E_{eff} in LATID MOS device is thus reduced. To examine the relationship between E_{eff} and hot carrier reliability, we performed a dc hot carrier stress biased at $V_{\mathrm{GS}} = 3.5$ V and $V_{\mathrm{DS}} = 7$ V to evaluate their interface state generation and the associated normalized drain current degradation $(\Delta I_D/I_{D0})$. The results are given in Fig. 8. The interface states (ΔN_{it}) are characterized by charge pumping measurement. We found that LATID device with larger implantation angle has smaller amount of ΔN_{it} and less $\Delta I_D/I_{D0}$, which means that hot carrier effect in such device is alleviated. The trend of the hot carrier effect in the characterized devices is consistent with that given by extracted E_{eff}. In other words, device with smaller E_{eff} will suffer less hot carrier effect and vice versa. E_{eff} successfully quantitizes hot carrier effect. Therefore, to compare the hot carrier reliability between various devices, in particular for the device drain engineering applications, E_{eff} and its components $(V_{\mathrm{DS}} - V_{D\mathrm{hot}}$, and $l_d)$ can provide more detailed physical information of the hot carrier effect than the conventional measured I_B/I_D ratio that people commonly used.

IV. Conclusion

In this paper, a new concept for modeling the hot carrier induced MOS device substrate current is proposed. Three major improvements over the previous models are 1) an effective electric field is introduced in the model to account for the hot carrier heating and 2-D field (nonlocal) effects within devices; 2) the new analytical substrate current model is rather flexible and suitable for any kind of MOS devices with different drain structures; and 3) *it enables us to model the post-stressed I_B characteristics for the first time.* This study also finds that different types of oxide damages show very different influences on the effective electric field. The post-stressed I_B characteristics are skillfully modeled through characterizing the time evolution of effective electric field. The new approach accurately calculates the I_B characteristics for MOS devices with effective channel length down to 0.3 μm.

One major application of the present model is to explore the hot carrier effect in designing a submicron MOS device with emphasis on the drain engineering issue. With a trade-off between the use of n^- implantation dosage and angle, we conclude that the design optimization of a hot carrier

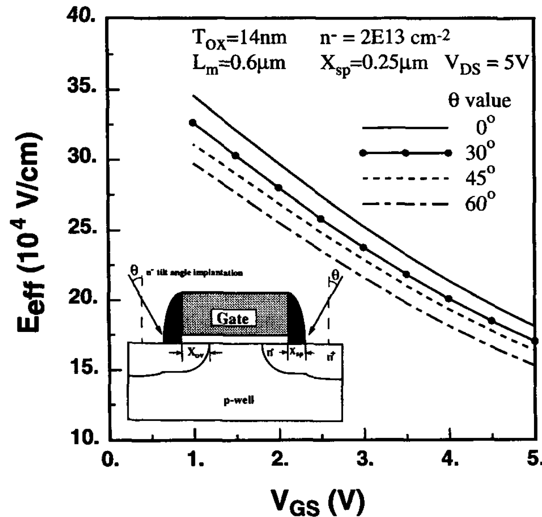

Fig. 7. Extracted effective electric field for LATID MOS devices with various n^- implantation angles. The insert is a schematic diagram of a LATID MOS device.

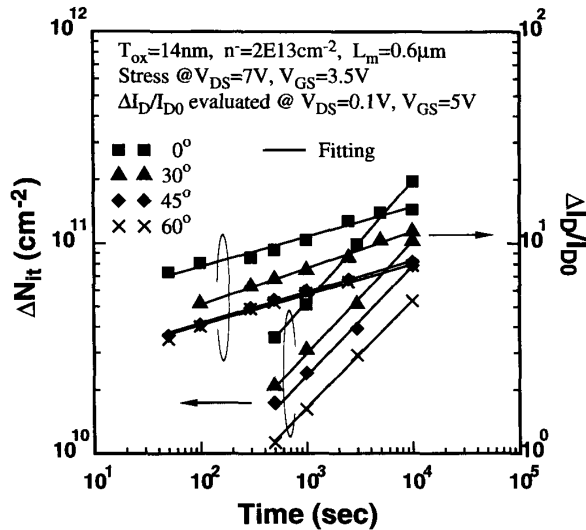

Fig. 8. Time evolution of hot carrier generated ΔN_{it} and linear region drain current degradation for LATID MOS devices with various implantation angles.

resistant LATID device can be better understood through the use of the newly developed substrate current model. The newly developed substrate current model can be further incorporated into SPICE models to evaluate the circuit level hot carrier reliability [18].

REFERENCES

[1] E. Takada and N. Suzuki, "An empirical model for device degradation due to hot-carrier injection," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 111–113, 1983.

[2] Y. Leblebici and S.-M. Kang, "Modeling of nMOS transistors for simulation of hot-carrier-induced device and circuit degradation," *IEEE Trans. Computer-Aided Design*, vol. 11, no. 2, pp. 235–246, 1992.

[3] S. S. Chung, P.-C. Hsu, and J.-S. Lee, "A new MOSFET hot carrier model in SPICE feasible for VLSI reliability analysis," in *Proc. Int'l VLSI Technology, Sys., and Appl.*, Taipei, Taiwan, May 22–24, 1991, pp. 283–287.

[4] P. K. Ko, "Hot-electron effects in MOSFET's," Ph.D. Dissertation, Dept. of Electrical Engineering and Computer Science, Univ. of California, Berkeley, June 1982.

[5] T. Y. Chan, P. K. Ko, and C. Hu, "A simple method to characterize substrate current in MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 505–507, 1984.

[6] G.-S. Huang and C.-Y. Wu, "An analytical saturation model for drain and substrate currents of conventional and LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. 37, no. 7, pp. 1667–1677, 1990.

[7] C. G. Hwang and R. W. Dutton, "Substrate current model for submicrometer MOSFET's based on mean free path analysis," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1348–1354, 1989.

[8] S. S. Chung and G.-H. Lee, "Accurate modeling of the energy-dependent hot electron effects in submicron MOSFET's," in *Proc. 1993 Int. Conf. Solid State Devices and Materials*, Chiba, Japan, Aug. 28–Sept. 1, 1993, pp. 479–481.

[9] P. Heremans, R. Bellens, G. Groeseneken, and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2194–2209, 1988.

[10] T. Hori, J. Hirase, Y. Odake and T. Yashi, "Deep-submicrometer large-angle-tilt implanted drain (LATID) technology," *IEEE Trans. Electron Devices*, vol. 39, no. 10, pp. 2312–2324, 1992.

[11] W. Y. Jang, C. Y. Wu, and H. J. Wu, "A new experimental method to determine the saturation voltage of a small-geometry MOSFET," *Solid-State Electron.*, vol. 31, pp. 1421–1431, 1988.

[12] J. W. Slotboom, G. Streutker, G. J. T. Davids, and P. B. Hartog, "Surface impact ionization in silicon devices," in *IDEM Tech. Dig.*, pp. 494–497, 1987.

[13] S. S. Chung and J.-S. Lee, "A new approach to determine the drain-to-source series resistance of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, no. 9, pp. 1709–1711, 1993.

[14] S. S. Chung, J.-J. Yang, C.-H. Tang, and P.-C. Chou, "Characterization of hot electron induced interface states in LATID MOS devices using an improved charge pumping method," in *Proc. 1993 Int. Conf. Solid State Devices and Materials*, Chiba, Japan, Aug. 28–Sept. 1, 1993, pp. 841–843.

[15] T. Y. Chan, P. K. Ko, and C. Hu, "Dependence of channel electric field on device scaling," *IEEE Electron Device Lett.*, vol. EDL-6, no. 10, pp. 551–553, 1985.

[16] F.-C. Hsu and H. R. Grinolds, "Structure-enhanced MOSFET degradation due to hot-electron injection," *IEEE Electron Device Lett.*, vol. EDL-5, pp. 71–74, 1984.

[17] J.-J. Yang, S. S. Chung, P.-C. Chou, C.-S. Chen, and M.-S. Lin, "Suppression of the hot carrier effect in designing LATID MOS devices based on a new substrate current model," in *Proc. Int'l VLSI Technology, Sys., and Appl.*, Taipei, Taiwan, May 12–14, 1993, pp. 173–177.

[18] J.-J. Yang, S. S. Chung, P.-C. Chou, C.-S. Chen, and M.-S. Lin, "A consistent drain and substrate current model of LDD MOS devices for circuit simulation," in *Proc. Int'l Workshop on VLSI Process and Devices Modeling (VPAD)*, Nara, Japan, May 14–15, 1993, pp. 140–141.

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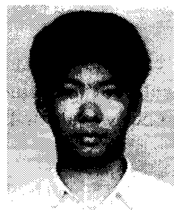

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