

# Modeling the Positive-Feedback Regenerative Process of CMOS Latchup by a Positive Transient Pole Method—Part II: Quantitative Evaluation

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**Abstract**—The positive-feedback regenerative process in a p-n-p-n structure during CMOS latchup transition has been modeled by a time-varying positive transient pole. The maximum peak value of the positive pole and the time required to first initiate the positive pole are adopted as two useful and meaningful parameters to quantitatively investigate the influence of device parameters on the positive-feedback regeneration of CMOS latchup. Some design guidelines can be obtained to improve latchup immunity of CMOS IC's.

## I. INTRODUCTION

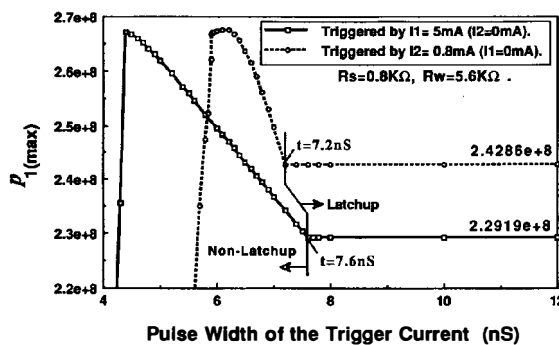
THE dynamic behaviors of CMOS latchup transition have been analyzed by the lumped equivalent two-transistor model and the time-varying large-signal base-emitter voltage waveforms of the cross-coupled bipolar transistors have been solved in [1]. In each time interval, the base-emitter voltage waveforms can be further represented as two-pole functions of time by the piecewise-linearized approximation. One of the poles is found to increase from negative to positive during the transition of latchup. After latchup occurs, this positive transient pole will decrease from positive to negative again to retain latchup in its stable low-impedance state.

Although a pole with positive value had ever appeared in several early works to qualitatively explain the turn-on transition of thyristors [2], [3], there was never an important parameter used to quantitatively investigate the positive-feedback regenerative process in a p-n-p-n structure. In this paper, the positive-feedback regenerative process in a p-n-p-n structure is quantitatively investigated by  $p_{1(\max)}$  and  $t_r$  parameters, which are the maximum peak value of the time-varying positive pole during the latchup transition and the minimum time period required to initiate this positive pole [1]. By using these two parameters, the influence of device parameters on the positive-feedback regenerative process in CMOS latchup are quantitatively investigated. Some design guidelines on the device parameters to prevent CMOS transient-induced latchup can be highlighted.

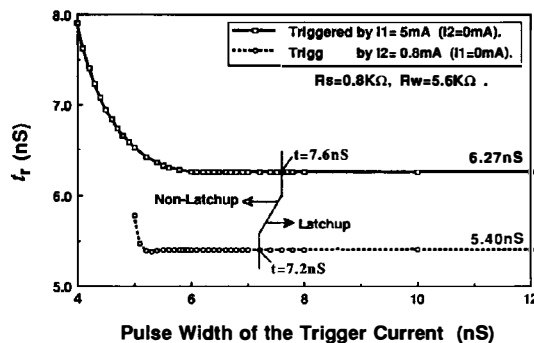
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(a)



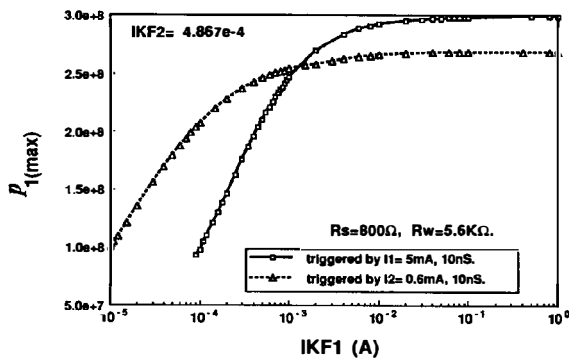
(b)

Fig. 1. The variations of (a)  $p_{1(\max)}$  and (b)  $t_r$  when the p-n-p-n structure is triggered by a 5-mA  $I_1$  or a 0.8-mA  $I_2$  with different pulse widths.

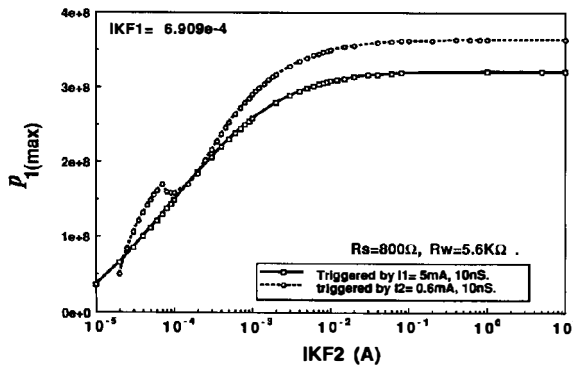
## II. QUANTITATIVELY MODELING THE POSITIVE-FEEDBACK REGENERATIVE PROCESS

### A. The Maximum Value of Positive Pole and The Time to Initiate Positive Pole

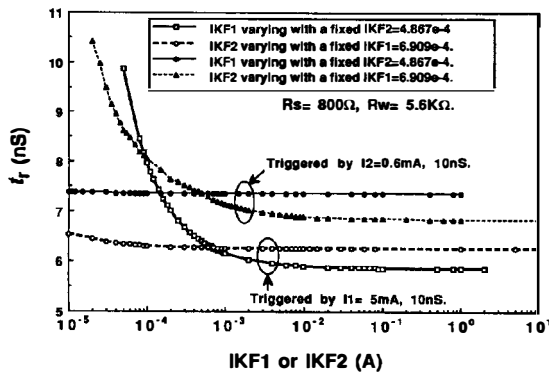
A p-n-p-n structure triggered by trigger currents with different pulse widths or different pulse heights will lead to different values of  $p_{1(\max)}$  and  $t_r$ . The curves in Fig. 1(a) and (b) show the variations on  $p_{1(\max)}$  and  $t_r$  due to  $I_1 = 5$  mA or  $I_2 = 0.8$  mA triggering with different pulse widths. The device parameters in the p-n-p-n structure used for calculation are listed in Table I of [1] with the substrate (well) resistance of 0.8 K $\Omega$  (5.6 K $\Omega$ ). In Fig. 1(a), as the pulse width of trigger



(a)



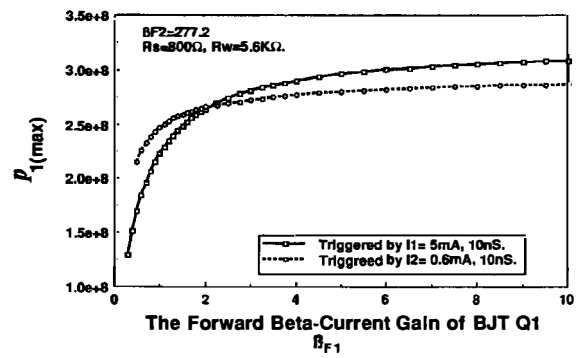
(b)



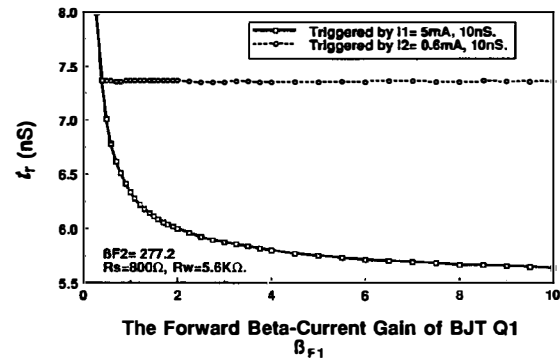
(c)

Fig. 2. The relations between (a)  $p_{1(\max)}$  and  $I_{KF1}$  parameter of BJT  $Q_1$ , (b)  $p_{1(\max)}$  and  $I_{KF2}$  parameter of BJT  $Q_2$ , (c)  $t_r$  and the  $I_{KF1}$  or  $I_{KF2}$  parameters, due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

current is greater than 7.6 nS for  $I_1 = 5$  mA ( $I_2 = 0$ ) or 7.2 nS for  $I_2 = 0.8$  mA ( $I_1 = 0$ ) in the latchup range,  $p_{1(\max)}$  is held at a constant value about  $2.2919 \times 10^8$  or  $2.4286 \times 10^8$ , respectively. If the pulse width of trigger current decreases from the critical time period,  $p_{1(\max)}$  raises up sharply and then it drops to zero suddenly as the pulse width of trigger current is much reduced. In Fig. 1(b),  $t_r$  is held at 6.27 nS (5.40 nS) for the triggering of  $I_1 = 5$  mA ( $I_2 = 0.8$  mA) in the latchup range. As the pulse width of trigger current is less



(a)



(b)

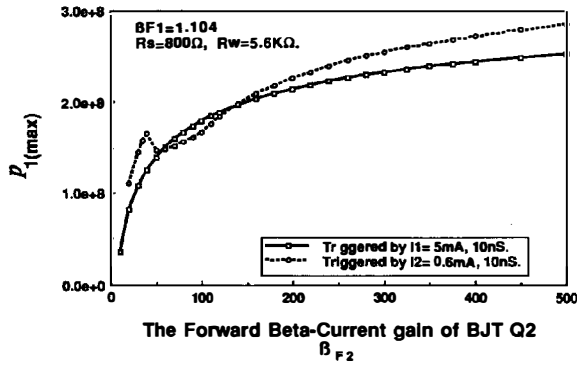
Fig. 3. The influence of the forward beta gain  $\beta_{F1}$  of BJT  $Q_1$  on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

than this constant value,  $t_r$  is first held as a nearly constant value in the nonlatchup range but then it quickly increases to infinite. The time  $t_r$  raising up to infinite means that the positive pole does not occur when the trigger current has a too short pulse width.

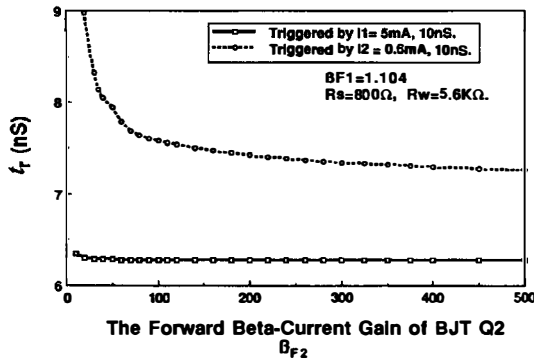
The values of  $p_{1(\max)}$  and  $t_r$  in the latchup range of Fig. 1(a) and (b) are held as constants in spite of different pulse widths of the trigger current. Therefore, for a trigger current with fixed pulse height, there exist the corresponding constant  $p_{1(\max)}$  and  $t_r$  in latchup case. These constant  $p_{1(\max)}$  and  $t_r$  can be seen as one of inherent characteristics of a p-n-p-n structure. Thus, they can be adopted as meaningful parameters to find the influence of device parameters on the positive-feedback regeneration of CMOS transient-induced latchup.

### B. The Difference Between the Time to Initiate Positive Pole and the Time to Cause Latchup

By using iterative HSPICE simulations, the p-n-p-n structure is found to be triggered into latchup only as the pulse width of 5-mA  $I_1$  is greater than 7.6 nS and that of 0.8-mA  $I_2$  greater than 7.2 nS. It is very interesting to find the reasons why the time  $t_r$  of 6.27 nS (5.40 nS) to initiate the positive pole and the minimum pulse width of 7.6 nS (7.2 nS) to cause latchup due to  $I_1 = 5$  mA ( $I_2 = 0.8$  mA) triggering are different.



(a)



(b)

Fig. 4. The influence of the forward beta gain  $\beta_{F2}$  of BJT  $Q_2$  on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

An analytical criterion based on the product of large-signal transient current gains greater than unity has been developed to judge the occurrence of latchup [4]. The criterion has been expressed as

$$\beta_{1tr}(t) \cdot \beta_{2tr}(t) \geq 1 \quad (1)$$

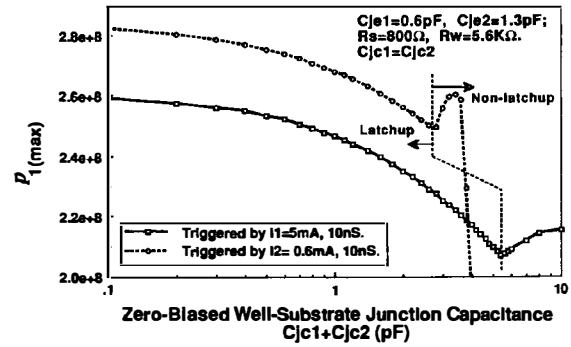
where

$$\beta_{1tr}(t) \equiv \frac{i_{C1}(t)}{i_{B1}(t)} \quad (2)$$

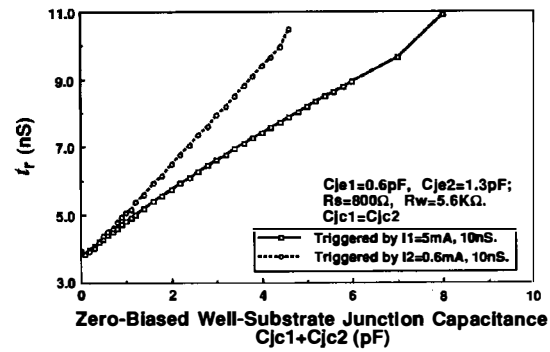
$$\beta_{2tr}(t) \equiv \frac{i_{C2}(t)}{i_{B2}(t)}. \quad (3)$$

$\beta_{1tr}(t)$  and  $\beta_{2tr}(t)$  are heavily dependent upon the junction capacitances in a p-n-p-n structure.

With this " $\beta_{1tr} \cdot \beta_{2tr} \geq 1$ " criterion, the difference between the minimum pulse width to cause latchup and the time  $t_r$  to initiate positive pole can be clearly explained. The time  $t_r$ , when the positive pole occurs, is the time that the positive-feedback regeneration starts. Although the starting of the positive-feedback regeneration will quickly push a p-n-p-n structure into latchup with a double exponential regenerative rate [1], it still needs a time period to cause the happening



(a)

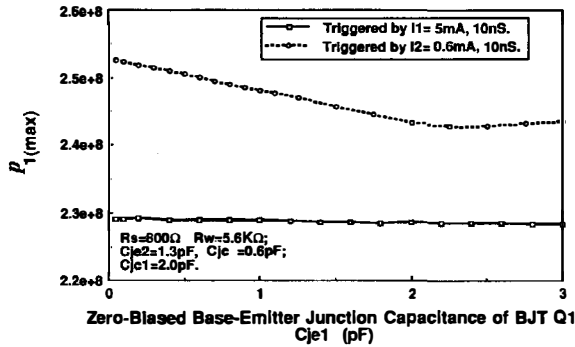


(b)

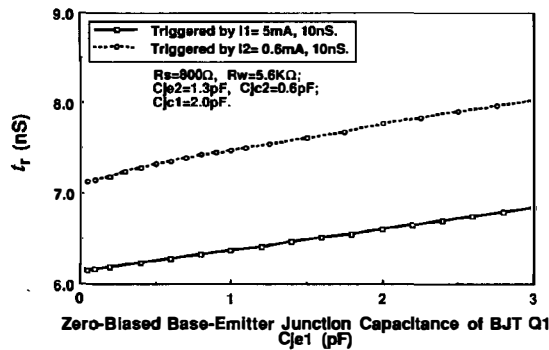
Fig. 5. The influence of the well-substrate junction capacitance on (a)  $p_{1(\max)}$  and (b)  $t_r$ , due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA triggering with a 10-nS pulse width.

of latchup. This time period is about 1.33 (1.8) nS for the triggering of  $I_1 = 5$  mA ( $I_2 = 0.8$  mA). A p-n-p-n structure which has a stronger positive-feedback regeneration needs a shorter time period to cause latchup after the occurrence of positive pole. The time, when latchup happens, have been found as the time that the value of  $\beta_{1tr}(t) \cdot \beta_{2tr}(t)$  reaches to unity [4]. So, if the trigger current with a pulse width long enough to initiate the positive pole but not long enough to make the value of  $\beta_{1tr}(t) \cdot \beta_{2tr}(t)$  reach to unity, the p-n-p-n structure is still not triggered into latchup state.

Moreover, there may be a question why the maximum positive pole in nonlatchup range has a greater value than that in latchup range, as shown in Fig. 1(a). The anomalous increase of  $p_{1(\max)}$  in nonlatchup range is due to the happening of physical self-regeneration in a p-n-p-n structure after the trigger current is off. This physical self-regeneration with the absence of trigger current in nonlatchup case causes the high-level injection effect, which occurs as the collector currents of BJT's  $Q_1$  and  $Q_2$  are greater than their  $I_{KF}$  parameters, to occur much later. Since the self-regeneration in the base and collector currents without enough supporting from the trigger current can not push  $\beta_{1tr} \cdot \beta_{2tr}$  to reach to unity, the collector currents of BJT's  $Q_1$  and  $Q_2$  raise up slower and then will gradually decrease because of the absence of latchup. Thus, the positive pole can grow up toward a larger value before the high-level injection effect occurs in the nonlatchup case.



(a)



(b)

Fig. 6. The influence of the base-emitter junction depletion capacitance of BJT  $Q_1$  on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

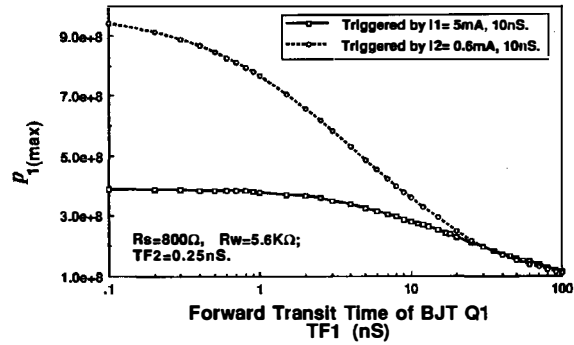
### III. THE INFLUENCES OF DEVICE PARAMETERS ON THE POSITIVE-FEEDBACK REGENERATION

In this section, the influence of device parameters on the positive-feedback regeneration during latchup transition is quantitatively investigated by the  $p_{1(\max)}$  and  $t_r$  parameters.

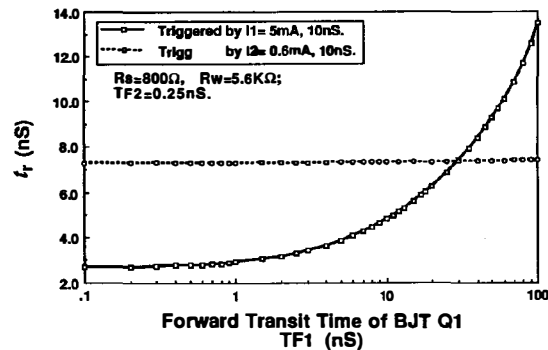
#### A. The Influence of Current-Gain Parameters

The value of  $p_1$  pole changing from positive to negative after latchup is due to the high-level injection effect which causes serious current-gain degradation in the parasitic BJT's  $Q_1$  and  $Q_2$ . The high-level injection effect, which is modeled by the knee-current  $I_{KF}$  parameter in the Gummel-Poon model of BJT device [5]–[7], degrades the current gains of BJT's  $Q_1$  and  $Q_2$  when these BJT's are heavily turned on during latchup transition in a p-n-p-n structure.

To quantitatively investigate the high-level injection effect on the positive-feedback regeneration of CMOS latchup, the trigger current of  $I_1 = 5$  mA (or  $I_2 = 0.6$  mA) with 10 nS pulse width is applied to the p-n-p-n structure under different  $I_{KF1}$  or  $I_{KF2}$  parameters in BJT's  $Q_1$  and  $Q_2$ . The  $p_{1(\max)}$  and  $t_r$  are used to quantitatively observe the influence of this effect. With a fixed  $I_{KF2}$  of  $4.867 \times 10^{-4}$  and variable  $I_{KF1}$  parameter, the influence of  $I_{KF1}$  on  $p_{1(\max)}$  due to the high-level injection effect of BJT  $Q_1$  in the p-n-p-n structure is shown in Fig. 2(a). In Fig. 2(b),  $I_{KF2}$  is



(a)

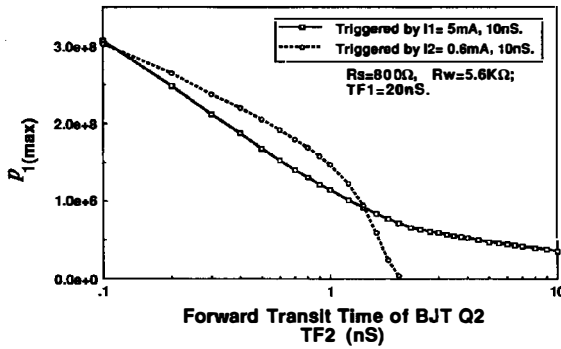


(b)

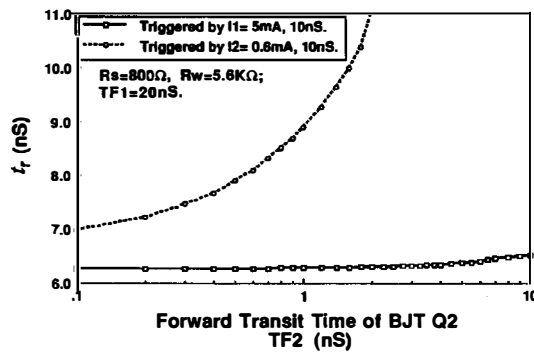
Fig. 7. The influence of the forward transit time  $\tau_{F1}$  of BJT  $Q_1$  on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

a variable but  $I_{KF1}$  is fixed as  $6.909 \times 10^{-4}$  to observe the influence of high-level injection effect in the parasitic vertical BJT  $Q_2$ . The influence of  $I_{KF1}$  or  $I_{KF2}$  on  $t_r$  is shown in Fig. 2(c). From these figures, it can be seen that larger  $I_{KF1}$  and  $I_{KF2}$  parameters, which mean a weaker high-level injection effect, lead to a larger  $p_{1(\max)}$  and a smaller  $t_r$ . The larger  $p_{1(\max)}$  implies a stronger positive-feedback regeneration during latchup transition. The smaller  $t_r$  means that the positive-feedback regeneration occurs more early. Thus, a p-n-p-n structure with larger  $I_{KF1}$  and  $I_{KF2}$  parameters is more sensitive to latchup. The variations of  $p_{1(\max)}$  and  $t_r$  in Fig. 2(a)–(c) are kept very small as  $I_{KF1}$  and  $I_{KF2}$  are greater than about  $1 \times 10^{-2}$ . This implies that the latchup immunity can be improved only when the  $I_{KF1}$  and  $I_{KF2}$  parameters are less than some threshold levels.

The device parameter related to the current gain of a BJT is the ideal maximum forward beta gain denoted as  $\beta_F$  in HSPICE [7]. The influence of the ideal maximum forward beta gain  $\beta_{F1}$  of BJT  $Q_1$  on the positive-feedback regeneration is shown in Fig. 3(a) and (b) with a fixed  $\beta_{F2} = 277.2$ , where  $\beta_{F2}$  is the ideal maximum forward beta gain of BJT  $Q_2$  in the p-n-p-n structure.  $\beta_{F2}$  in submicron CMOS technologies could be in the range about several hundreds, but  $\beta_{F1}$  is only around 1–2. The influence due to  $\beta_{F2}$  variation is shown in Fig. 4(a) and (b) with a fixed  $\beta_{F1} = 1.104$ . As seen in Figs.



(a)



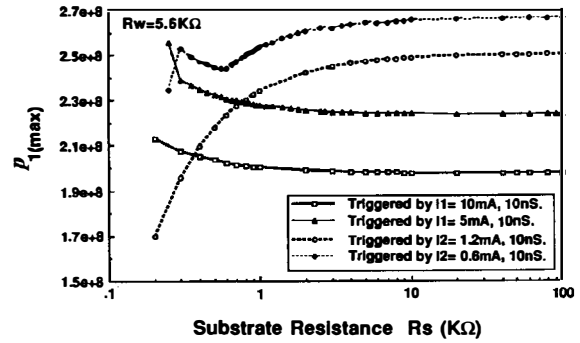
(b)

Fig. 8. The influence of the forward transit time  $\tau_{F2}$  of BJT  $Q_2$  on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

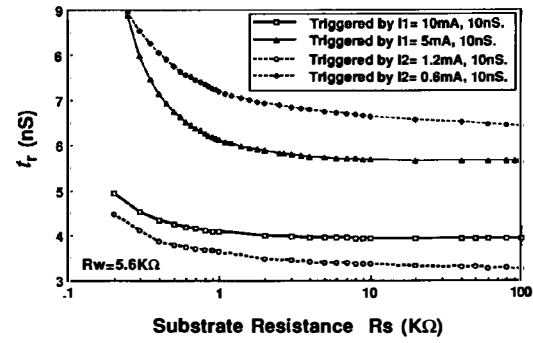
3(a) and 4(a),  $p_{1(\max)}$  has a larger value if the p-n-p-n structure has a larger  $\beta_{F1}$  or  $\beta_{F2}$ . The influence of  $\beta_{F1}$  on  $t_r$  is more sensitive as the p-n-p-n structure is triggered by the substrate current  $I_1$ , but  $t_r$  only varies a little as it is triggered by the well current  $I_2$ . On the contrary, the influence of  $\beta_{F2}$  on  $t_r$  is more sensitive as the p-n-p-n structure is triggered by  $I_2$ , but  $t_r$  only varies a little by the triggering of  $I_1$ . A p-n-p-n structure with larger beta gains generally leads to a larger  $p_{1(\max)}$  but a smaller  $t_r$ , so it is easy triggered into its latching state.

### B. The Influence of Device Capacitance Parameters

The device capacitances have strong relations to the time-varying transient poles [1]. Fig. 5(a) and (b) show the dependence of the positive-feedback regeneration on the zero-biased well-to-substrate junction capacitance in the p-n-p-n structure of CMOS IC's. The well-substrate junction capacitance is the sum of the base-collector junction capacitances in BJT's  $Q_1$  and  $Q_2$ . The  $C_{je1}$  ( $C_{je2}$ ) presents the zero-biased base-collector junction capacitance of BJT  $Q_1$  ( $Q_2$ ). The trigger currents in Fig. 5(a) and (b) are  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with the pulse width of 10 nS. It is shown that a p-n-p-n structure with a larger well-substrate junction capacitance has a smaller  $p_{1(\max)}$  but a larger  $t_r$ . This means that it has a higher latchup immunity against the substrate or well current triggering. This result is quite different to the latchup transition



(a)



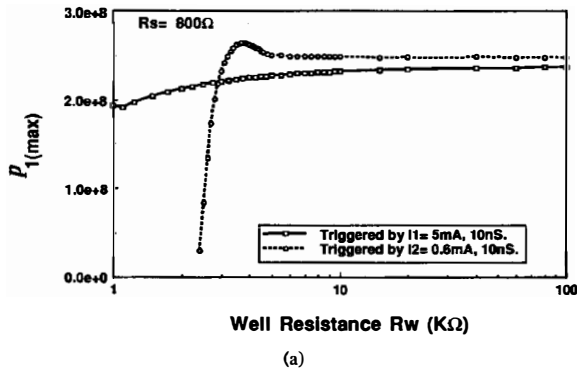
(b)

Fig. 9. The influence of the substrate resistance on (a)  $p_{1(\max)}$  and (b)  $t_r$  due to  $I_1 = 10$  mA or 5 mA and  $I_2 = 1.2$  mA or 0.6 mA triggering with a 10-nS pulse width.

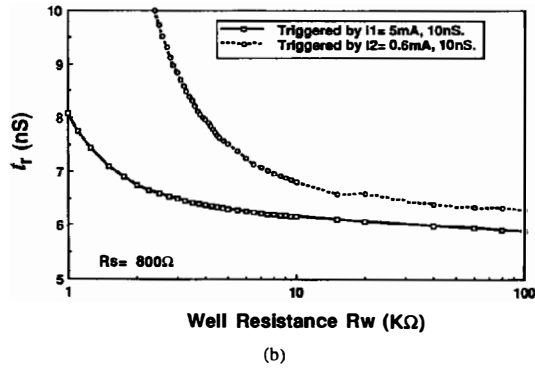
induced by the power-up ramp ( $dV_{DD}/dt$ ) [8]–[10]. There is an anomalous increase in the gradually decreasing curves in Fig. 5(a). This anomalous increase is due to the nonlatchup range with the pulse width of trigger current not longer enough as that in Fig. 1(a). A little anomalous increase due to the same reason also appears in the gradually decreasing curves in Figs. 2(b) and 4(a) under  $I_2 = 0.6$  mA triggering. In the latchup range of Fig. 5(b),  $t_r$  is found to have a nearly linear relation with the well-substrate junction capacitance.

The dependence of base-emitter junction depletion capacitances of BJT  $Q_1$  on the positive-feedback regeneration is shown in Fig. 6(a) and (b), where the  $C_{je1}$  ( $C_{je2}$ ) is the zero-biased base-emitter junction depletion capacitance of BJT  $Q_1$  ( $Q_2$ ). The dependence of  $C_{je2}$  on the  $p_{1(\max)}$  and  $t_r$  is similar to that in Fig. 6(a) and (b). Generally, a larger base-emitter junction capacitance leads to a smaller  $p_{1(\max)}$  but a larger  $t_r$ . A weaker dependence of  $p_{1(\max)}$  on the junction capacitance  $C_{je1}$  due to  $I_1$  triggering and  $C_{je2}$  due to  $I_2$  triggering in the latchup range is observed. The anomalous raise due to nonlatchup condition also appears in the curves due to  $I_2 = 0.6$  mA triggering. It is also found that the dependence of  $t_r$  on the zero-biased base-emitter junction capacitances  $C_{je1}$  and  $C_{je2}$  is nearly linear.

Another important device parameter which also has an obvious contribution on the junction diffusion capacitances is



(a)



(b)

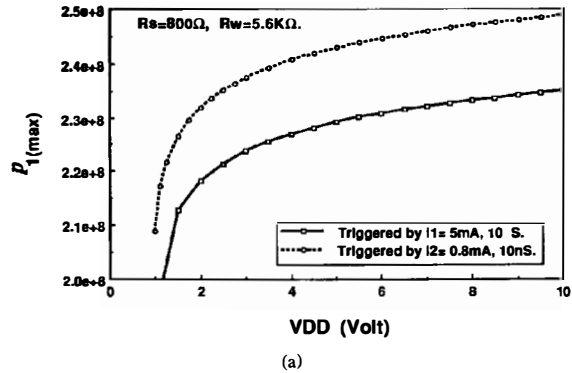
Fig. 10. The influence of the well resistance on (a)  $p_{1(max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.6$  mA with a 10-nS pulse width.

the forward transit time, denoted as  $\tau_F$  [7]. The influence of the forward transit times,  $\tau_{F1}$  and  $\tau_{F2}$ , of BJT's  $Q_1$  and  $Q_2$  on the positive-feedback regeneration are shown in Figs. 7 and 8, respectively. The curves indicate that a p-n-p-n structure with larger forward transit times has a smaller  $p_{1(max)}$  but a larger  $t_r$ . However,  $t_r$  is found to be nearly independent of  $\tau_{F1}$  and  $\tau_{F2}$  in Figs. 7(b) and 8(b) under the triggering of  $I_2 = 0.6$  mA and  $I_1 = 5$  mA, respectively.

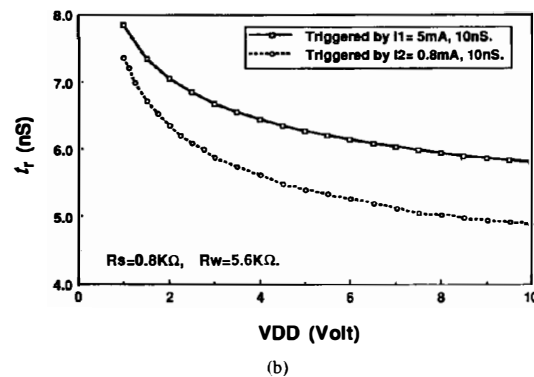
The curves in Figs. 6–8 show that a p-n-p-n structure has higher latchup immunity against the substrate and well current triggering if its base-emitter junction depletion and diffusion capacitances are larger.

### C. The Influences of Device Resistance Parameters

According to (23) of [1], the substrate and well resistances have important effects on CMOS latchup transition. The curves in Figs. 9 and 10 show their effects on the positive-feedback regeneration. In Fig. 9(a),  $p_{1(max)}$  under  $I_1 = 5$  mA or  $I_1 = 10$  mA triggering is slowly decreased as the substrate resistance increases from 0.2 to 3.0 K  $\Omega$ , and then it is held nearly constant as the substrate resistance greater than 3.0 K  $\Omega$ . But,  $p_{1(max)}$  under  $I_2 = 0.6$  mA or  $I_2 = 1.2$  mA triggering continuously increases to its final value as the substrate resistance increases. Although the variation tendency of  $p_{1(max)}$  in Fig. 9(a) due to  $I_1$  and  $I_2$  triggering is different, Fig. 9(b) shows that  $t_r$  decreases as the substrate resistance increases in spite of the trigger current. In Fig. 9(a),



(a)



(b)

Fig. 11. The influence of the power supply  $V_{DD}$  on (a)  $p_{1(max)}$  and (b)  $t_r$  due to the triggering of  $I_1 = 5$  mA or  $I_2 = 0.8$  mA with a 10-nS pulse width.

the nonlatchup condition causes two anomalous increases in the curves of  $p_{1(max)}$  under  $I_2 = 0.6$  mA and  $I_1 = 5$  mA triggering as the substrate resistance is smaller. Similarly, an anomalous increase also appears in Fig. 10(a) because the 10-nS pulse width of the 0.6-mA trigger current  $I_2$  not long enough to cause the occurrence of latchup when the well resistance is less than 5 K  $\Omega$ .

A p-n-p-n structure with larger well or substrate resistances generally has a larger  $p_{1(max)}$  and a smaller  $t_r$  during latchup transition. This causes CMOS latchup more easy to be initiated by the transient-induced current triggering in substrate or well.

### D. The Influence of $V_{DD}$ Power Supply

In above various calculations, the  $V_{DD}$  supply is all set to 5 volts as in the conventional CMOS IC's. The effect of  $V_{DD}$  on the positive-feedback regeneration in a p-n-p-n structure is also investigated and the results are shown in Fig. 11 to observe the influence of the scaled down  $V_{DD}$  on CMOS latchup. The curves show that a lower  $V_{DD}$  supply leads to a smaller  $p_{1(max)}$  and a larger  $t_r$  during latchup transition. Thus, the scaled down  $V_{DD}$  has a benefit to prevent CMOS latchup.

## IV. CONCLUSION

Through the detailed investigations on the variations of device parameters, it is found that a p-n-p-n structure with stronger high-level injection effect, larger well-substrate ca-

capacitance, larger forward transit time, larger base-emitter junction capacitance, but smaller well and substrate resistance, and smaller forward beta gain in the parasitic vertical and lateral BJT's generally has a smaller value of the maximum positive pole and a longer time to initiate the positive pole. Thus, it has higher latchup immunity against transient-induced current triggering in substrate or well of CMOS IC's.

The characterization of the positive-feedback regeneration using the time-varying positive transient pole is useful and convenient in CMOS latchup analysis under any type of triggering. This new developed method is also suitable for transient analysis on the turn-on process of thyristors or

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