The State-of-the-Art Mobility Enhancing Schemes for High-Performance Logic CMOS Technologies

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Abstract

In this talk, an overview of the mobility enhancing techniques for high performance/low power CMOS technologies will be introduced first. Three categories of mobility enhancing schemes with global strain, local strain, and hybrid-substrate engineering, will be discussed next. Either nMOSET or pMOSFET has their respective strategies for achieving the best device performance. However, the strain technique has indeed raised reliability issues. Different reliability issues have been observed for different strain technologies. In the past several years, we have paid much more attention on the current performance of these technologies, the device reliability study has not been sufficient in the previous studies. As a consequence, this talk will also address the importance of these mobility enhancing schemes and their impact on the device reliability for advanced CMOS technologies which utilize strain schemes for current enhancement.

1. Introduction

In more recent years, in order to extend the scalability of the sub-100nm CMOS technology, mobility enhancing schemes have aroused much interest. Among these schemes, strained-Si devices [1-2], substrate engineering, and hybrid substrate technology [3-5] have been attractive for high speed and low power logic CMOS technologies. For the strained Si/SiGe devices, it provides a factor of 50% to 100% mobility enhancement over that of bulk devices. The typical mobility enhancement of n-type strained-Si is much larger than that of p-type devices. Therefore, several techniques have been proposed to enhance the pMOSFET reliability, i.e., SiGe S/D [6], the hybrid technology with different substrate orientations for nMOSFET and pMOSFET respectively [5].

In this paper, this talk will address several examples of these mobility enhancing schemes, as well as the challenges of these devices reliability, and the design guidelines for manufacturable CMOS technologies for 65nm and beyond.

2. The Strain-Engineering for Mobility Enhancement

The interest in the strain engineering has been speed-up in recent years as a need in further scaling of CMOS device for high speed and low power applications. In ITRS report 2007 [7] it was pointed out that the strain silicon technology has to enhance the driving current of CMOS devices to 180% ultimately. A typical 3D strain engineering is illustrated in Fig. 1 [8], in which stress can be achieved by channel [2] or substrate engineering[3]. Uniaxial strain can be achieved by trench isolation, silicide, nitride cap layer, and recessed S/D etc [6]. Depending on process types and device structures, these devices exhibit different degrees of mobility enhancement comparing to conventional process/device structures. Table 1 lists various schemes which can be categorized into **global**, **local**, and **hybrid** strains. The **Global** strain is almost biaxial strain, and made by epi-growth strain layer on the substrate. It involves SiGe in most of the cases, and therefore, Ge out-diffusion becomes inevitable [9]. Also, significant dislocation issues are emerged due to a large area strain.

Moreover, this technique has an inherent disadvantage of high manufacturing cost. The **local** strain is usually unaxial strain which is induced through the process. There are many stressors to implement local strain, such as SiGe eS/D, SiC eS/D [10], and capping layer. The most typical process- induced strain is shown in Fig. 2 with a Contact Etch stopped SiN Layer (CSEL) [11, 14], [15] which will greatly enhance the channel mobility. Different from global strain [16], dislocation issues are prevented in the local strain. Finally, it is low cost for manufacturing simplicity. The last one is **hybrid** strain [17]. Hybrid strain involves a combination of nMOSFET and pMOSFET with different mobility enhancement schemes. But it faces the big challenge of complex manufacturing.

3. The Channel Engineering

A most typical example of using Si/SiGe structure is

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shown in Fig. 3 with relaxed SiGe layer grown on Silicon substrate, from which examples of the I-V characteristics are shown in Fig. 5.

The MOSFET with a strained-Si/SiGe channel has been the prime initiative for mobility enhancement schemes. As a result of the lattice mismatch shown in Fig. 4, a Si layer on relaxed SiGe layer is under a tensile strain, which modifies the band structure and enhances carrier transport since this induces a lower effective mass of the carriers. Figs. 5 and 6 show the n-MOSFET and p-MOSFET drain current and mobility, respectively [5]. It shows that Si/SiGe n-MOSFET mobility has been increased 70% over that of bulk device. However, there is one disadvantage of the SiGe strained devices in that p-MOSFET does not get much gain.

Here comes another idea on developing p-MOSFET on (110) substrate [3]. A typical result shown in Fig. 7 reveals that p-MOSFET mobility has been enhanced while we receive a loss of mobility in n-MOSFET [9]. Similar results in their driving currents, Fig. 8. As a result, an idea of the so-called hybrid substrate CMOS technology becomes a more promising technology, Fig. 9, as will be explained in latter section.

For the state-of-the-art design in nMOSFETs, there are some guidelines from our experiences. Fig. 10 shows the I_{on}-I_{off} characteristics of nMOSFETs with various strains. We may categorize all the splits into two groups. The first group is SiGe on substrate devices and CESL capping layer devices with excellent performance up to 34% and 30%, respectively, in comparison of that of bulk devices at the same value of I_{off} for each device. The other group is SiC on S/D devices and SSOI devices, which exhibit good performance around 15% by comparing to bulk devices at the same value of I_{off} for each device.

For the design of pMOSFET, comparisons between the bulk, SiGe on channel (biaxial,) and SiGe on S/D(uniaxail) devices, Fig. 11, have been compared. The I_{on}-I_{off} characteristics of both the splits and control sample are given in Fig. 12 . We can find SiGe on S/D devices exhibit high driving current enhancement comparing to SiGe on the channel with the same value of I_{off}, which is because the stressor of SiGe on S/D devices is closer to channel than that of SiGe on channel devices. The closer the stressor is to the channel, the higher the effect of the strain becomes. Hence, SiGe on S/D devices have higher performance than that of SiGe on channel devices.

4. The Hybrid-Substrate Engineering

In order to maintain a simultaneous current gain in a CMOS technology, we can take advantage of the n-MOSFET on (100) substrate while p-MOSFET is made on (110) substrate. This constitutes the hybrid substrate technology[3] as shown in Fig. 9. Here, p-MOSFET mobility can be more than doubled on (110) Si-substrate with current flow on the (110) direction comparing to that along the (100) direction (Fig. 7). Also, electron mobility is the largest along the (100) direction.

On the contrary, for the substrate engineering with orientations different from (100) substrate, for example, for devices made on (110) substrate, it provides a much larger hole mobility enhancement in pMOSFET, while receives a loss of mobility in nMOSFET [4-5]. Therefore, a hybrid substrate technology is evolved for a need with pMOSFET on (110) substrate and nMOSFET on (100) substrate.

Figs. 7 and 8 show the drain currents and mobilities for both nMOSFET and pMOSFET on (100) and (110) substrates. It reveals that pMOSFET has a 50% enhancement in its mobility using (110) substrate, while nMOSFET mobility is reduced. The result is just the opposite to that of strained-Si devices.

5. The Challenges on Designing Reliable Strained Devices

A. Enhanced Degradations in Strained Si/SiGe Devices

As reported in [8] that a larger enhancement of mobility may adversely degrade the device reliability. As a consequence, it is important to understand the various strain-induced stress effect incurred by different strained techniques. To investigate the degradation effect, the first set of tested devices is the strained-Si/SiGe nMOSFETs in Fig. 13. Figs. 14(a) and (b) show the drain current degradations after FN and HC stress respectively. As we reported in [5], the origin of the drain current degradation is related to the mobility enhancement. And, to further differentiate its degradation mechanisms, the vertical and lateral field effects have been evaluated. Fig. 15 shows the measured ΔI_{CP} for studying the vertical field effect using FN stress. Since ΔI_{CP} is proportional to the generated N_{it}, we do not

see a major difference. However, the comparison for bulk and strained devices under V_G=V_D HC stress (Fig. 16), we have seen a huge difference of ΔI_{CP}, in which lateral field becomes dominant. In other words, the huge degradation in Fig. 14 and the much higher ΔI_{CP} in Fig. 16 are caused by a large impact ionization rate (I_B/I_D) of the strained devices.

In comparison, a second set of nMOSFET devices with tensile-cap, shown in Fig. 17, has a comparable mobility for long channel while an enhanced mobility by the tensile-strain. Similarly, device I_D degradation under FN and HC stress has been compared in Figs. 18 and 19 for the ΔI_{cp} after FN and HC stress respectively. It is noted that the ΔI_{CP} for tensile-Si does not increase as much comparing to the strained-Si/SiGe device (Fig. 16). The reason is attributed to a higher impact ionization rate in tensile-Si devices. Therefore, we see that the tensile-Si shows high drain current enhancement while it shows even smaller HC degradation. This can be explained that a large I_D degradation in strained-Si/SiGe device is attributed to the large mobility enhancement and hence induces large I_B/I_D.

B. Reliability of SiGe-channel and SiGe S/D pMOSFETs

To investigate different strained effect for pMOSFETs, similar experiments have been conducted. Fig. 11 shows a set of devices with SiGe-channel(biaxial) and SiGe S/D(uniaxial). Fig. 12 is Ion-Ioff characteristics of these devices. Figs. 20-22 show that all three devices have about the same ΔI_{cp} after FN stress. Also, results from Figs. 21 to 22 show a comparable ΔI_{cp} for biaxial or uniaxial device after the HC stress. SiGe S/D device shows a little larger I_D degradation. While, as a result of misfit [8] in a biaxial strain, SiGe-channel device generates much larger N_{it} than the SiGe S/D ones.

C. NBTI Improvement for SiGe S/D pMOSFETs

One other issue which is critically important to pMOSFET is the NBTI. As demonstrated in [18], the NBTI effect in a SiGe S/D and SiGe-channel pMOSFET is serious. Also, SiGe S/D uniaxial strain (uniaxial) shows much better NBTI characteristics comparing to SiGe-channel (biaxial) ones. To further improve this S/D strained technology, a recent approach with embedded-diffusion barrier (EDB) SiGe S/D [6], Fig. 23, has been demonstrated with even better NBTI improvement. Results are shown in Fig. 24, in which a large lifetime improvement can be achieved with this EDB structure in SiGe S/D. This is attributed to the prevention of boron diffusion toward the channel through this barrier, such that the embedded SiGe S/D is successful for short channel effect control and high reliability design.

To summarize, although various mobility enhancing schemes have been shown with very good performance in terms of its I_{ON}, I_{OFF}, we still face challenges for a successful applications in terms of the process control, manufacturability, and in particular their reliabilities. For either strained channel or substrate engineering with combination of mobility enhancing schemes, it tends to give a worse reliability for the advanced CMOS devices. Therefore, much effort needs to be done for the understanding of their reliabilities before these strained techniques can be used for manufacturing in high- end CMOS logic applications.

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References

[1] C. H. Ge et al., in ***Tech. Dig. IEDM***, p. 73, 2003.
[2] J. Hoyt et al., in ***Tech. Dig. IEDM***, p. 23, 2002.
[3] M. Yang et al., in ***Tech. Dig. IEDM***, p. 453, 2003.
[4] T. Ghani et al., in ***Tech. Dig. IEDM***, p. 978, 2003.
[5] S. S. Chung et al., ***Symp. on VLSI Tech***., p. 86, 2005.
[6] C. H. Tsai et al., ***Symp. on VLSI Tech***., p. 188, 2006.
[7] Process Integration, Devices, and Structures, in *ITRS*, p. 15, 2007.
[8] H. C.H. Wang et al., in ***Tech. Dig. IEDM***, p. 61, 2003.
[9] S. S. Chung et al., in ***Tech. Dig. IEDM***, p. 567, 2005.
[10] S. Pidin et al., in ***Tech. Dig. IEDM***, p. 209, 2004.
[11] F. Ootsuka et al., in ***Tech. Dig. IEDM***, p. 575, 2000.
[12] K. Rim et al., in ***Symp. on VLSI Tech***., p. 98, 2002.
[13] F Andrieu et al., ***Symp. on VLSI Tech***., p. 50, 2007.
[14] W. -S. Liao et al., EDL, p. 86, 2008.
[15] K. -M. Tan et al., ***Symp. on VLSI Tech***., p. 127, 2007.
[16] J. W. Pan et al., in ***Tech. Dig. IEDM***, p. 461, 2006.
[17] S. Pidino et al., in ***Tech. Dig. IEDM***, p. 213, 2004.
[18] S. S. Chung et al., ***Tech. Dig. IEDM***, p. 325, 2006.

	nMOSFET				pMOSFET				Hybrid
Strain Direction	Uniaxial		Biaxial		Uniaxial			Biaxial	
Strain scheme	CESL	SiC on S/D FinFET	Relaxed SiGe sub	SSOI	SiGe on S/D +EDB	CESL	Diamond -like carbon cap	SiGe-channel + cap	T-CESL for nFET C-CESL for pFET
ΔI_{on}(%)	+12	+30	+13	+18	+25	+14	+69	+80	nFET• 60% pFET• 55%
Lg(nm)	37	25	60	25	45	60	70		40
EOT(A°)	18.8	20	22	17.5 (TiN/HfO_2)		14			
Ref.	[11]	[10]	[12]	[13]	[6]	[14]	[15]	[16]	[17]

Table 1 Summary of various typical strain techniques and the device performance.

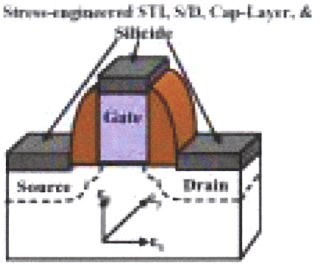


Fig. 1 Several different approaches to enhance the mobility of CMOS devices. [1]

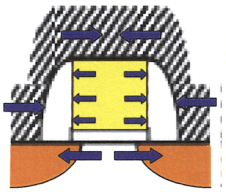


Fig. 2 Several different approaches to enhance the mobility of CMOS devices. [11]

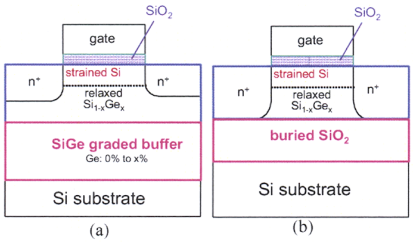


Fig. 3 (a) The strained Si/SiGe structure on bulk-Si substrate and (b) the strained Si/SiGe on SOI substrate.

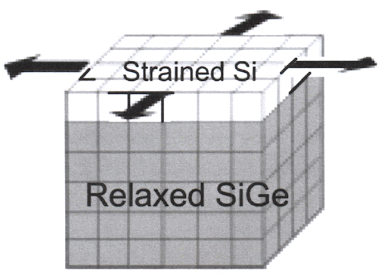


Fig. 4 A strained-Si layer on top of SiGe showing the biaxial strain.

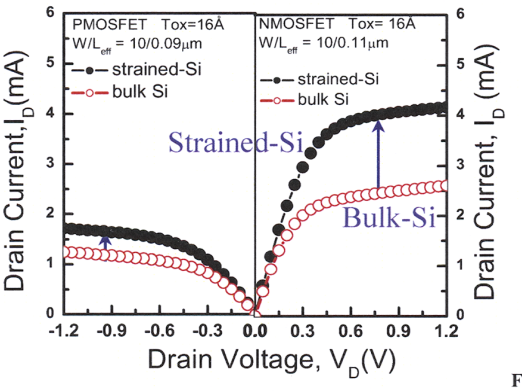


Fig. 5 Comparison of the I_D current for strained-Si and bulk-Si devices, (left) p-MOSFET (right) n-MOSFET.

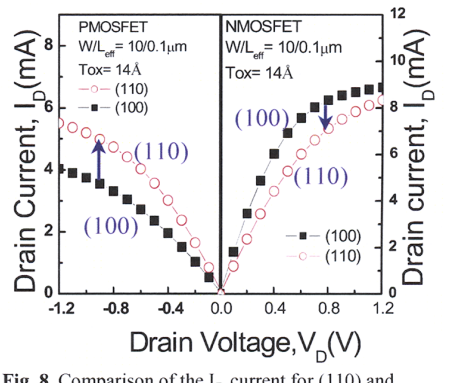


Fig. 8 Comparison of the I_D current for (110) and (100) substrate p-MOSFET (left) n-MOSFET (right).

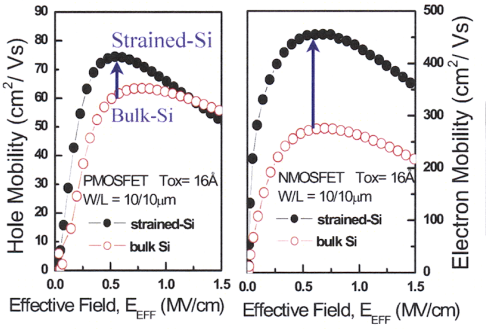


Fig. 6 Comparison of the mobility for strained-Si and bulk-Si devices, (left) p-MOSFET, (right) n-MOSFET.

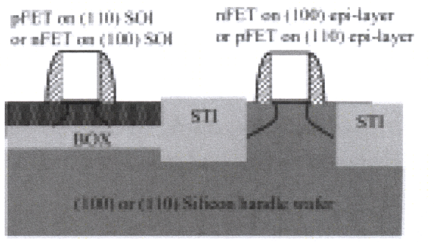


Fig. 9 The concept of hybrid substrate engineering with pMOSFET on (110) substrate while nMOSFET is on (100) substrate. [3]

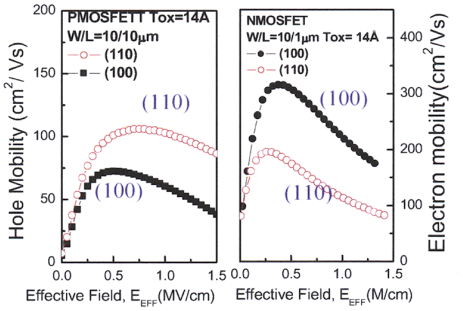


Fig. 7 Comparison of the mobility for (110)and (100) substrate devices, p-MOSFET (left) and n-MOSFET (right).

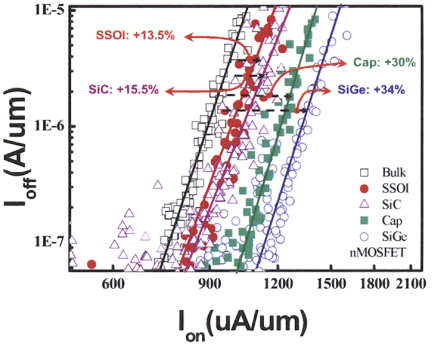
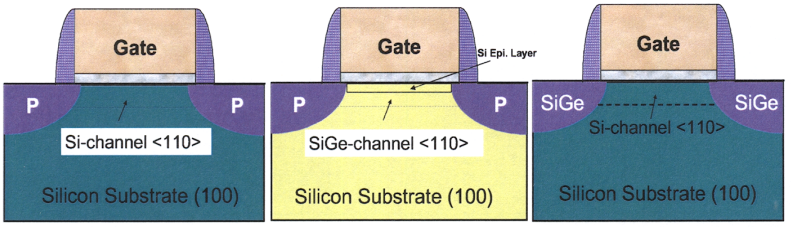


Fig. 10 Comparison of the Ion-Ioff current enhancements for nMOSFETs with various strains.



(a) Control (b) SiGe-channel (c) SiGe S/D

Fig. 11 The cross-sectional view of (a) bulk-Si device and (b) SiGe-channel, and (c) SiGe Source/drain compressively strained pMOSFETs.

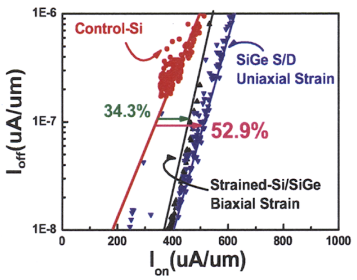


Fig. 12 Comparison of the Ion-Ioff current enhancements for pMOSFETs shown in Fig. 14. Note that SiGe S/D structure (uniaxial) exhibits a largest Ion current enhancement.

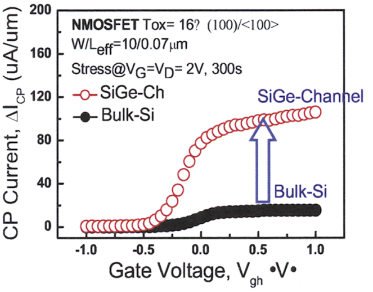
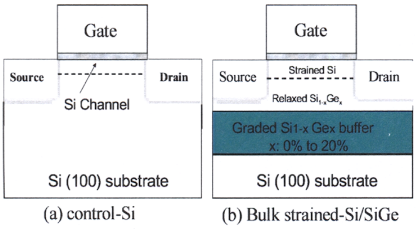
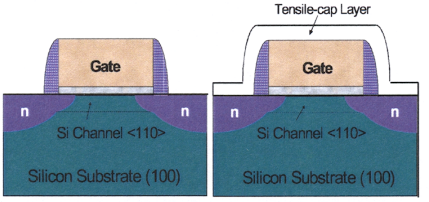


Fig. 16 Comparison of the ΔIcp after HC stress for the devices in Fig. 3. Note the ΔIcp for strained-Si/SiGe is greatly enhanced comparing to FN stress in Fig. 5.



(a) control-Si (b) Bulk strained-Si/SiGe

Fig. 13 The cross-sectional view of the experimental bulk-Si and biaxial strained-Si/SiGe devices.



(a) Control-Si (b) Si-channel w/Tensile-cap

Fig. 17 The cross-sectional view of (a) bulk-Si device and (b) bulk-Si channel with tensile-cap layer.

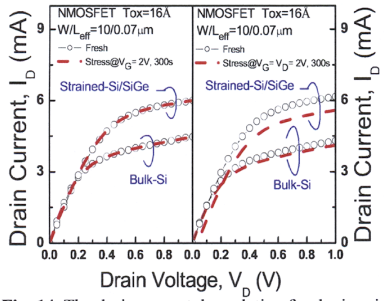


Fig. 14 The drain current degradation for devices in Fig. 13 under FN(left) and HC(right) stresses. Strained-Si/SiGe device exhibits a larger I_D degradation after HC stress.

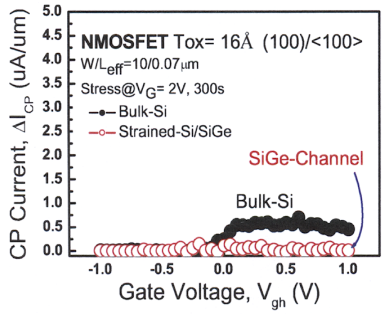


Fig. 15 Comparison of the ΔIcp after FN stress. Note that the enhancement of ΔIcp is very close for strained-Si/SiGe and bulk-Si of n-MOSFET devices.

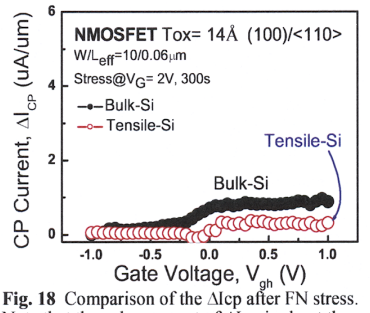


Fig. 18 Comparison of the ΔIcp after FN stress. Note that the enhancement of ΔIcp is about the same for tensile-Si and bulk-Si of nMOSFET devices.

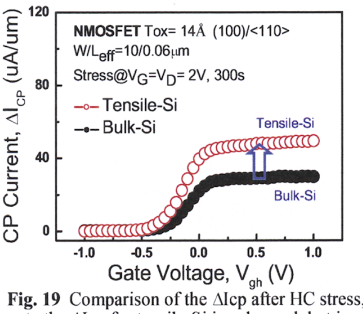


Fig. 19 Comparison of the ΔIcp after HC stress, note the ΔIcp for tensile-Si is enhanced, but is not so huge, comparing to Fig. 6, in the case of strained-Si/SiGe devices.

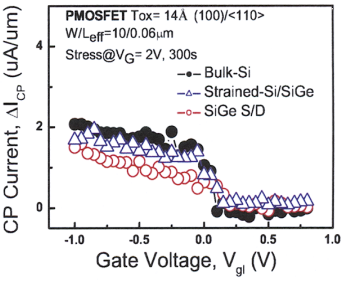


Fig. 20 Comparison of the ΔIcp after FN stress. Note that the enhancement of ΔIcp is about the same for three devices given in Fig. 11.

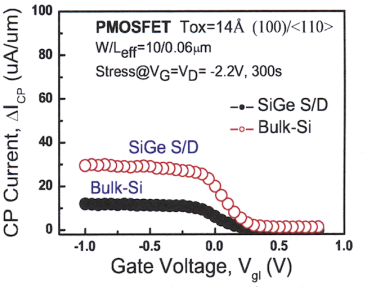


Fig. 21 Comparison of the ΔIcp after HC stress, for SiGe S/D device in Fig. 11, where ΔIcp is a little smaller than SiGe-channel device in Fig. 22.

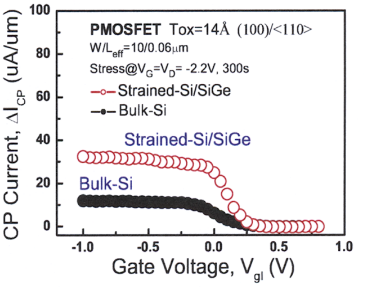
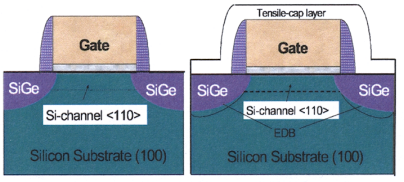


Fig. 22 Comparison of the ΔIcp after HC stress. Note the ΔIcp for SiGe-channel device in Fig. 11, the enhanced I_D degradation is caused by a large impact ionization rate.



(a) SiGe S/D w/o EDB (b) SiGe S/D w/EDB

Fig. 23 The cross-sectional view of (a) SiGe-S/D and (b) SiGe S/D with embedded barrier for S/D region [6].

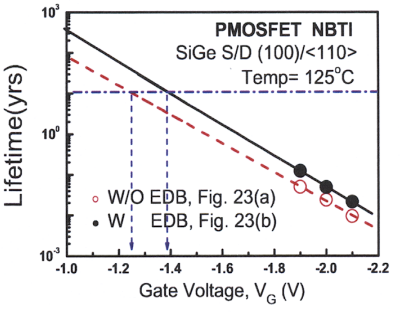


Fig. 24 Comparison of the NBTI degradations for the devices given in Fig. 23. The lifetime measurement based on NBTI for devices in Fig. 23, the SiGe S/D with embedded barrier shows a much better NBTI improvement.