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A New Profiling Technique for Characterizing Hot Carrier Induced Oxide Damages in LDD n-MOSFET's

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Abstract - Previous studies showed that simultaneous determination of the interface states (N_{it}) and oxide-trapped charges (Q_{ox}) in the vicinity of drain side of MOS devices are rather difficult. A new technique which allows the simultaneous characterization of the spatial distributions of both N_{it} and Q_{ox} will be presented. Submicron LDD n-MOS devices were tested and charge pumping (CP) measurements were performed. The spatial distributions of both N_{it} and Q_{ox} have been justified by 2-D device simulation results. Results show that simulated drain current characteristics compare well with experimental data. Moreover, results show that fixed-oxide charge effect is less pronounced to the device degradation in LDD n-MOS devices.

1. INTRODUCTION

Hot carrier effect and the associated device or circuit degradation are increasingly important in the VLSI/ULSI reliability issue. This hot-carrier-induced phenomenon constitute a threat to the long-term reliability of such devices in that the injected carriers may lead to both oxide trapped charges (Q_{ox}) in the oxide and the formation of interface states (N_{it}) at the Si-SiO_2 interface [1]. Recently, the charge pumping technique [2,3] has been proven to be a powerful method for the analysis of the interface properties of the silicon/silicon dioxide system. So far, however, it has been very difficult for simultaneous determination of the spatial distributions of both N_{it} and Q_{ox}.

In this paper, a new characterization technique which allows the simultaneous characterization of the spatial distributions of both N_{it} and Q_{ox} will be presented. It was based on a conventional charge pumping measurement and a new characterization algorithm. For detailed illustration and experimental verification, we will apply this new technique to LDD n-MOSFET's as an example. Finally, these extracted $N_{it}(x)$ and $Q_{ox}(x)$ will be incorporated in a 2-D device simulator to justify the validity of the proposed method.

2. DESCRIPTION OF A NEW METHOD FOR DETERMINING $N_{it}(x)$ AND $Q_{ox}(x)$

In this study, first we propose an algorithm to determine $N_{it}(x)$ and $Q_{ox}(x)$, respectively, from the CP measured results, see Fig. 1. Based on the experimental results I_{cp}-V_{gh} and I_{cp}-V_{gl}, we can calculate the virginal local threshold and flatband voltages respectively by assuming the symmetrically identical nature of source and drain sides, and the uniform N_{it} distribution in the initial samples (i.e., I_{cp}-V_{gh} and I_{cp}-V_{gl} relationships can be transformed into$V_{t,vir}(x)$-x and $V_{fb,vir}(x)$-x) [3]. Table 1 shows the equations for determining both N_{it} and Q_{ox}. Now, by assuming a $V_{t,str}(x)$ curve as formulated in Eq. (1a) (Table 1), for the device after stress, the post-stress local threshold voltage can be uniquely determined once A is known

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from Eq. (2). This A value can be determined by an optimization procedure [6]. Fig. 2 shows the schematic diagram of an LDD n-MOSFET's and the corresponding notations in Table 1. Through the minimization of $N_{it,vgh}(x)$ and $N_{it,vgl}(x)$ [6], $N_{it}(x)$ can thus be determined from Eq. (3). In addition, due to the 2-D fringing effect at the gate-drain edge in the spacer region, capacitances $C_{ox,cp}(x)$ instead of C_{ox} should be used in calculating Q_{ox}. This nonlinear capacitance can be obtained using device simulator. Therefore, $Q_{ox}(x)$ can be extracted from the discrepancy between $V_{t,str}(x)$ and $V_{t,vir}(x)$ by Eq. (4a). Finally, simulation will be used to justify the validity of the extracted $Q_{ox}(x)$ and $N_{it}(x)$ from a comparison of the I-V characteristics between simulated and experimental results.

3. EXPERIMENTAL RESULTS

The LDD n-MOSFET's samples were fabricated using a poly-Si gate twin-well 0.7μm CMOS process. In our experiment, we used Minimos 4 to simulate the majority-carrier distribution to define the effective channel length L_{eff} that contributed to charge pumping current. During the charge pumping measurements, 1-MHz pulse waves with rise/fall times of 200ns were used, and the high and base levels (V_{gh} and V_{gl}) of the gate pulse were fixed at +5 and -5V, respectively. It is noted that the drain and source biases were held constant at zero to avoid the changes of $V_t(x)$ and $V_{fb}(x)$ during the inversion and accumulation half cycles as demonstrated by Ma et al. in [2].

Fig. 3 shows I_{cp}'s for an n-channel LDD MOSFET's before and after 10^4 seconds of DC hot-carrier stress at V_{DS} = 7V and V_{GS} = 3V when V_{gh} is swung with V_{gl} constant and V_{gl} swung with V_{gh} constant, respectively. As illustrated in [3], we can directly obtain the local $V_{t,vir}(x)$ and $V_{fb,vir}(x)$ distributions along the channel for a virginal device (i.e., before stress) in Fig. 4. With the aid of Minimos 4, we can further determine the covering channel end, especially the drain side, which contributes to the charge pumping current. In this case, the channel end-point, that can be detected with charge pumping method, is at 0.745-μm while V_{gl} is held at -5V. Usually, the range of damaged region is less than 0.1-μm and the damage profile is also well correlated with the lateral electric field peak as in [5]. Values of the optimized A and B are determined from Eq. (2). As long as A and B are known, $V_{t,str}(x)$ and $V_{fb,str}(x)$ can be calculated as shown in Fig. 4. Before determining the effective densities of oxide trapped charges, we should first calculate $C_{ox,cp}(x)$ to incorporate the fringing effect, as shown in Fig. 5. Thus, $Q_{ox}(x)$ and $N_{it}(x)$ can be easily profiled as shown in Fig. 6. Simulation results also show that the maximum electric field is located at 0.706-μm under the stress bias condition of V_{DS} = 7V and V_{GS} = 3V.

To verify the validity of the characterized $Q_{ox}(x)$ and $N_{it}(x)$, device simulator Minimos 4 has been used by incorporating $Q_{ox}(x)$ and $N_{it}(x)$. The simulated and measured drain current characteristics are compared in Figs. 7 and 8 respectively and very good agreements can be achieved.

In summary, in this paper charge pumping technique has been applied to the characterization of localized oxide damages in LDD n-MOS devices. In particular, a new method has been developed in which both the spatial distributions of interface states $N_{it}(x)$ and oxide-trapped charges $Q_{ox}(x)$ can be derived. By incorporating the spatial distribution of $N_{it}(x)$ and $Q_{ox}(x)$ into 2-D simulations, predictions of I-V characteristics for degraded devices can be achieved. The developed technique is expected to be useful for drain-engineered design in the submicron or even deep-submicron MOS VLSI/ULSI device technology.

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$$V_{t,str}(x) = B \cdot \ln\left(1 - \frac{x - x_1}{A}\right) + V_{t,vir}(x_1), \quad (1a)$$

where

$$B = \frac{V_{t,vir}(x_2) - V_{t,vir}(x_1)}{\ln\left(1 - \frac{x_2 - x_1}{A}\right)}. \quad (1b)$$

$$\min\left[\sum_x \left|N_{it,vgh}(x) - N_{it,vgl}(x)\right|\right]. \quad (2)$$

[6]

$$N_{it}(x) = N_{it,vgh}(x)|_A. \quad (3)$$

$$Q_{ox}(x) = C_{ox,cp}(x)(V_{t,str}(x) - V_{t,vir}(x)) \quad (4a)$$

where

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}. \quad (4b)$$

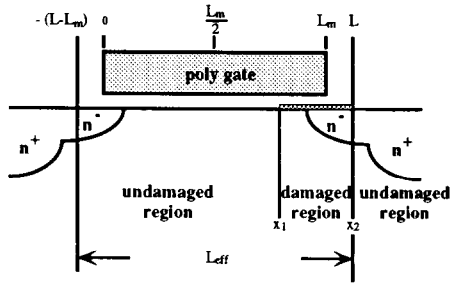

Fig. 1 Characterization algorithm for $N_{it}(x)$ and $Q_{ox}(x)$.

Table 1 Equations for determining N_{it} and Q_{ox}.

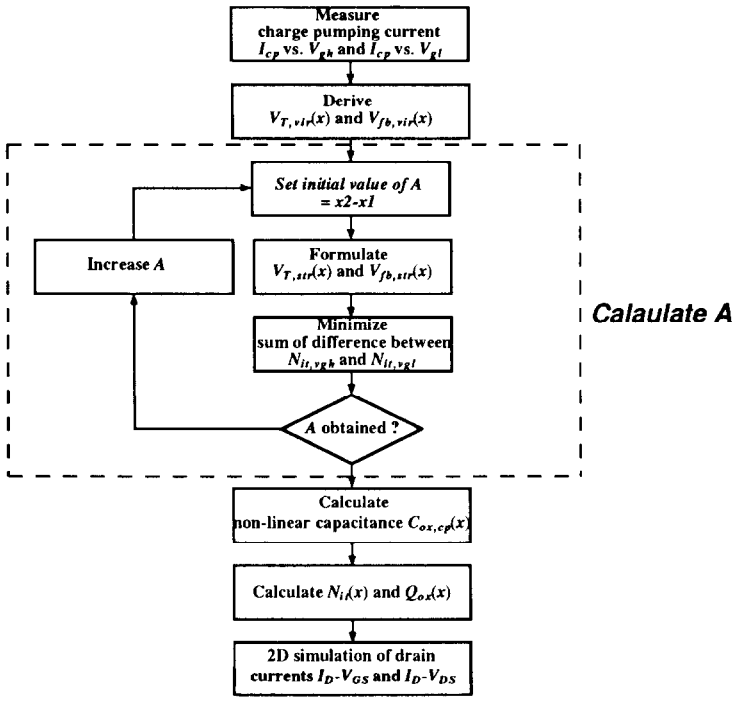

Fig.2 The schematic diagram of an LDD nMOSFET's and the corresponding notations in Table 1.

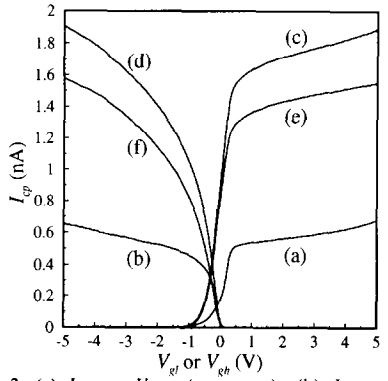

Fig.3 (a) I_{cp} vs. V_{gh} (pre-stress), (b) I_{cp} vs. V_{gl} (pre-stress), (c) I_{cp} vs. V_{gh} (post-stress), (d) I_{cp} vs. V_{gl} (post-stress), (e) $I_{cp,d}$ vs. V_{gh} (post-stress) and (f) $I_{cp,d}$ vs. V_{gl} (post-stress) curves of a 0.7 μm LDD nMOSFET's with stress condition at V_{DS}=7V, V_{GS}=3V, measured at zero drain bias.

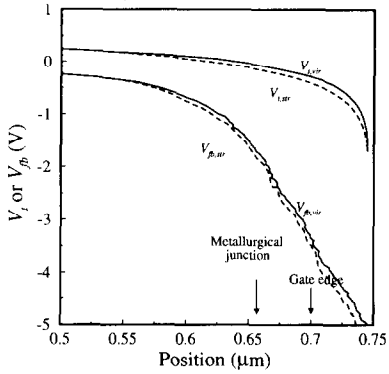

Fig.4 Calculated local threshold $V_{t,vir}(x)$ ($V_{t,str}(x)$) and flatband $V_{fb,vir}(x)$ ($V_{fb,str}(x)$) voltage distributions along channel before and after DC stresses.

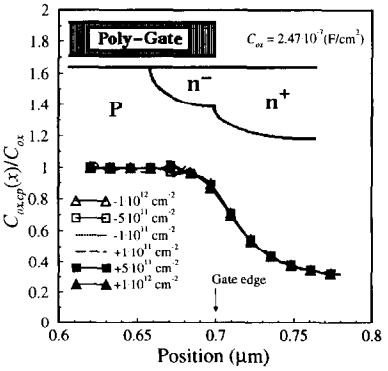

Fig.5 Modified gate-oxide capacitance (normalized) versus position for calculating $Q_{ox}(x)$.

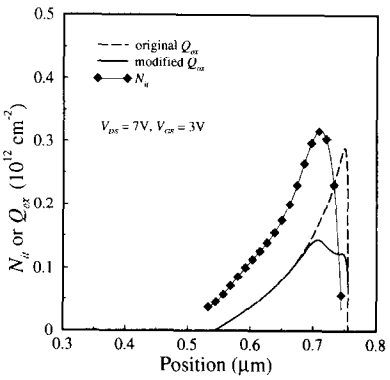

Fig.6 Lateral distributions of $Q_{ox}(x)$ obtained from original C_{ox} and modified $C_{ox,cp}(x)$ respectively. Lateral distributions of $N_{it}(x)$ are also shown.

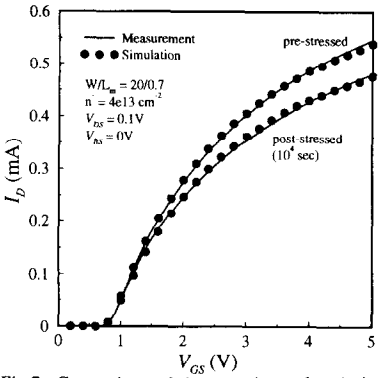

Fig.7 Comparison of the experimental and simulated I_D characteristics for fresh and stressed devices.

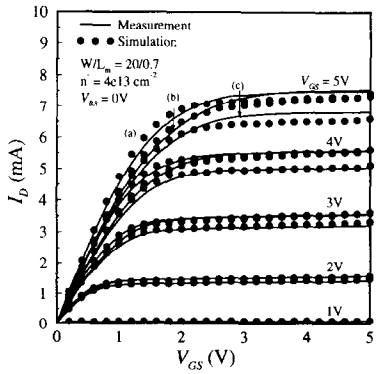

Fig.8 Comparison of the experimental and simulated I_D characteristics for fresh and stressed devices. The results for pre-stress characteristic are denoted by (a) and the results for post-stress forward (b) and reverse (c) characteristics are also shown.