Solid-State Electronics 64 (2011) 6–9

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Reduced leakage current of nickel induced crystallization poly-Si TFTs by a simple chemical oxide layer

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ARTICLE INFO

Article history:
Received 1 December 2010
Received in revised form 17 May 2011
Accepted 3 July 2011
Available online 2 August 2011

The review of this paper was arranged by Y. Kuk

Keywords:
Metal-induced crystallization (MIC)
Thin film transistors (TFTs)
Chemical oxide
Leakage current
Poly-Si

ABSTRACT

Ni-metal-induced crystallization (MIC) of amorphous Si (α-Si) has been used to fabricate low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs). However, the leakage current of MIC-TFT is high. In this study, a chemical oxide layer was used to avoid excess of Ni atoms into α-Si layer during MIC process, which was simple and without extra expensive instrument. The minimum leakage current and on/off current ratio were significantly improved.

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1. Introduction

Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have attracted considerable interest for high resolution integrated active-matrix organic light-emitting diodes (AMOLED) because they exhibit good electrical properties and can be used in the realization of system-on-glass (SOG) [1]. In various technologies for achieving large-area poly-Si, metal-induced crystallization (MIC) has potential due to low cost, good uniformity, low crystallization temperature (~500 °C) and short crystallization time (0.5–5 h) [2,3]. However, the leakage current of MIC-TFT is high. This is because Ni residues in the poly-Si film increase the leakage current and shift the threshold voltage [4,5]. The Ni residues could be reduced by gettering method or metal diffusion filter layer (MICC). Gettering method was an efficient technology to capture Ni residues from poly-Si, but the process was complex and the on current of poly-Si films decreased [6]. MICC used a SiNx cap layer to reduce Ni diffusion into poly-Si film, however that still needed high temperature and long annealing time, and the Ni degree of reduction is not conspicuous [7,8]. Besides, these two methods need extra expensive and complicated vacuum instrument.

In this letter, a simple chemical oxide layer was introduced between α-Si layer and Ni layer to avoid excess of Ni atoms into α-Si layer during MIC process. It was found that the minimum leakage current of poly-Si TFT was greatly reduced. The manufacture processes were very simple and without extra expensive instrument.

2. Experimental

N-channel poly-Si TFTs were investigated in this study. A 100-nm-thick undoped α-Si layer was deposited onto a 500-nm-thick oxide-coated Si wafer by low pressure chemical vapor deposition (LPCVD) system. To form chemical oxide MIC poly-Si (CF-MIC), samples were dipped into a chemical solution of $3H_2SO_4$:$1H_2O_2$ for 20 min to form a chemical oxide filter layer on the top of α-Si. The transmission electronic microscopy (TEM) cross-section image of chemical oxide layer was shown in Fig. 1. To examine the quality of chem-SiO_2, after the chem-SiO_2 layer was formed, platinum was deposited on top of the chem-SiO_2 for image contrast in TEM sample preparation. A 5-nm-thick Ni film was then deposited and subsequently annealed at 500 °C for 1 h in N_2 for crystallization of α-Si. The unreacted Ni film and chemical oxide layer were then removed by wet etching.

The islands of poly-Si regions on the wafers were defined by Reactive ion etching (RIE). After cleaning process, a 100-nm-thick tetraethylorthosilicate/O_2 (TEOS) oxide layer was deposited as the gate insulator by plasma-enhanced chemical vapor deposition (PECVD). Then a 100-nm-thick poly-Si film was deposited as the gate electrode by LPCVD. After defining the gate, self-aligned

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doi:10.1016/j.sse.2011.07.002

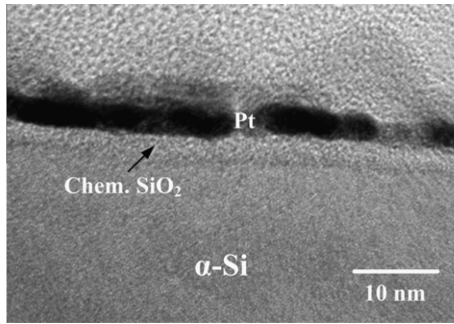

Fig. 1. TEM cross-section image of chemical oxide layer. Platinum film deposited on the top of the chem-SiO_2 layer was for the TEM sample preparation.

35 keV phosphorous ions were implanted at a dose of $5 \times 10^{15}\ cm^{-2}$ to form the source/drain and gate. The dopant activation was performed at 600 °C for 24 h. A 500-nm-thick TEOS oxide layer was deposited as the passivation layer by PECVD, followed by a definition of contact holes. A 500-nm-thick Al layer was then deposited by thermal evaporation and patterned as the electrode. Finally, sintering process was performed at 400 °C for 30 min in N_2 ambient.

It is worthy to note that this CF-MIC process does not need any additional annealing step and expensive vacuum equipment, and is compatible with conventional MIC processes.

For the purpose of comparison, solid phase crystallization (SPC) TFT, and conventional MIC TFT without chemical oxide layer were also fabricated under the same conditions.

3. Results and discussion

A relation of chemical oxide thickness, as investigated/measured by TEM, versus immersed time is shown in Fig. 2. It was found that oxide thickness increased with immersed time and saturated around 3.4 nm when the time reached 10 min. This is because the chemical oxide growth was controlled by diffusion of reactants through the pre-existing oxide layer [9]. Since oxide thickness was saturated when time reached 10 min, in this work, 20 min was chosen as the immersed time to gain stable oxide thickness.

Fig. 3 shows X-ray photoelectron spectroscopy (XPS) of Si2p peak for the chemical oxide on top of α-Si layer. By fitting, it was observed Si, SiO and SiO_2 peaks are located at binding energy of 99.6, 101.7 and 103.2 eV, respectively [10–12]. We believe that the signal of Si peak was from the bottom layer (α-Si) because

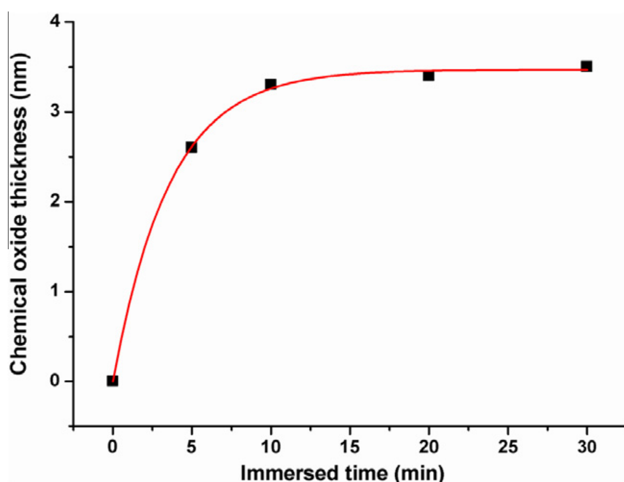

Fig. 2. Formation thickness of chemical oxide versus immersed time.

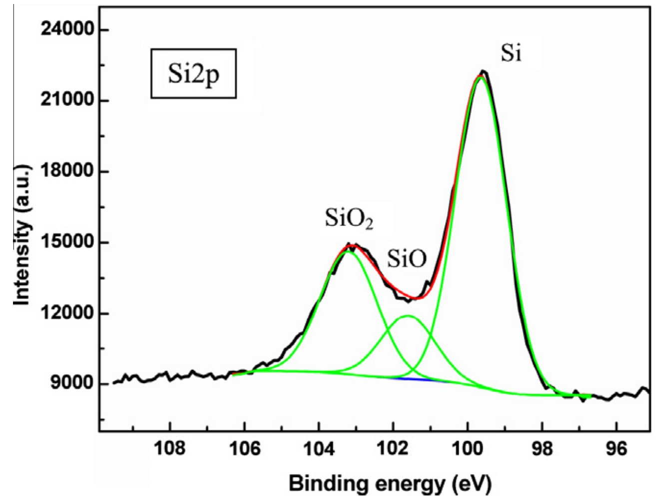

Fig. 3. X-ray photoelectron spectroscopy (XPS) of Si2p peak for the chemical oxide on top of α-Si layer.

the thickness of chemical oxide layer is less than XPS sampling depth. In other words, the chemical oxide was composed of SiO and SiO_2.

To investigate the effect of chemical oxide on the reduction of Ni residues, samples were purposely dipped into a silicide-etching solution (HNO_3:NH_4F:H_2O = 4:1:50) after unreacted Ni film and chemical oxide layer were removed. As shown in Fig. 4, numerous holes were observed. These holes were residues of Ni silicides that had been etched away by the silicide-etching solution. The Ni residues in CF-MIC were much lower than those in conventional MIC. This reduction must be due to the introduction of chemical oxide layer in CF-MIC processes. Oxide filter layer can avoid Ni directly contact with α-Si and remove unreacted Ni easily from surface.

Secondary-ion mass spectroscopy (SIMS) depth profile was also used to analyze the Ni concentrations (residues) in Si films (without silicide-etching process). As expected, Ni content in CF-MIC was much less than that in MIC as shown in Fig. 5. Obviously, chemical oxide layer can reduce the Ni concentrations in Si films. This is because the diffusivity of Ni in α-Si is 10^8 times higher than that in SiO_2 at 500 °C [13,14]. As a result, chemical oxide as a filter, which can retard the in-diffusion of Ni into Si. In other words, Ni concentrations in Si films were reduced.

The effect of immersed time on the reduction of Ni concentration is shown in Fig. 6. The Ni concentration, as estimated by Ni intensity at 50 nm deep, was found to decrease with the increasing of immersed time and then saturate after 10 min. This is because in CF-MIC process, Ni need diffuse through oxide layer to crystallize α-Si. As shown in Fig. 2, oxide thickness increased with immersed time. Therefore, the Ni concentration decrease with immersed time

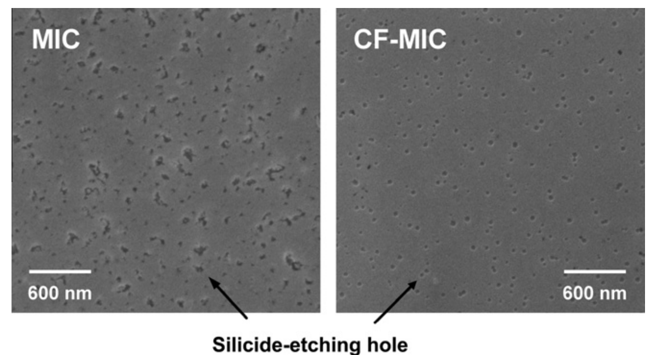

Fig. 4. SEM of the silicide etching holes after metal induced crystallization of poly-Si with and without chemical oxide layer.

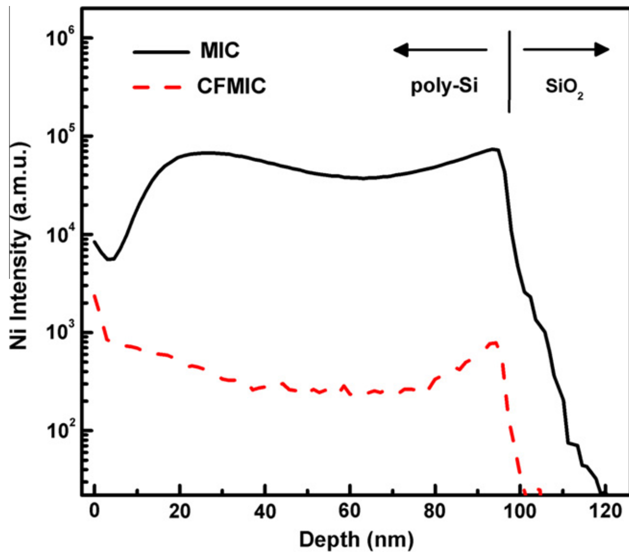

Fig. 5. SIMS depth profiles of nickel and in the structure of poly-Si film after MIC process.

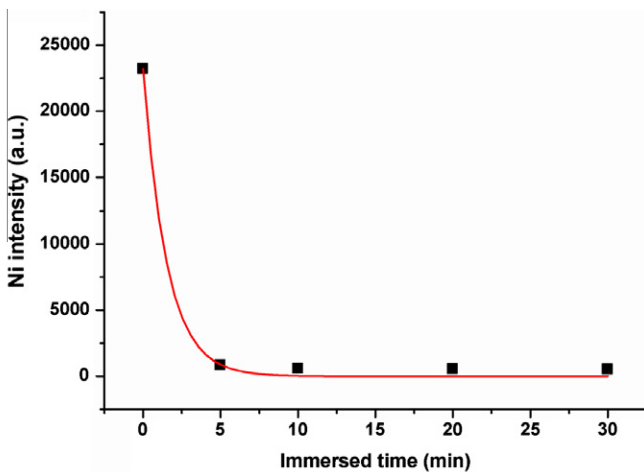

Fig. 6. A relation of Ni intensity at a depth of 50 nm versus immersed time by SIMS after MIC annealing.

and then saturated after 10 min. In this study, to gain stable oxide thickness/device performance, only 20 min was chosen as the immersed time to fabricate devices.

After Ni film and chemical oxide were removed, their surfaces (without silicide-etching) were measured using atomic force microscopy (AFM) to identify the degree of texturing. The root mean square surface (rms) roughness of CF-MIC surface (0.798 nm) was less than that of CF-MIC surface (1.348 nm). These results are in agreement with the MICC studies of Choi et al. [8], who found that MIC with cap layer can achieve a clean and smooth surface.

Finally, Fig. 7 exhibits the I_D–V_G transfer characteristics of TFTs at a drain bias of 5 V. The device parameters were extracted at W/L = 10/10 μm, and 10 TFTs were measured. The average values with standard deviations in parentheses were shown in Table 1. The threshold voltage (V_{th}) is defined at a normalized drain current of $I_{DS} = (W/L) \times 100$ nA at V_{DS} = 5 V. The field-effect mobility (μ_{FE}) is extracted from the maximum value of transconductance at V_{DS} = 0.1 V. As shown in Table 1, the electrical characters of CF-MIC TFTs were significantly improved. This improvement must be due to the introduction of chemical oxide layer in CF-MIC

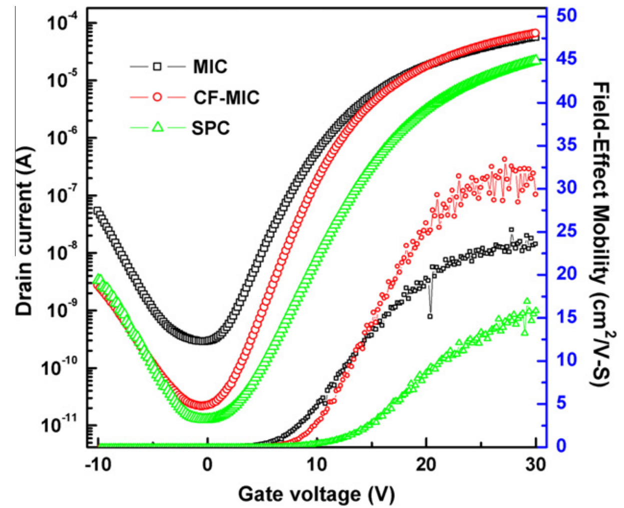

Fig. 7. Typical I_{DS}–V_{GS} transfer characteristics of conventional MIC, CF-MIC and SPC (W/L = 10/10 μm).

Table 1
Average device characteristics of MIC, CF-MIC and SPC with standard deviations in parentheses.

W/L = 10/10 μm	MIC	CF-MIC	SPC
μ_{FE} (cm^2/V-S)	25.5 (2.39)	35.8 (2.65)	17.0 (1.26)
V_{th} (V)	7.11 (0.81)	8.73 (0.88)	13.02 (0.18)
S.S (V/decade)	1.86 (0.14)	1.81 (0.12)	1.83 (0.14)
Imin (pA/μm)	30.00 (3.71)	2.10 (0.12)	1.26 (0.08)
Max on/off ratio (10_5)	2.08 (0.48)	35.98 (5.21)	18.67 (1.18)

processes. Compared with conventional MIC TFTs, CF-MIC TFTs shows a 17.3-fold increase in the on/off current ratio and a 14.3-fold decrease in the minimum leakage current.

The leakage current improvement was attributed to the reduction of Ni concentration in the CF-MIC films. It is known that Ni-related defects might degrade electric performance because the trap states introduced dangling bonds and strain bonds [15]. The chemical oxide layer reduced content of Ni (Ni-related defect) into channel layer during MIC annealing process. With the reduction of the Ni concentration, the minimum leakage current was reduced and therefore the on/off current ratio was increased [16,17]. In addition, the carrier mobility also increased due to lower impurity scattering of Ni-related defects. However, the V_{th} of CF-MIC was showed a positive shift compared with conventional MIC. The result is similar to earlier findings suggesting that the negative shift of V_{th} was caused by positive charge in high Ni residues poly-Si film [6].

The electrical performances of SPC TFT were also measured. As shown in Table 1, Fig. 7, the on/off current ratio of CF-MIC TFT was higher than that of SPC TFT. The leakage current of CF-MIC TFT was as low that of SPC TFT. This also demonstrated the reduction of Ni residues through the introduction of chemical oxide layer.

4. Conclusions

The chemical oxide filter layer was introduced into MIC processes to reduce the leakage current of MIC TFT. The process was very simple and without extra expensive instrument. It just added α-Si coated sample into chemical solution before depositing the Ni film. As a result, the electrical performance of MIC TFTs with chemical oxide layer was significantly improved. Compared with conventional MIC TFT, CF-MIC TFT shows a 14.3-fold decrease in the minimum leakage current and a 17.3-fold increase in the on/off current ratio. This is because the chemical oxide layer can avoid

Ni directly contact with α-Si, avoid excess of Ni atoms into α-Si layer and remove unreacted Ni easily from surface.

Acknowledgements

This Project was funded by Sino American Silicon Products Incorporation and the NSC of the ROC under Grant No. 98-2221-E-009-041-MY3. Technical supports from the National Nano Device Laboratory, Center for Nano Science and Technology and the Nano Facility Center of the National Chiao Tung University are also acknowledged.

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