Effect of Lateral Body Terminal on Silicon–Oxide–Nitride–Oxide–Silicon Thin-Film Transistors

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***Abstract*—We investigate lateral-body-terminal silicon–oxide–nitride–oxide–silicon thin-film transistors (LBT SONOS TFTs) under erasing operation. These devices have superior erasing efficiency by gate as well as lateral body electrode exerting bias. The erasing mechanism of LBT SONOS TFTs has been illustrated by the energy band diagrams. Holes gain sufficient energy by the electric field in the deep-depletion region to surmount the tunneling oxide barrier because of exerting body bias under erasing operation. In addition, the lateral body terminal exerting bias can enhance the erasing efficiency and is confirmed by different erasing conditions and structures. In addition, to verify the hole current injecting from the lateral body site, the size effect of LBT SONOS TFTs is also discussed.**

***Index Terms*—Erasing efficiency, hole injection, silicon–oxide–nitride–oxide–silicon (SONOS), thin-film transistors (TFTs).**

I. Introduction

LOW-TEMPERATURE polysilicon (LTPS) thin-film transistors (TFTs) have been adopted in flat-panel displays, including active-matrix liquid-crystal displays and active-matrix organic light-emitting diode displays [1]. The major advantage of LTPS TFTs is its suitability for multifunctional active-matrix displays because it can integrate sensor, controller [2], and memory [3] into a panel for system-on-panel (SOP) applications. Silicon–oxide–nitride–oxide–silicon (SONOS)-type TFTs serving as nonvolatile memory by embedding a trapping layer into the gate oxide of the transistor have been proposed for SOP applications because their processes are simple and fully compatible with the poly-Si TFT process [4]–[8]. The read principle of the SONOS memory device is by measuring the corresponding current between the programming and erasing states and identifying the distinct status of the memory device [9], [10]. Thus, the memory window, i.e., the threshold-voltage difference between the programming and erasing states, must be large enough to distinguish the status of the memory device. However, traditional SONOS TFTs have poor erasing efficiency. Hole tunneling is forbidden due to the large hole barrier height (> 4 eV) of the oxide, so that the memory window cannot be distinguished clearly [11], [12]. Therefore, a variety of approaches to enhance the erasing efficiency is worthy of study. In this letter, lateral body terminal (LBT) SONOS TFTs are used to enhance the erasing efficiency. These devices have superior erasing efficiency than conventional three-terminal SONOS memory devices. In addition, to confirm the erasing hole current injecting from the lateral body site, we investigate the size effect of LBT SONOS TFTs under erasing operation and explain it with the schematic.

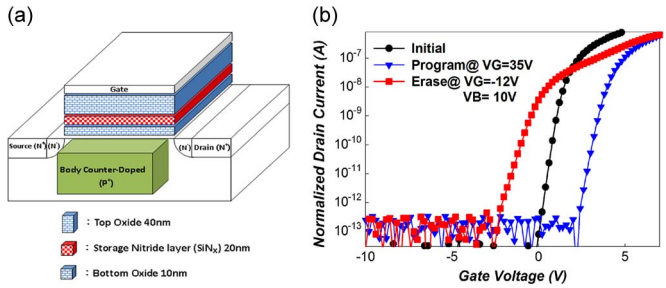

Fig. 1. (a) Schematic cross-sectional view of SONOS TFTs with LBT. (b) Electrical characteristics under the erasing condition with both $V_G = -12$ V and $V_B = 10$ V.

II. Experimental Setup

Fig. 1(a) shows the schematic cross-sectional view of a SONOS-TFT with LBT. The devices used in this letter are n-channel SONOS TFTs with top gate and self-aligned lightly doped drain (LDD) structures fabricated on a Corning 1737 glass substrate. The detailed fabrication procedures are as

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follows. First, a silicon oxide buffer layer and a 50-nm-thick undoped amorphous-Si (a-Si) film were deposited sequentially by plasma-enhanced chemical vapor deposition (PECVD) at 380 °C. Then, the polysilicon channel was formed by a 308-nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2, and a 95% laser overlap ratio was adopted to obtain large grain size and better uniformity of the active layer. The source/drain and LDD region were formed by the mass-separated ion implanter technique. Doping activation was performed at 530 °C/1-h thermal furnace. Next, the multilayer gate dielectric consisting of tunneling oxide (10 nm)/silicon nitride (20 nm)/top oxide (40 nm) (O/N/O) was deposited by PECVD. Then, MoW was sputtered and patterned as a gate metal. The fabrication process of the LBT SONOS-TFT was almost the same as that of the n-channel LTPS SONOS TFT. The p-doped LBT was the only difference. The fabrication process of LBT SONOS TFTs does not need any additional mask step. The body terminal was formed by the mass-separated ion implanter technique, just like the boron doping process of the conventional poly-Si TFT to form the P^+ doping region. The electrical properties of SONOS TFTs with an LDD length of 1 μm were analyzed by using an Agilent B1500A semiconductor device analyzer. Here, the normalized drain current is defined as drain current/(width/length), i.e., $I_D/(W/L)$. The threshold voltage is defined as the voltage, while NI_D reaches 10^{-8} A. All the measurements were taken at 30 °C.

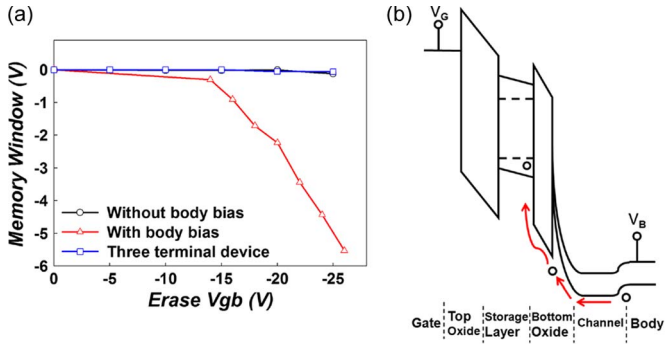

Fig. 2. (a) Memory window characteristics of SONOS TFTs at different erasing conditions and structures. (b) Band diagram at the erasing operation.

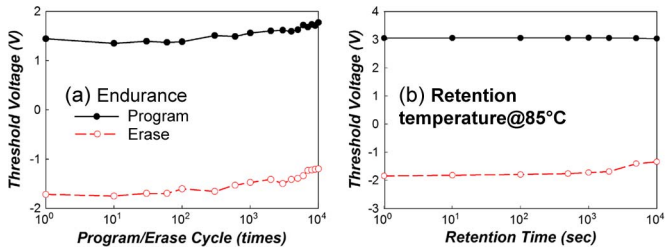

Fig. 3. (a) Endurance characteristics of LBT SONOS TFTs after various numbers of P/E cycles. (b) Retention characteristics of LBT SONOS TFTs measured after various periods, as the devices were heated at 85 °C.

III. Results and Discussion

Fig. 1(b) shows the normalized current–voltage (I–V) characteristics of the LBT SONOS TFT with $W/L = 12/6$ μm under erasing operation. Before the erasing operation, the memory device was programmed by a gate bias of 35 V for 1 s. Thus, electrons were injected from the channel through the tunnel oxide to the nitride layer by Fowler–Nordheim (FN) tunneling because the gate bias induced a high electric field. Then, the device was operating under erasing at a gate bias of -12 V as well as a body bias of 10 V for 1 s. The memory window can attain a threshold-voltage shift of 3.3 V under an erasing $V_{\rm GB}$ of -22 V.

The memory window characteristics of SONOS TFTs at different erasing conditions and structures are shown in Fig. 2(a). The memory window reaches 5.6 V under the LBT SONOS TFT at a gate bias of -16 V as well as a body bias of 10 V for 1 s. However, for the device after the erasing operation at a gate bias of -25 V without body bias, the memory window only reaches 0.55 V of threshold-voltage shift. In addition, compared with traditional three-terminal SONOS TFTs, the erasing efficiency is similar to that of the LBT SONOS TFT under erasing operation without body bias but is significantly poorer than that with body bias. The energy band diagram of the LBT SONOS TFT under erasing operation, as shown in Fig. 2(b), is used to illustrate the better erasing efficiency of LBT SONOS TFTs. Under erasing operation, the energy band of the gate region is raised when the gate exerts a negative bias. In addition, the LBT exerts a positive bias that can enhance hole injection to the channel from the lateral body site. Holes obtain kinetic energy by the electric field in the deep depletion of the channel region. Some holes gain sufficient energy to surmount the tunneling oxide barrier. Then, these holes are injected into the gate stack and are subsequently trapped in the charge-storage nitride layer to perform the erasing operation. However, traditional SONOS TFTs have poor erasing efficiency. Injecting holes to the nitride layer by FN tunneling becomes difficult because hole tunneling is forbidden due to the large hole barrier height ($>$ 4 eV) of the oxide [11]. Therefore, LBT SONOS TFTs have better erasing efficiency than conventional devices. Fig. 3(a) shows the endurance characteristics of LBT SONOS TFTs following various numbers of program/erase (P/E) cycles. A memory window of 2.5 V is sufficiently large to identify digital states (0 or 1) in a logic memory circuit. The LBT SONOS memory device maintains a wide threshold-voltage window even after 10^4 P/E cycles. In Fig. 3(b), the threshold-voltage shift of LBT SONOS TFTs was measured after various periods, as the devices were maintained at 85 °C. LBT SONOS TFTs exhibit good retention for 10^4 s, without a significant decline in the memory window.

Moreover, the subthreshold slope appears to change under erasing operation, as shown as in Fig. 1(b), because holes are not uniformly injected into the storage layer. Fig. 4(a) shows the schematic of LBT SONOS TFTs under erasing operation. Most of the holes are injected into the storage layer edge near the lateral body site because they come from the LBT. Thus, this region, called the edge transistor, has a lower threshold voltage. The other region, called the main transistor, has a higher threshold voltage due to the smaller amount of holes injected into the storage layer. The side that is farther away from the lateral body has less hole injection. Therefore, the transfer

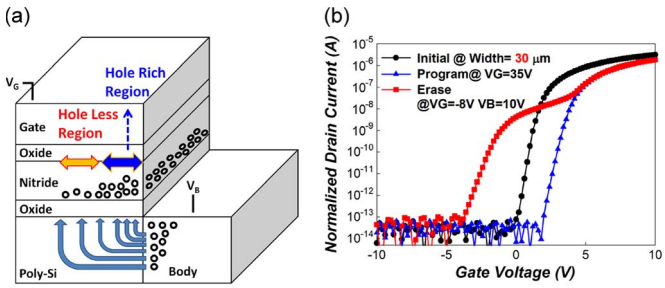

Fig. 4. (a) Regions corresponding to the hole-rich region (the main transistor) and the hole-less region (the edge transistor) are illustrated. (b) Electrical characteristics of the LBT SONOS memory device with width $= 30$ μm. The erase conditions was $V_G = -8$ V and $V_B = 10$ V.

characteristics are determined by the parallel main transistor and edge transistor.

To confirm the erasing hole current injecting from the lateral body site, the size effect of LBT SONOS TFTs under erasing operation was discussed. The electrical characteristics of LBT SONOS TFTs with width $= 30$ μm are shown in Fig. 4(b). It is found that a hump appears at a certain drain current level around 8×10^{-8} A. It suggested that the hump curve is determined by the main transistor and the edge transistor. The main transistor means the upper part of the transfer characteristic which does not shift under erasing operation. The lower part of the Id–Vg curve, determined by the edge transistor, shifts toward the negative direction significantly after erasing. It indicates that holes are not uniformly injected into the storage layer. Most of the holes are injected near the lateral body side. The side that is farther away from the lateral body has less hole injection. Therefore, in the process of erasing, the hump phenomenon appears at the large width of LBT SONOS TFTs.

IV. Conclusion

In this letter, we have investigated LBT SONOS TFTs under erasing operation. These devices have superior erasing efficiency, and the erasing mechanism has been illustrated by the energy band diagrams. The role of the LBT under erasing operation has been verified by different erasing conditions and structures. In addition, the hump phenomenon presenting at the large width of LBT SONOS TFTs after erasing operation has also been discussed and explained with the schematic diagram.

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