

# Characterization and Modeling of On-Chip Inductor Substrate Coupling Effect

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**Abstract** — The substrate coupling effects of two adjacent coplanar spiral inductors are characterized and modeled. The noise magnitude between two 45 $\mu\text{m}$ -away inductors can be reduced by 6.83 dB by using guard-ring surrounding each inductor, and improved by 10.28 dB further by adding patterned ground polysilicon shield beneath at 3 GHz. The inductor with patterned polysilicon shield beneath shows improved quality factor and noise isolation. Moreover, a macro model is presented for modeling quality factor and inductance of on-chip spiral inductor and associated neighboring inductor's coupling noise effect.

## I. INTRODUCTION

The inductor is one of the key elements in monolithic RFIC designs such as amplifiers, mixers, filters and oscillators [1][2]. For silicon technology, the significant coupling noise through lossy substrate is a big issue. The characterization and modeling [3][4][5] of s-parameters, inductance, quality factor, and coupling effect of coplanar spiral inductors are essential to optimize the RFIC performance and to minimize chip size and coupling noise by proper design and placement of components.

Reported here is the coupling effect of on-chip coplanar spiral inductors for various schemes, which has never been studied in previous works to the authors' knowledge. A correspondent model to characterize the coupling effect, integrated with single inductor's intrinsic high frequency characteristics, is presented. The inductor model can be used for the simulation and optimization of inductors' coupling noise, placement, and chip area.

## II. COUPLING EFFECT OF ON-CHIP COUPLED COPLANAR SPIRAL INDUCTORS

### A. Experimental Setup

A 0.25 $\mu\text{m}$  5-level metal CMOS technology is used to fabricate the on-chip spiral inductors. The P-type substrate resistivity is 10 $\Omega\text{-cm}$ , M4 and M5 thickness are 5700 $\text{\AA}$  and 10000 $\text{\AA}$ , respectively, and the oxide dielectric thickness between M4 and the substrate is about 56000 $\text{\AA}$ .

A 3.5-Turns octagonal spiral inductor is designed by using M4 and M5 stacked to form the coil and M3 to form the underpass. The layout representations of main configurations of coupled coplanar inductors are shown in Fig. 1. Fig. 1(a) shows the inductors without guard-ring within, and Fig. 1(b) shows the inductors with guard-rings within, and with or without patterned ground polysilicon shield beneath (PGS-inductor). A variety of inductor distances (D) are designed. M5 terminals are defined as port 1 and port 3; while, M3 terminals are defined as port 2 and port 4. The inductance (L) and quality factor (Q) in this paper are measured and extracted from the inductor between port 1 and port 2. For coupling noise measurement, a RF signal is forced to port 3 and the port 2 is sensed to measure the coupling noise ( $S_{23}$ ). All ground lines and guard-rings for coupled coplanar inductors are shorted together, and the spacing from guard-ring to coil is 20  $\mu\text{m}$ .

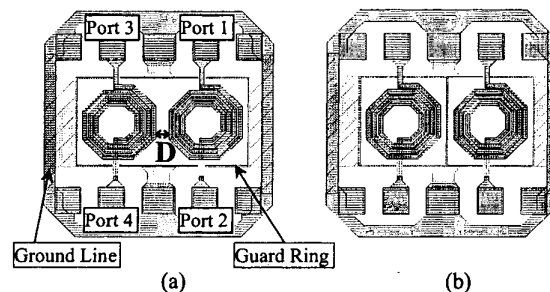


Fig. 1. Different configurations of on-chip coupled coplanar inductors with port numbering.

S-parameters are measured using Cascade Microtech G-S-G RF probes and an HP8510C Network Analyzer. Pad parasitic is de-embedded by subtracting out open-pattern's y-parameters. The two-port measurements are done as the other two remaining ports are floating. L and Q are extracted from the de-embedded Z-parameters using

$$L = \frac{\text{imag}(Z_{1\text{port}})}{2\pi f}; \quad Q = \frac{\text{imag}(Z_{1\text{port}})}{\text{real}(Z_{1\text{port}})}$$

And the coupling-noise is defined as the magnitude of de-embedded  $S_{23}$ .

## B. On-Chip Coupled Inductors

### B.1. Inductance, Quality Factor, and Self-Resonant Frequency of Single Inductors

First of all, for various single inductor configurations, the L and Q characteristics are investigated and shown in Fig. 2. At low frequency, all configurations show similar L and Q performance. There is no difference for L and Q of inductors with and without guard-ring. The previous work [6] indicated the Q of PGS-inductor could be improved 33% at 2GHz. In our experiment, the maximum Q is raised from 7.21 (at 2.7GHz for inductor without patterned ground polysilicon shield) to 8.39 (at 3.7GHz for PGS-inductor). And the maximum improvement of Q is 72% at 5.6GHz with the addition of patterned ground polysilicon shield. For PGS-inductor, the thinner dielectric thickness from coil to patterned polysilicon shield layer results in larger parasitic capacitance and lower self-resonant frequency ( $F_{SR}$ ). As the frequency is near  $F_{SR}$ , the inductance's drastic transition of PGS-inductor implies that the lower parasitic resistance, due to low resistance's patterned polysilicon, is in parallel with substrate parasitics. The lower parasitic resistance contributes to the observed Q's improvement of PGS-inductor.

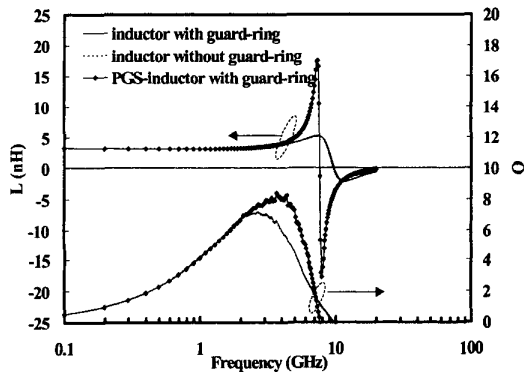


Fig. 2. Inductance (L) and quality factor (Q) versus frequency.

### B.2. Coupling Noise Effects of Coupled Inductors

Coupling noise through substrate is a critical issue for lossy substrate technology like silicon substrate. The realization and isolation techniques of coupling noise are crucial for the compact and confident RFIC layout and design. RF noise isolation can be improved by using grounded substrate guard ring surrounding the inductor [8] and/or patterned ground polysilicon shield beneath [6]. We investigate coupling noise effects of two closely placed coplanar spiral inductors for various configurations here.

The comparison of coupling noise on various distances (D) between two coupled inductors, with and without guard-ring within, is shown in Fig. 3. The equivalent

circuit of coupled inductors, between port 3 and port 2 in Fig. 1, at low frequency can be approximated to be the one as shown in Fig. 4 and its S-parameter  $S_{ba}$  is derived to be  $\frac{2(sC_{ox})^2 R_{sub}^2}{R_{subc}}$  (Eq. 1) under the conditions of low

frequency and  $R_{subc}$  being much larger than  $R_{sub}$ , where  $s = j\omega$ . At low frequency, Fig. 3 shows the initial slope of the  $S_{23}$  of 40 dB per decade, this is due to a couple of dc zeros [9]. The existence of two dc zeros implies that the  $S_{23}$  is proportional to  $s^2$  with substitution of  $s = j\omega$ . The measured coupling noise characteristic agrees well with the derived equation, Eq. 1. The two dc zeros are created by the  $C_{ox}$  of two coplanar inductors, in series. The larger coupling noise for higher frequency, owing to the two zeros, results in that the coupling noise needs to be considered more carefully for higher frequency application. At medium frequency, the magnitude of  $S_{23}$  turns down by  $-20$ dB per decade of frequency as frequency increases above 6GHz. The  $-20$ dB per decade indicates three poles occurring around this knee-point frequency. Two poles depend on the coil-to-substrate capacitors ( $C_{ox}$ ) and the two kinds of substrate resistances ( $R_{sub}$  and  $R_{subc}$ ); and the third pole depends on the core inductive characteristics of inductors. The frequency of knee-point can be derived by  $(2\pi R_{sub} C_{ox})^{-1}$ . At frequency above 15GHz, the substrate capacitance between two inductors will lead the increase of  $S_{23}$  again, as observed in Fig. 3.

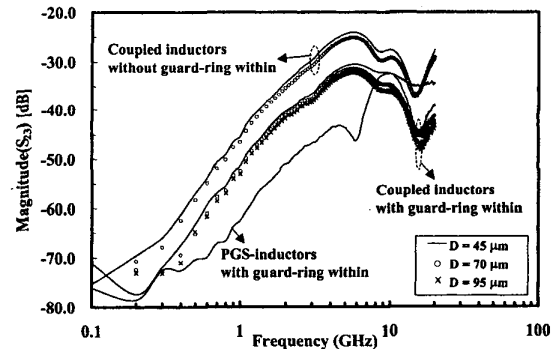


Fig. 3. Coupling noise versus frequency for various coupled coplanar inductor configurations and distances D.

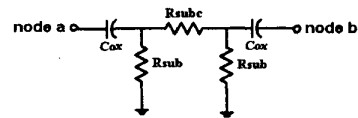


Fig. 4. A equivalent circuit of coupled inductors. The coil-to-substrate capacitors of two coupled inductors are modeled by  $C_{ox}$ . The resistance between the top substrate surface under inductor and the guard ring and the resistance between the two inductors are represented by  $R_{sub}$  and  $R_{subc}$ , respectively.

As shown in Fig. 3, the 6.83dB improvement of  $S_{23}$  at 3GHz is obtained for coupled inductors of  $D=45\mu\text{m}$  with guard-ring within than that without guard-ring within. The within guard-ring can improve the noise isolation well at low frequency, even at high frequency. The significant improvement is because that the fraction of substrate noise is shunted to ground effectively through the path of within guard-ring pick-up, not coupled to neighboring inductor. While PGS-inductor configuration with guard-ring (GR) within can give much better noise isolation characteristic for frequency below 9.6GHz than conventional inductor with GR within. It also has  $S_{23}$  at 3GHz 10.28dB lower than inductor without PGS but with GR within, and 17.11dB lower than that without either PGS or GR within. The coupling noise can be effectively reduced by using the within guard-ring, and further enhanced by using the beneath-inductor patterned ground polysilicon shield.

Because the typical silicon substrates are resistive up to several GHz [3], the  $S_{23}$  is inversely proportional to  $R_{\text{subc}}$  as shown in Eq. 1. Fig. 5 shows the coupling noise effects versus coupled inductors distances at 3GHz and the distance coefficient with guard-ring within is simplified to  $0.037\text{dB}/\mu\text{m}$  for a limited distance range. The linear-spacing-dependence is easy to use for the optimization of layout. The frequency limit of resistive substrate could be estimated from the relaxation time constant ( $\tau = \epsilon_{\text{si}} \cdot \rho = 1.05 \cdot 10^{-11}\text{sec}$ ) of typical substrates and the frequency at which the skin depth becomes comparable to the substrate dimensions (The characteristic frequency for skin-effect in Si-layer is  $\rho / \pi \mu_0 t_{\text{si}}$ , where  $t_{\text{si}}$  is the thickness of silicon layer [10]). Thus, based on this evidence and theory, we developed a lumped-circuit model by adding substrate resistors only between two inductors to emulate the substrate coupling effect in Section III.

The low distance coefficient in Fig. 5 implies that the significant coupling noise reduction will result in large chip area penalty. Thus, the effective substrate noise isolation techniques with maintaining compact chip size are important for RFIC design.

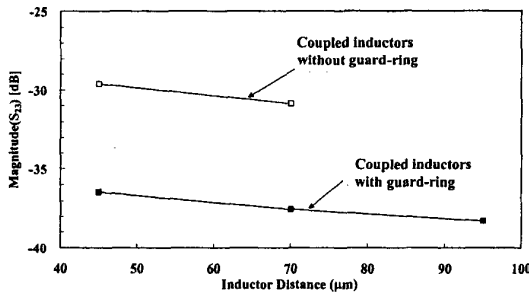


Fig. 5. Coupling noise at 3 GHz for different distances (D).

### III. MACRO MODEL OF COUPLED SPIRAL INDUCTORS FOR COUPLING EFFECT

Several equivalent-circuit models have been developed and successfully used to model most on-chip spiral inductors [11][12][13][7] for designing RF IC's. In order to accurately characterizing the eddy current effect and the skin effect, the model presented in [7] is adopted for modeling each single spiral inductor. In Fig. 6(a), the spiral coil structure is represented by an ideal inductance  $L_s$ , a series resistance  $R_s$ , a series composition of  $R_{\text{sk}}$  and  $L_{\text{sk}}$  in parallel, external connection wires inductance  $L_{x1}$  and  $L_{x2}$ , and an inter-wire capacitance  $C_x$ . The shunt parasitics result from a combination of oxide capacitance ( $C_{\text{ox}1}$ ,  $C_{\text{ox}2}$ ) between coil and substrate and substrate parasitics ( $R_{\text{sub}1}$ ,  $R_{\text{sub}2}$ ,  $C_{\text{sub}1}$ ,  $C_{\text{sub}2}$ ). As a result, the model for inductor with guard-ring shows good agreements with measured L and Q in Fig. 7. And the errors of both real and imaginary parts of S-parameters are below 10% for frequency lower than 5.7GHz. Similarly, the model of PGS-inductor also is implemented with same accuracy.

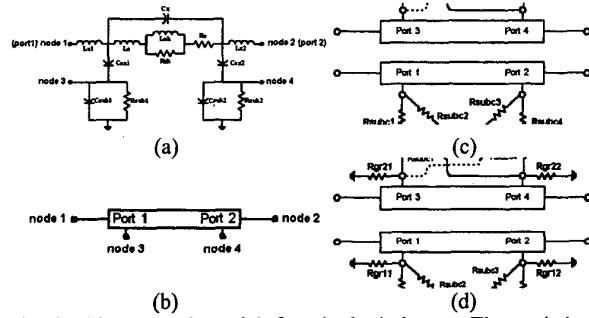


Fig. 6. (a) Lumped model for single inductor. The resistive networks for the coupled coplanar inductors configurations: without GR within (c) and with GR within (d).

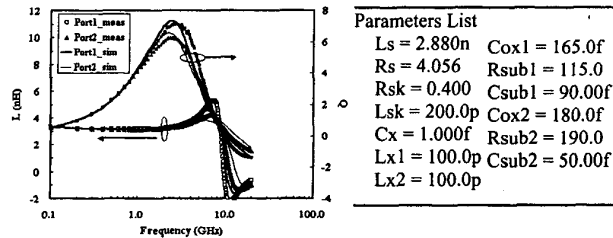


Fig. 7. L and Q for inductor with guard-ring. All parameters for the lumped models are shown in Parameter List Tables.

For modeling the substrate coupling effect of coupled inductors, two simple resistive networks are presented in Fig. 6 (c) and 6(d). This macro models are for the first order estimation of coupling noise and are easy to extract. The single inductor model in Fig. 6(a) is represented as a four-port sub-circuit in Fig. 6(b). For coupled inductor configuration without GR within, the resistive network for

coupling effect is composed by four  $R_{subc}$  as shown in Fig. 6(c). The parasitic substrate resistance between two coupled inductors is characterized by  $\pi$  model. Four  $R_{gr}$  are added as Fig. 6(d) for modeling the effect of guard-ring addition for coupled inductors with GR within. The four  $R_{subc}$  and  $R_{gr}$  values can be assumed to be same, respectively, for the symmetry layout. Then,  $R_{subc}$  and  $R_{gr}$  can be extracted out individually by modeling  $S_{23}$  characteristics of coupled inductors without and with GR within in sequence. Fig. 8 shows, at frequency below several GHz, the good agreements of simulated and measured  $S_{23}$  for various coupled inductor configurations with  $D=45\mu\text{m}$ . However, as frequency up to 0.6GHz, the phases of the  $S_{23}$  start to drop from  $180^\circ$ , that is  $\pi$  (radian). The descending slopes also indicate the poles exist as explained previously in Section II. The frequency of knee-point of  $\text{Mag}(S_{23})$  can be estimated by  $(2\pi R_{sub} C_{ox})^{-1} \sim 6\text{GHz}$ , where  $R_{sub}$  and  $C_{sub}$  are from the inserted table in Fig. 7, which shows good agreement with measurement results. In this macro model, the parasitic effect for coupling noise simulation at frequency near or above self-resonant frequency is not considered in order to simplify the model but to preserve the accuracy within the application frequency range. The  $R_{subc}$  should be distance-dependent resistance and extracted from coupling noise characteristics of coupled inductors with various distances  $D$ . The distance coefficient is  $6 \Omega/\mu\text{m}$ ; that means, the  $R_{subc}$  is  $1350\Omega$  for  $D=70\mu\text{m}$  and  $1500\Omega$  for  $D=95\mu\text{m}$ . The simulation results with the distance coefficient are shown in Fig. 9, as compared with measurement data. Thus, enough accuracy can be obtained by simple resistive network we present and the macro model is helpful to optimize the coupling effect and simulate whole chip's complete characteristics.

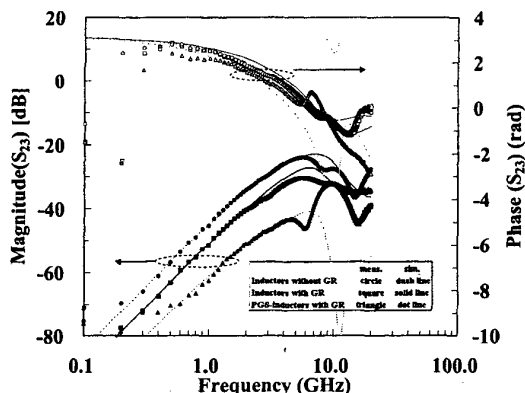


Fig. 8. Comparison of macro models for  $S_{23}$ , where  $R_{subc}$  are  $1.2 \text{ K}\Omega$  and  $R_{gr}$  are  $190 \Omega$ .

#### IV. CONCLUSION

The characterization on coupling effect of on-chip coplanar inductors has been presented. The inductors with guard-ring within have significant noise isolation improvement, even for high frequency above 10 GHz. The PGS-inductor can enhance quality factor and noise isolation performance simultaneously. We develop the circuit simulation macro models with simple resistive networks to consider the coupling noise effect for coupled inductors as well as the inductor's intrinsic characteristics.

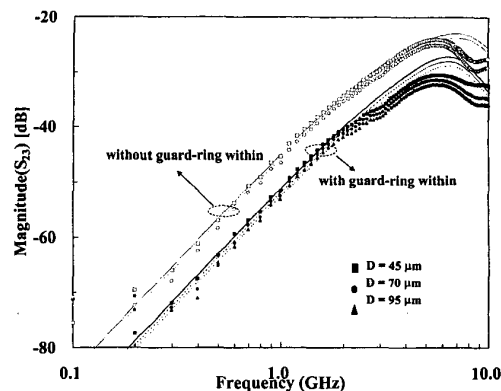


Fig. 9. Coupling noise of macro models vs. distance dependence.

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