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An Electrical Method to Characterize Thermal Reactions of Pd/GaAs and Ni/GaAs Contacts

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Capacitance-voltage (C-V) and current-voltage (I-V) measurements were used to study the thermal reaction of Pd/GaAs contacts and Ni/GaAs contacts. The thickness of GaAs consumed by the metal/GaAs reaction during annealing was calculated from C-V analyses and I-V analyses. For annealing temperatures below 350°C, the Schottky characteristics of the diodes were good but the electrical junction moves into the GaAs after annealing. The amount of junction movement was calculated directly from our measurements. The diffusion coefficients of Pd and Ni in GaAs at 300°C were estimated both to be around 1.2×10^{-14} cm^2/s.

Key words: Activation energy, diffusion coefficients, Schottky contacts

INTRODUCTION

The threshold voltage of a GaAs metal-semiconductor field effect transistor (MESFET) can be controlled by adjusting the thickness of the epitaxial or the conducting layer under the gate. In MESFETs with a buried gate,[1] this is achieved by reacting the gate metal with the epitaxial layer underneath.[2] As the reaction proceeds, the thickness of the epitaxial layer is reduced and the threshold is thus adjusted. Neither wet etching nor dry etching is needed to adjust thickness of the epitaxial layer.

The near-noble metals, Ni, Pd, or Pt are suitable for the application as a gate metal in the buried gate FETs because of ease of deposition, low reaction temperature with GaAs, and resistance to oxidation. Many studies of these metals' contacts to GaAs have been reported[3–19] with most focused on the characterization and understanding of the material properties of these metal-semiconductor systems[6–8,15] or on the relationship between the material properties and the Schottky characteristics.[11,17,19] In the application for buried gate FETs, the Schottky characteristics of gate contacts and the amount of shift in depletion width due to metal/semiconductor interaction is critical information. However, the previous studies did not investigate the thickness of the epitaxial layer reduced during annealing or the Schottky characteristics after metal/semiconductor interaction simultaneously.

In this paper, we discuss the thermal reactions of Pd/GaAs contacts and Ni/GaAs contacts by current-voltage (I-V) measurements and capacitance-voltage (C-V) measurements. The reacted thickness of GaAs and the amount of change in depletion layer width are directly obtained by calculating the carrier concentration profiles of these samples from C-V measurements while the Schottky characteristics of these diodes are clarified by I-V measurements. The dependence of depletion layer width on Schottky barrier height is also considered in calculating the thickness of GaAs reacted with metal to ensure a better accu-

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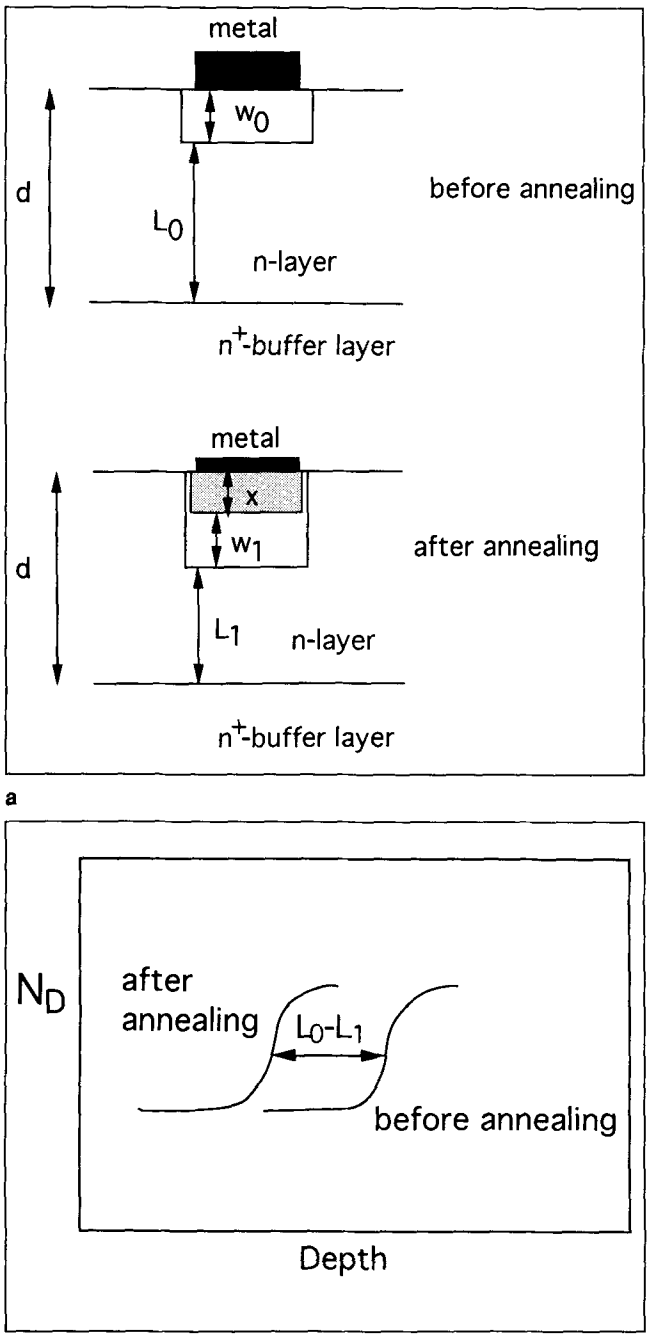


Fig. 1. (a) The layer structures used to interpret the difference between the samples before and after thermal treatment in this study, and (b) the carrier concentration profiles of the samples before and after heat treatment used to interpret the shift in the n-GaAs/n⁺-GaAs interface during annealing.

racy. The diffusion coefficients of Pd and Ni in GaAs and the activation energy are also estimated.

EXPERIMENTS AND ANALYSES

Polished n-type (100) GaAs wafers with a dopant concentration of about $5 \times 10^{16}/cm^3$ were used in these studies. Two epitaxial layers were grown upon the substrates by molecular beam epitaxy (MBE) before the fabrication of Schottky contacts. The first layer was a 0.3 μm n^+-buffer layer with a carrier concentration of $5 \times 10^{17}/cm^3$. The second layer was a 0.3 μm n-layer with a carrier concentration of $8 \times 10^{16}/cm^3$.

Circular Schottky diodes with a diameter of 500 μm were defined on the epitaxial layers. The metal film was deposited by electron gun evaporation. The samples were first subjected to a wet chemical cleaning treatment that included the following: 5 s dip in $1H_2SO_4:1H_2O_2:500H_2O$ at room temperature, 1 min. rinse in deionized (DI) water, 1 min dip in $1HCl:1H_2O$, and a final rinse in DI water for 30 s. The substrates were blow dried with filtered dry nitrogen prior to evaporation. The metal film thickness deposited was 0.2 μm. The backside of these samples were then coated with Au by a radio frequency (RF) sputtering system for ohmic contact. Heat treatments were performed in a N_2 ambient with annealing temperatures ranged from 200 to 400°C. The diodes were then characterized by I-V and C-V measurements. An HP-4145 semiconductor parameter analyzer was used to measure the I-V characteristics of the Schottky diodes. The C-V characteristics were measured by an HP-4275 multi-frequency LCR meter.

It is assumed that there is no redistribution of Si dopants in the sample after 300°C annealing. As shown in Fig. 1a, if d denotes the distance between the metal/semiconductor interface and the n-GaAs/n⁺-GaAs interface, w denotes the distance between the metal/semiconductor interface and the depletion region edge of Schottky contacts at zero bias, and L denotes the distance from the depletion region edge to the n-GaAs/n⁺-GaAs interface, then the relationship between d, w, and L can be expressed as:

$$d = w_0 + L_0 = x + w_1 + L_1 \quad (1)$$

$$\text{or } x = (w_0 - w_1) + (L_0 - L_1) \quad (2)$$

where x denotes the amount of GaAs consumed by metal/GaAs reactions during annealing. The letters with subscript "0" indicate the parameters of the sample before thermal treatments, whereas those with subscript "1" indicate the parameters of the sample after annealing. The term $(w_0 - w_1)$ in the right hand side of Eq. (2) is the change in depletion region depth due to the Schottky barrrier height variation after annealing. The second term $(L_0 - L_1)$ denotes the amount of the horizontal shift of the carrier concentration profiles of the thermal annealed sample from that of the as-deposited one as shown in Fig. 1b. From the values of Schottky barrier height of the samples before and after thermal treatments obtained from I-V analyses, we can calculate $(w_0 - w_1)$ by using the equation

$$w_0 - w_1 = [2\varepsilon_s(\phi_{B0} - V_n)/(qN_D)]^{1/2} - [2\varepsilon_s(\phi_{B1} - V_n)/(qN_D)]^{1/2} \quad (3)$$

where ϕ_{B0} and ϕ_{B1} are the Schottky barrier heights of the diodes before and after thermal treatments, V_n is the energy difference between the Fermi level and the bottom of condution band in semiconductor, ε_s is the

dielectric constant of the semiconductor, and N_D is the doping concentration in the epitaxial layer.[20] From C-V measurements and by using the equations:

$$C = \varepsilon_s/w \quad (4)$$

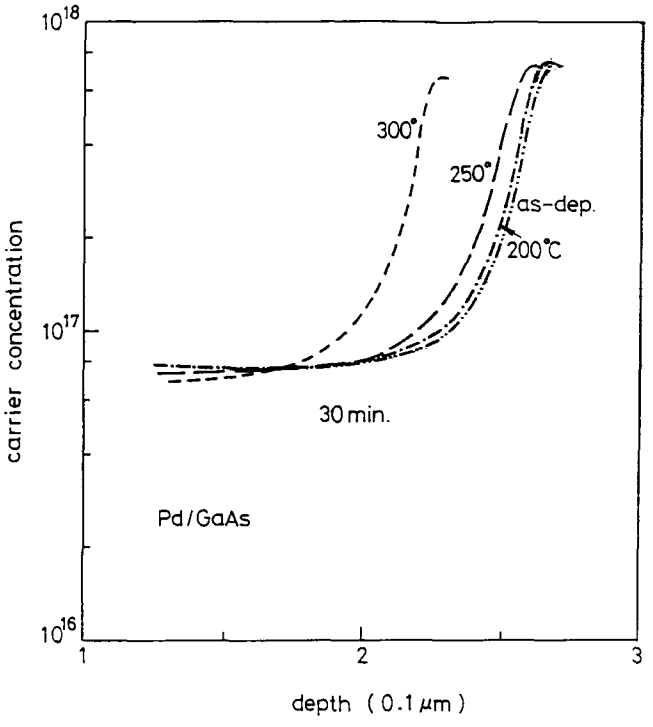
$$N_D = [2/(q\varepsilon_s)][-1/(\partial(1/C^2)/\partial V)] \quad (5)$$

we can estimate the amount of the horizontal shift of the carrier concentration profiles of the samples annealed. As a result, the thickness of GaAs reacted with metal x can be calculated.

RESULTS

Pd/GaAs Contacts

The carrier concentration profiles of Pd/GaAs Schottky diodes with various annealing temperatures obtained from C-V analyses are shown in Fig. 2a. The corresponding Schottky barrier heights and ideality factors (defined as $n = (q/kT)/[\partial(\ln I)/\partial V]$) of these diodes obtained from I-V analyses are shown in Fig. 2b. There are four curves in Fig. 2a, representing



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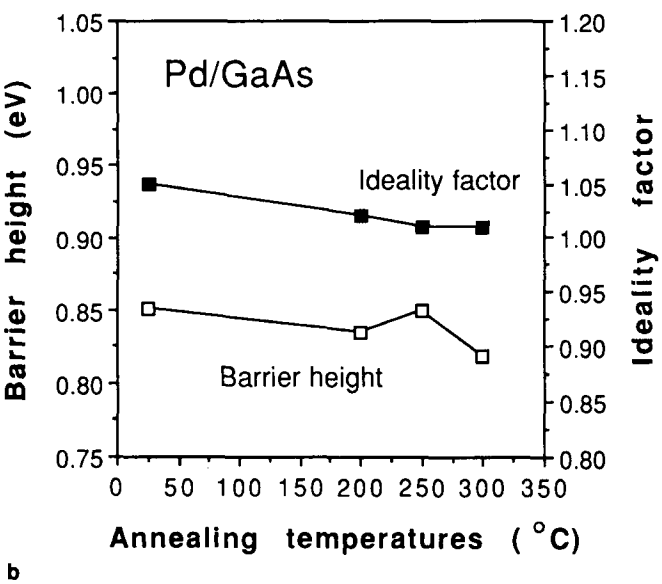

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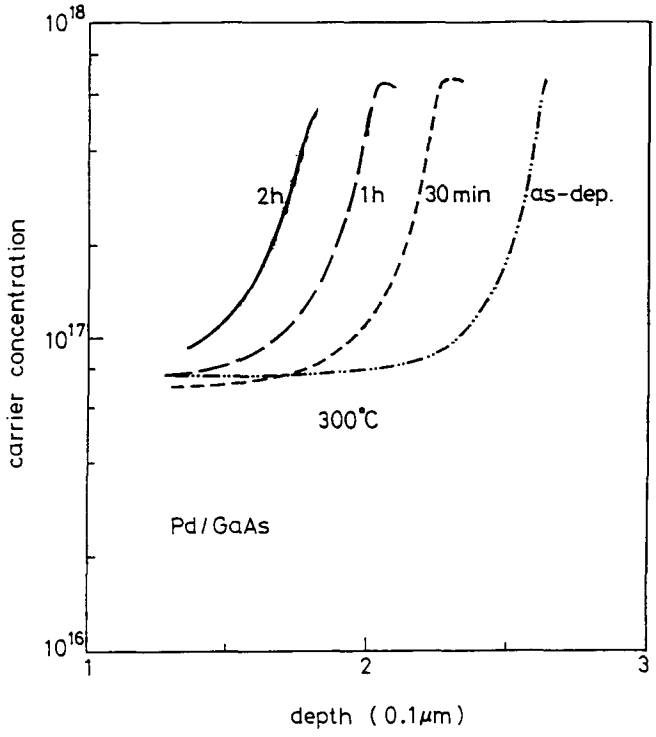
Fig. 2. (a) The carrier concentration profiles of Pd/GaAs Schottky diodes after 30 min annealing at various annealing temperatures; and (b) the ideality factor and Schottky barrier height of Pd/GaAs diodes vs annealing temperature for 30 min isochronal annealing.



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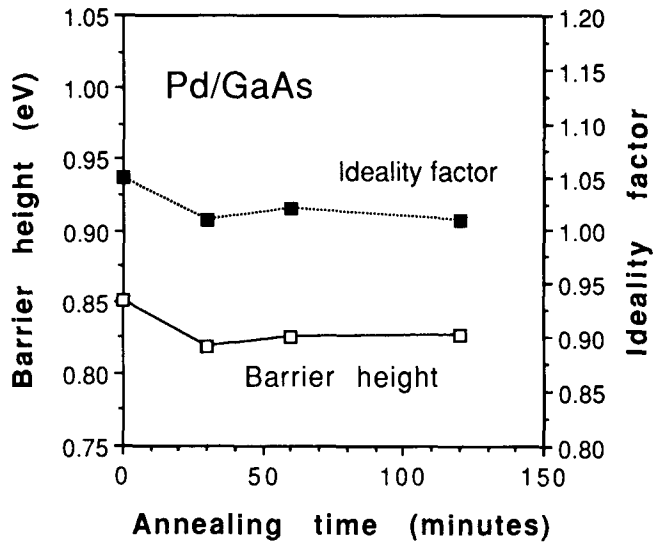

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Fig. 3. (a) The carrier concentration profiles of Pd/GaAs Schottky diodes with various annealing time as a parameter obtained from C-V analyses; and (b) the ideality factor and and Schottky barrier height of the diodes in part (a) vs annealing time for 300°C isothermal annealing.

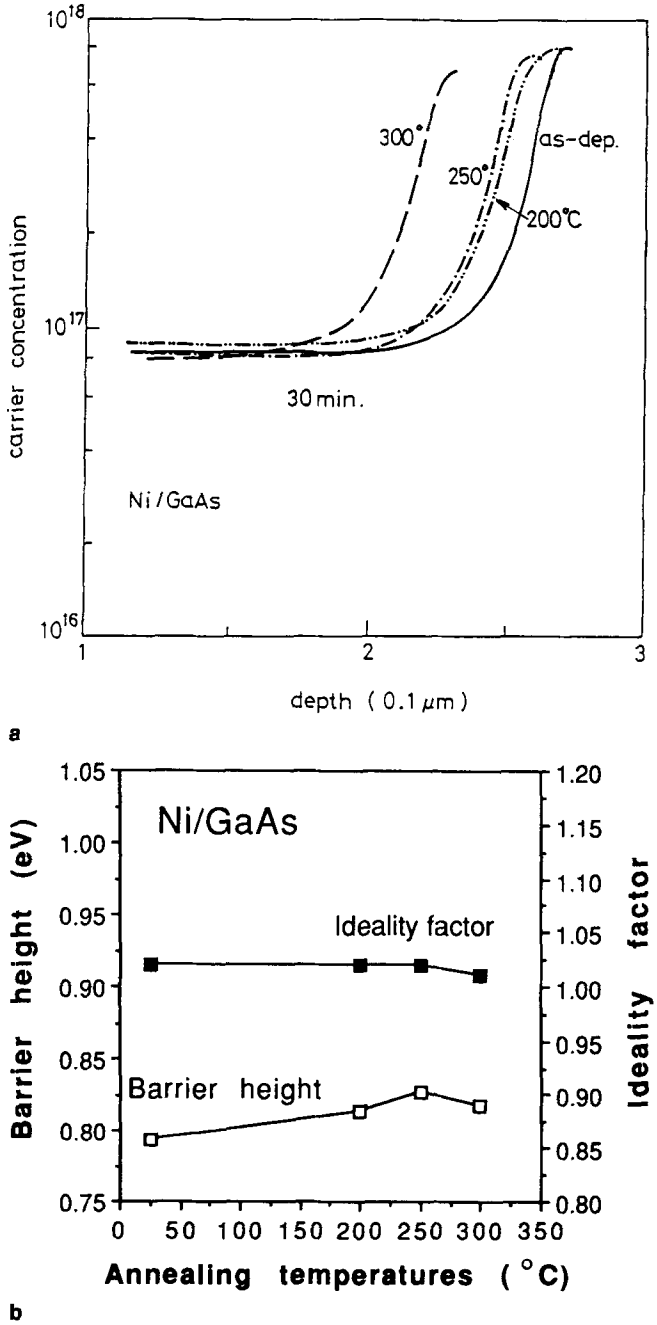


Fig.4. (a) The carrier concentration profiles of Ni/GaAs Schottky diodes with various annealing temperatures as a parameter obtained from C-V analyses; and (b) the ideality factor and Schottky barrier height of Ni/GaAs diodes obtained from I-V analyses vs annealing temperatures for 30 min isochronal annealing.

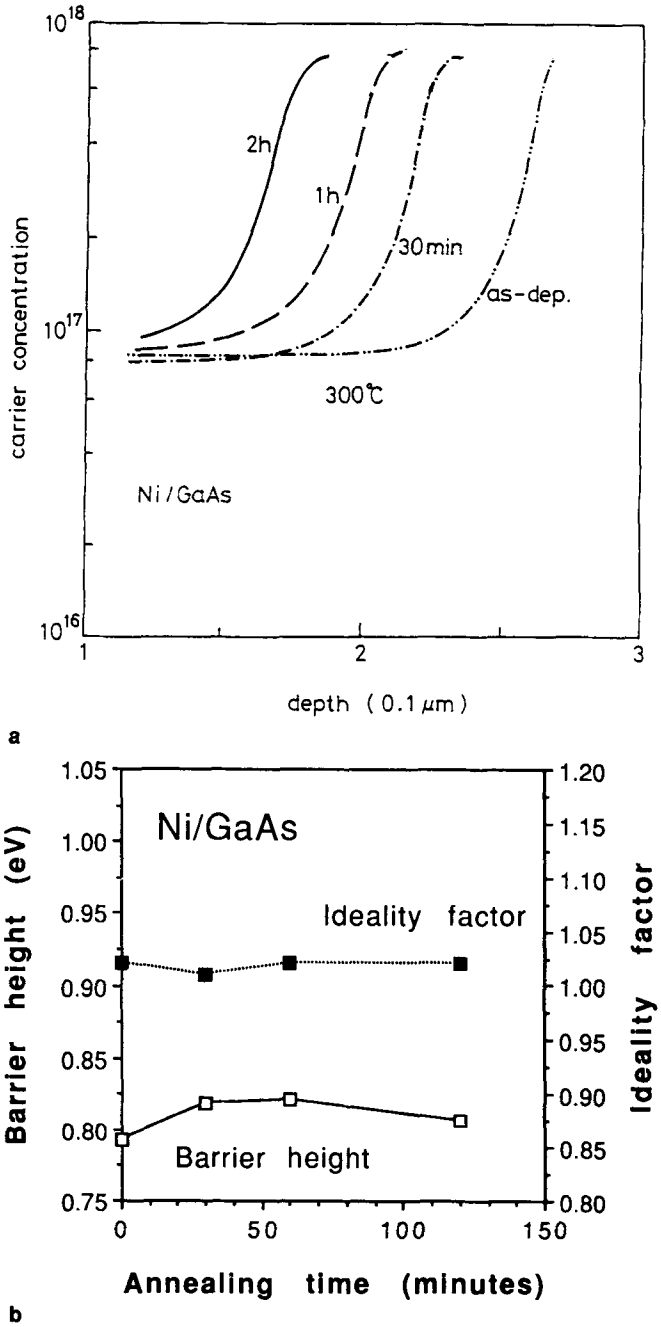


Fig. 5. (a) The carrier concentration profiles of Ni/GaAs Schottky diodes with various annealing time as a parameter obtained from capacitance-voltage analyses; and (b) the ideality factor and Schottky barrier height of the diodes in part (a) vs annealing time for 300°C isothermal annealing.

the carrier concentration profiles of the diodes before and after annealing at 200, 250, and 300°C for 30 min. The right most curve in the figure is the profile obtained from a diode before any thermal treatment. The doping concentration change at the interface between the n- GaAs layer and the n^+- GaAs layer is clearly seen in the figure. As the annealing temperature increases, the curve gradually shifts to the left. The n-GaAs/n^+-GaAs interface appears to be closer to the surface. This is a clear indication that part of the GaAs layer has reacted with Pd after annealing, and the Schottky junction has moved inside the GaAs layer. The Schottky characteristics of these diodes remain good after annealing. The carrier concentration profiles of Pd/GaAs Schottky diodes annealed at 300°C with various annealing times are also calculated and are shown in Fig. 3a. The annealing times were 30, 60, and 120 min. The corresponding Schottky barrier heights and ideality factors of these samples are shown in Fig. 3b. All these diodes have good Schottky characteristics as indicated in the figure.

Ni/GaAs Contacts

The carrier concentration profiles of Ni/GaAs Schottky diodes for various annealing temperatures are shown in Fig. 4a and the corresponding Schottky barrier heights and ideality factors of these samples are shown in Fig. 4b. As in the case of Pd/GaAs contacts, as the annealing temperature increases, the curve gradually shifts to the left and the n-layer/n^+-layer interfacial depth, W, decreases, indicating part of GaAs has been reacted with Ni. The carrier concentration profiles of Ni/GaAs Schottky diodes annealed at 300°C for 30, 60, and 120 min are shown in Fig. 5a.The corresponding Schottky barrier heights and ideality factors of these samples are shown in Fig. 5b. For longer annealing times, more GaAs reacts with the Ni. All the diodes have good Schottky characteristics with ideality factors close to unity as indicated in Fig. 4b and Fig. 5b.

DISCUSSION

Substituting the values of Schottky barrier heights of these samples obtained from I-V analyses into Eq. 3 and using Eq. 2, we can calculate the thickness of GaAs reacted with metal during thermal treatments.

The thicknesses of reacted GaAs for Pd/GaAs and Ni/GAAs samples as functions of annealing temperature for 30 min isochronal annealing are shown in Fig. 6. With the annealing temperature fixed at 300°C, the thicknesses of GaAs reacted with Pd and Ni are found to be proportional to the square root of annealing time. The relationships are plotted in Fig. 7a and 7b. This type of time dependence indicates that the reaction between the metal and GaAs is a diffusion controlled process. Comparing Fig. 7a and 7b, there is no significant difference between the metal systems, although Ni seems to diffuse faster at lower temperatures as indicated in Fig. 6. From the relationship between the amount of GaAs consumed by reaction and the annealing time in our results and by the aid of the nomograph for extracting diffusion coefficients proposed by Hall and Morabito,[21] we can estimate the diffusion coefficients of Pd and Ni in GaAs at 300°C. Both the diffusion coefficients of Pd in GaAs at 300°C and that of Ni in GaAs at the same temperature were estimated to be around 1.2×10^{-14} cm^2/s.

From the results of isochronal annealing, the rela-

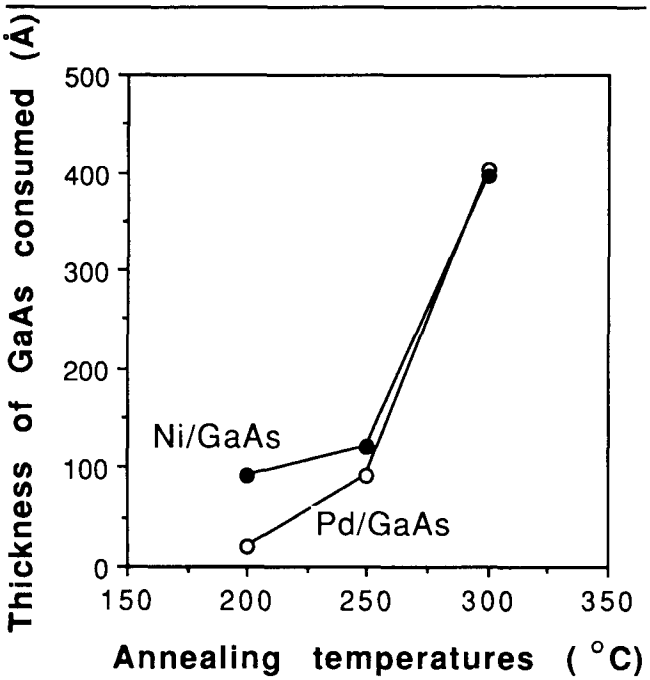
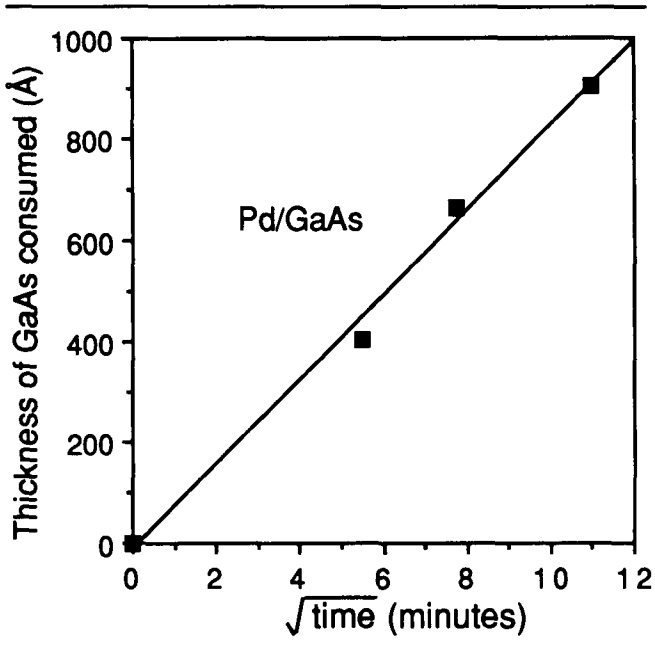


Fig. 6. The thickness of GaAs consumed by Pd/GaAs reaction and that consumed by Ni/GaAs reaction during annealing vs annealing temperatures for 30 min isochronal annealing.



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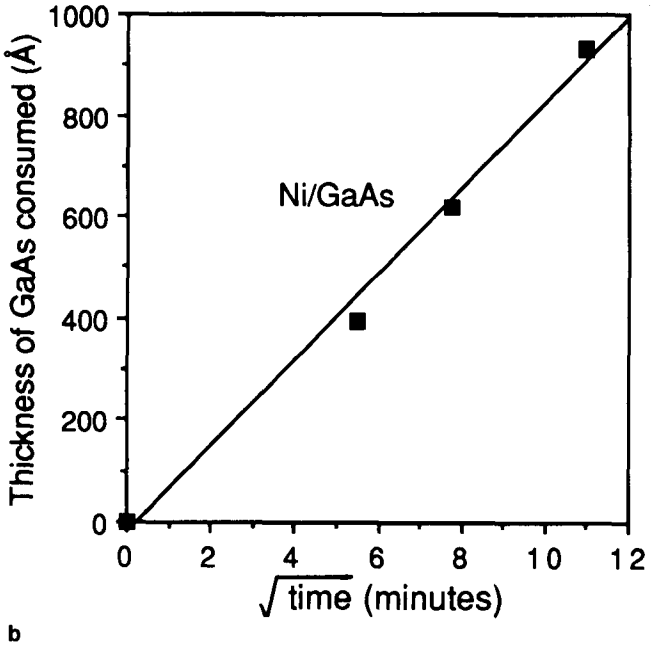

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Fig. 7. (a) The thickness of GaAs consumed by Pd/GaAs reaction during annealing vs square root of annealing time for 300°C isothermal annealing; and (b) the thickness of GaAs consumed by Ni/GaAs reaction during annealing vs square root of annealing time for 300°C isothermal annealing.

tionship between the thickness of GaAs reacted with metal and the annealing temperatures was used to calculate the activation energy for metal diffusion in GaAs. The activation energy was found to be about 1.4 and 0.67 eV for Pd diffusion and Ni diffusion in GaAs, respectively. Pd, which diffuses with an obviously larger activation energy than that for Ni, is more suitable to be used as the gate metal for the buried gate MESFETs from the viewpoint of activation energy because it reacted with GaAs slower than Ni did for temperature lower than 250°C, the possible temperature range for device operation. However, in the papers of Sands et al.,[3,4] they mentioned that during annealing between 250 and 275°C, the Pd/GaAs reaction involved the nucleation and growth of a second Pd_xGaAs phase and the reacted layer was found to be laterally nonuniform. This might limit the feasibility of Pd to be a suitable reactant for a buried gate from the perspective of device yield.

An obvious difference in the annealing behavior of the Schottky barrier height (SBH) can be observed from the I-V analyses of the two contacts. The SBH of Pd/GaAs contacts decreases after low temperature annealing as shown in Fig. 2b and Fig. 3b, while that of Ni/GaAs contacts increases under similar annealing conditions (see Fig. 4b and Fig. 5b). The increase in SBH of Ni/GaAs contacts after low temperature annealing was also reported by Yu et al.[17] and Lahav et al.[11] Yu et al. attributed the increase in SBH to the removal of native oxides typical to the as-deposited sample. The decrease in SBH of Pd/GaAs contacts after low temperature annealing was also observed in the experiments of Liew et al.,[18] Nee et al.,[19] and Sharda et al.[10] The SBH decrease of Pd/GaAs contacts was attributed by Liew et al. to the onset of a solid-phase reaction that changes the interface chemistry.

Solomon et al. previously studied the diffusion of Ni in GaAs and obtained diffusion coefficients for Ni at different temperatures using Auger sputter analysis for Ni on both clean and oxide covered GaAs.[16] The diffusion coefficient obtained was around 2.4×10^{-14} cm^2/s for oxygen-free Ni/GaAs interfaces and around 6×10^{-16} cm^2/s for those with oxygen-contaminated interfaces at 300°C. Our results obtained from electrical analyses are slightly less than the diffusion coefficient of their oxygen-free samples. This may be due to the fact that a small amount of oxides exist at the Ni/GaAs interface in our samples, slightly impeding the diffusion of Ni into GaAs. Both our electrical method and the Auger sputter profile analysis can be used to calculate the diffusion coefficients of Ni in GaAs, however, the former can give the information of the Schottky characteristics of the contacts simultaneously, while the latter not. In the Auger sputter profile analysis method, an additional process is necessary to characterize the electrical properties of the structure. The Auger analysis usually provides a physical confirmation of the electrical measurements.

CONCLUSIONS

We have studied the thermal reaction of Pd/GaAs contacts and Ni/GaAs, contacts by C-V and I-V analyses. The thickness of GaAs consumed by the metal/GaAs reaction during annealing was calculated directly from C-V analyses and I-V analyses. The Schottky characteristics were good but the electrial junction moves inside GaAs after annealing. The amount of junction movement was calculated directly from our measurements. The diffusion coefficient of Pd and Ni in GaAs and the activation energy were estimated.

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