Inspection of the Current-Mirror Mismatch by Secondary Electron Potential Contrast With *In Situ* Nanoprobe Biasing

Po-Tsun Liu, *Senior Member, IEEE*, and Jeng-Han Lee

***Abstract*—The mismatch mechanism in a current mirror consisting of laterally diffused p-channel MOS (LDPMOS) technology was investigated using a scanning electron microscope (SEM) with *in situ* nanoprobing. The electrical measurement found a saturation current mismatch of 52 μA between the LDPMOS transistors. Furthermore, the proposed inspection identified successfully 0.4-μm p-well layer misalignment, which was the root cause of the mismatch. This letter demonstrates that an *in situ* nanoprobing system is a powerful tool for enhancing p-well dopant contrast in a SEM, analyzing site-specific failures, and studying device physics under a dynamic scope.**

***Index Terms*—Current mirror, laterally diffused p-channel metal–oxide–semiconductor (LDPMOS), nanoprobing, secondary electron potential contrast (SEPC).**

I. Introduction

Laterally diffused MOS (LDMOS) devices are widely used to reduce costs and increase flexibility in high-voltage and high-current applications, e.g., power-management integrated circuits, motor drivers, and class-D amplifiers [1]–[3]. The channel length plays an important role in determining device performance. The channel length of an LDMOS device is controlled by the physical location of the active area, the poly-silicon gate, the n-well, and the p-well. Poor control of the photomask alignment and the dimensions of these four layers will result in a channel length deviation and thus interfere with device performance. At worst, device performance variation will result in failure, and failure analysis should be conducted for yield enhancement. The physical location of the active area and the poly-silicon gate can be inspected easily by a scanning electron microscope (SEM). However, the p-well and n-well implantation areas need additional delineation procedures for SEM inspection. Recently, secondary electron potential contrast (SEPC) in SEMs has emerged as a quantitative tool for dopant profile inspection, with sensitivity ranging from 10^{16} to 10^{20} cm^{-3} and a spatial resolution of 10 nm [4]–[6]. The SEPC signals arise from differences in the built-in potential between different doping areas. Researchers have conducted studies on materials with wide energy band gaps, such as SiC [7], [8]. However, the SEPC signal inspection using silicon is more difficult, i.e., given a silicon's small (1.1 eV) band gap. In addition, an amorphous layer generated in the sample preparation process will also reduce the SEPC in SEMs [9]. All these effects will hinder the SEPC application in the dopant area inspection. In this letter, we use *in situ* nanoprobing to apply a direct-current bias to the p-well/n-well nodes to intensify the SEPC signal. The proposed method identifies successfully p-well misalignment as the root cause of channel length variation.

Manuscript received April 10, 2011; revised June 18, 2011; accepted June 29, 2011. Date of publication July 31, 2011; date of current version September 28, 2011. The review of this letter was arranged by Editor M. Passlack.

P.-T. Liu is with the Department of Photonics and Display Institute, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: ptliu@mail.nctu.edu.tw).

J.-H. Lee is with the Department of Photonics and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: jameslee395@gmail.com).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2011.2161567

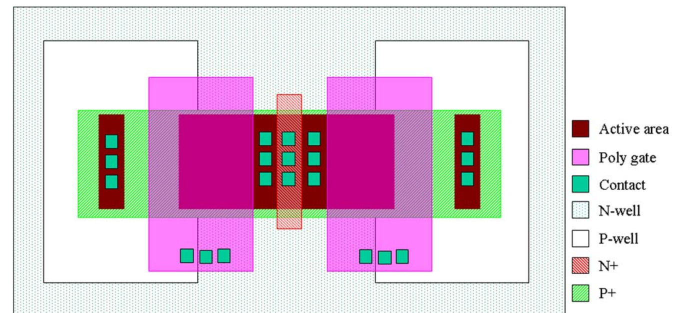

Fig. 1. Pattern layout of the current mirror.

II. Experiment

The sample used in this letter is a power-management chip fabricated using 0.6-μm LDMOS technology, which suffers an abnormally high shutdown current in wafer-level testing [1]–[3]. The designer suspected that this abnormality was initiated by a mismatch of the current mirror. Two laterally diffused p-channel MOS (LDPMOS) transistors were designed with the same physical dimensions for the current-mirror application in the chip. Fig. 1 shows a schematic that illustrates the pattern layout of the current mirror with two LDPMOS transistors built in a back-to-back MOS layout. The left LDPMOS is the master transistor, and the right LDPMOS is the slave transistor. The channel length L_{channel} is the overlap area of the n-well and the poly gate, which is controlled by the physical location of the active area, the poly gate, the n-well, and the p-well. To verify the mismatch, two samples, i.e., one bad die and one good die, were polished manually to the contact layer for electrical performance characterization. A Zyvex nanoprobing

0741-3106/$26.00 © 2011 IEEE

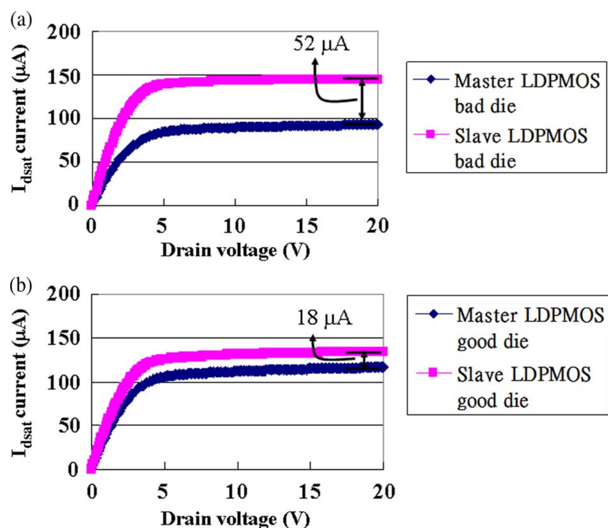

Fig. 2. (a) Electrical characteristics I_d–V_d of the master and slave LDPMOS transistors from the bad die at $V_g = -5$ V. (b) Electrical characteristics I_d–V_d of the master and slave LDPMOS transistors from the good die at $V_g = -5$ V. The LDPMOS pair from the bad die shows an obvious I_{dsat} mismatch of 52 μA in comparison with a I_{dsat} mismatch of 18 μA from the good die.

system with four micromanipulators was used to measure the transistors, which were mounted on the stage of an SEM Leo 1530. Following the electrical measurement, the sample was immersed in an HF solution to remove the dielectric oxide exposing the active area of the sample. The sample was then put into the SEM chamber to inspect the plane-view dopant area. The nanoprobing tips probed the n-well and p-well regions with electrical biases in of 5 and 0 V in the n-well and the p-well, respectively. Optimum SEM operating conditions were set to view the SEPC image.

III. Results and Discussion

Fig. 2(a) depicts the drain current I_d as a function of the drain voltage V_d at the gate voltage $V_g = -5$ V with the master and slave LDPMOS transistors from the bad die. The saturation currents I_{dsat} of the master LDPMOS and the slave LDPMOS are 93 and 145 μA, respectively. Fig. 2(b) depicts the drain current I_d as a function of V_d at $V_g = -5$ V with the master and slave LDPMOS transistors from the good die. The I_{dsat} current of the master LDPMOS and slave LDPMOS are 116 and 134 μA, respectively. The LDPMOS pair from the bad die shows an obvious I_{dsat} mismatch of 52 μA in comparison with a I_{dsat} mismatch of 18 μA from the good die. The obvious I_{dsat} mismatch from the bad die was most likely caused by misalignment during the processing of the p-well region and could be the original cause of the failure.

Fig. 3(a) is a plane-view SEM image with three nanoprobing tips probing the n-well and p-well regions without electricity bias. The image shows no dopant area information. Fig. 3(b) is a SEM image in which nanoprobing tips are electrically biased with 5 V on the n-well region and 0 V on the p-well region. Dopant area is visible in the image, with the p-well region providing the brightness contrast and the n-well providing the darkness contrast. The proposed *in situ* nanoprobing method exhibited a very good dopant contrast enhancement effect and

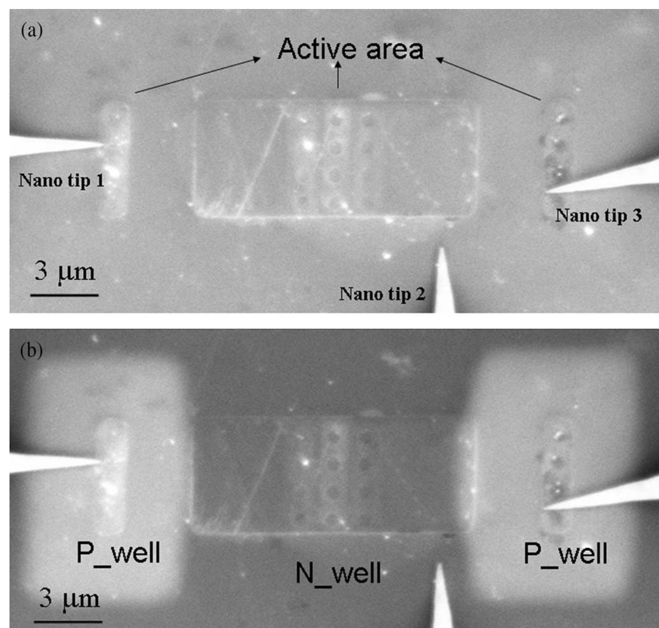

Fig. 3. (a) Plane-view SEM image with three nanoprobing tips probing the n-well and p-well regions without electricity bias. The image shows no dopant area information. (b) SEM image in which nanoprobing tips were biased electrically with 5 V on the n-well region and 0 V on the p-well region. Dopant area is visible in the image, with the p-well region providing the brightness contrast and the n-well providing the darkness contrast.

has great practical applications in a real circuit. Fig. 3(b) also indicates that the p-well is misaligned with the active area layer.

Since 1960, researchers have been investigating the mechanism of dopant contrast in SEMs. Several studies reported that the 1-D SEPC profile of boron-doped p^+/n-well shows a linear relationship with the logarithm of the Secondary Ion Mass Spectrometry depth profile [4], [5]. The study of Venables and Maher on a biased junction found that the SEPC intensity is proportional to the built-in voltage of the silicon surface [4]. Venables and Maher reported the same intensity contour level corresponding to the same doping concentration [4]. For a biased junction in this letter, the points in the same intensity contour level, e.g., an intensity contour of 50%, should correspond to the same doping concentration and surface voltage. Therefore, this 50% intensity contour line indicates a line with same doping concentration and could be used for misalignment measurement. To measure quantitatively the misalignment, the intensity contours resulting from the image of Fig. 3(b) are shown in Fig. 4. Point A highlighted in Fig. 4 represents the center point of the active area layer. Points B and C in Fig. 4 represent the 50% intensity level of the left p-well and the right p-well, respectively. The distances between points B and A and between points C and A are 6.2 and 5.4 μm, respectively. The misalignment value between the active layer and the p-well layer can be expressed as the following:

$$\text{Misalignment Value} = \frac{\overline{AB} - \overline{AC}}{2} \tag{1}$$

The calculation shows that the misalignment of the active area layer and the p-well layer is 0.4 μm. A designed p-well-layer misalignment experiment split also confirmed that

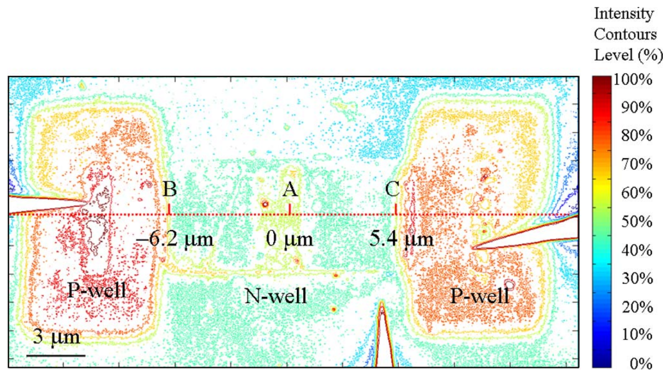

Fig. 4. Intensity contours result from the image in Fig. 3. The misalignment between the active area and the p-well layer is 0.4 μm.

misalignment greater than 0.4 μm will induce a high shutdown current in the chip.

IV. Conclusion

In summary, this letter has used a SEM and nanoprobing to investigate the mismatch mechanism of a current mirror. A 52-μA mismatch of the saturation current between the master LDPMOS and the slave LDPMOS was characterized by a nanoprobing system. Furthermore, a novel combination of SEM and nanoprobing was proposed to inspect the dopant area and identified successfully 0.4-μm misalignment between the active area layer and the p-well layer. This misalignment contributed to the mismatch of the current mirror and induced an abnormal shutdown current in the chip. The proposed method can maintain stable voltage conditions in the junction, thus facilitating dopant area inspection in SEMs. This letter has contributed to the development of an efficient method of inspecting dopant areas in real circuits.

Acknowledgment

The authors would like to thank the editor and reviewers for reading this manuscript and offering a number of helpful comments. The authors would also like to thank D. Su, Y. S. Huan, Y. T. Lin, and M. H. Wang for their kindly support and valuable discussion.

References

[1] J. F. Chen, K. S. Tian, S. Y. Chen, K. M. Wu, and C. M. Liu, “On-resistance degradation induced by hot-carrier injection in LDMOS transistor with STI in the drift region,” *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1071–1073, Sep. 2008.

[2] C. C. Cheng, J. F. Lin, T. Wang, T. H. Hsieh, J. T. Tzeng, Y. C. Jong, R. S. Liou, S. C. Pan, and S. L. Hsu, “Physics and characterization of various hot-carrier degradation modes in LDMOS by using a three-region charge-pumping technique,” *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 3, pp. 358–363, Sep. 2006.

[3] C. C. Cheng, K. C. Du, T. Wang, T. H. Hsieh, J. T. Tzeng, Y. C. Jong, R. S. Liou, S. C. Pan, and S. L. Hsu, “Investigation of hot carrier degradation modes in LDMOS by using a novel three-region charge pumping technique,” in *Proc. IRPS*, 2006, pp. 334–337.

[4] D. Venables and D. M. Maher, “Quantitative two-dimensional dopant profiles obtained directly from secondary electron images,” *J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct.*, vol. 14, no. 1, pp. 421–425, Jan. 1996.

[5] S. L. Elliott, R. F. Broom, and C. J. Humphreys, “Dopant profiling with the scanning electron microscope—A study of Si,” *J. Appl. Phys.*, vol. 91, no. 11, pp. 9116–9122, Jun. 2002.

[6] P. T. Liu, J. H. Lee, Y. S. Huan, and D. Su, “Application of secondary electron potential contrast on junction leakage isolation,” *Appl. Phys. Lett.*, vol. 95, no. 12, p. 122 105, Sep. 2009.

[7] M. Buzzo, M. Ciappa, M. Stangoni, and W. Fichtner, “Imaging and dopant profiling of silicon carbide devices by secondary electron dopant contrast,” *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 2, pp. 203–212, Jun. 2006.

[8] M. Buzzo, M. Ciappa, and W. Fichtner, “Secondary electron potential contrast for dopant profiling of silicon carbide devices,” in *Proc. IEEE ISTFA*, 2006, pp. 279–288.

[9] P. Kazemian, A. C. Twitchett, C. J. Humphreys, and C. Rodenburg, “Site-specific dopant profiling in a scanning electron microscope using focused ion beam prepared specimens,” *Appl. Phys. Lett.*, vol. 88, no. 21, p. 212 110, May 2006.