Novel Tunneling Dielectric Prepared by Oxidation of Ultrathin Rugged Polysilicon for 5-V-Only Nonvolatile Memories

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***Abstract*— A novel dielectric fabricated by thermal oxidation of ultrathin rugged polysilicon film is proposed for nonvolatile memories. Different roughness degrees for the top and bottom interfaces of this dielectric are detected by the atomic-force-microscopy (AFM) and high resolution transmission electron microscopy (HRTEM). Due to the microtips formed at the bottom interface of the dielectric, significant improvements in the high conduction efficiency, low trapping rate, good uniformity, and high reliability under positive gate-bias are obtained for the dielectric. Therefore, rugged polyoxide is promising for future 5-V-only floating-gate applications.**

RELIABLE thin dielectric films are urgently required for scaled 5-V-only floating-gate memories, such as advanced EPROM's, EEPROM's, and flash EEPROM's. Many researchers have claimed meeting the requirements for EEPROM manufacturing by using N_2O oxides or silicon rich oxides [1], [2], but many obstacles are necessary to be solved. Wu *et al.* [3] have also reported that the dielectric formed by oxidizing thin polysilicon will increase the tunneling efficiency. However, the time-dependent dielectric breakdown (TDDB) characteristic of this dielectric needs to be improved. Recently, the nature of rugged polysilicon has been extensively studied [4]. In this letter, a novel tunneling dielectrics grown on rugged polysilicon, which possesses a high electron conduction efficiency, a low electron trapping rate, stable interface states, and excellent reliability, is proposed for future 5-V-only nonvolatile memories.

(100) oriented, 2.5–3.5 Ω-cm, both p-type and n-type Si wafers were used. After RCA cleaning, a very thin rugged polysilicon film was then deposited using SiH_4 at 590°C for 40 sec in LPCVD system. The structural change to the rugged shape has been confirmed to occur around 590°C by the AFM images of these Si films deposited at various temperatures. The deposition and deposition pressure of the rugged polysilicon were controlled at about 60 Å/min and 100 mTorr, respectively. The deposition rate was roughly estimated by that the thickness of a quite-thick poly-Si film divided by

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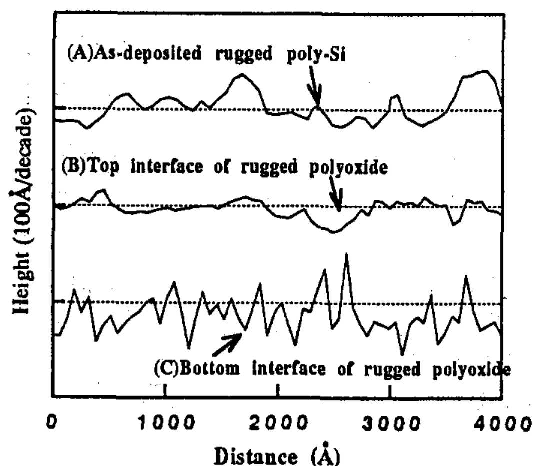

Fig. 1. Height profiles of various interfaces obtained by atomic force microscopy (AFM).

the deposition time. Subsequently, the wafers were oxidized at 900°C, which is below the viscous flow temperature of 950°C to quench the morphology of the as-deposited poly-Si, in pure O_2 ambient. Some bare silicon wafers were oxidized simultaneously and the resultant oxide thickness is 75 Å (TEM observation). After a 2500 Å-thick LPCVD poly-Si was deposited and subsequently $POCL_3$-diffused at 850°C for 30 min, the MOS capacitors were patterned to extract electrical characteristics. To avoid the charge depletion effect, positive ($+Vg$) and negative ($-Vg$) gate-bias measurements were conducted on n-type and p-type substrates, respectively.

Fig. 1 shows the height profiles of various interfaces obtained by AFM. The surface of the ultra-thin rugged poly-Si before oxidation exhibits a hemispherical-grain (HSG)-like surface from the 3-dimensional AFM photographs (not shown) and the curve A of Fig. 1. After oxidation, the rugged polyoxide is obtained because of the coarse surface of the silicon wafer. Obviously, the bottom interface of the rugged polyoxide is much rougher than the top interface, as shown in curve B and C of Fig. 1. This phenomenon is reconfirmed by the HRTEM photograph, as shown in Fig. 2. For the top interface of the rugged polyoxide, the topography changes mildly. However, for the bottom interface, the intermittent microtips are observed though the gross topography changes corresponding to the top interface. From Fig. 2, the oxide thickness above the asperity is about 65 Å.

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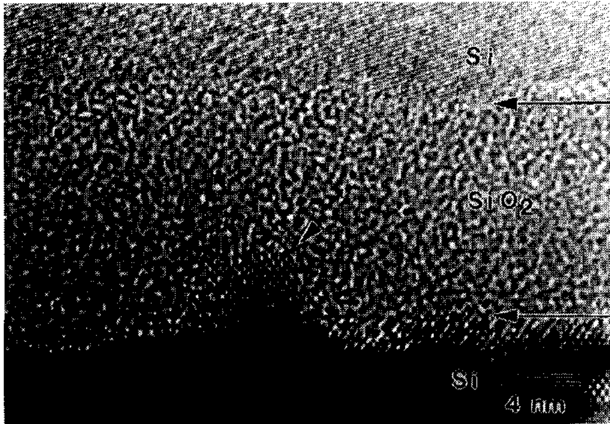

Fig. 2. High resolution TEM photograph of the rugged polyoxide.

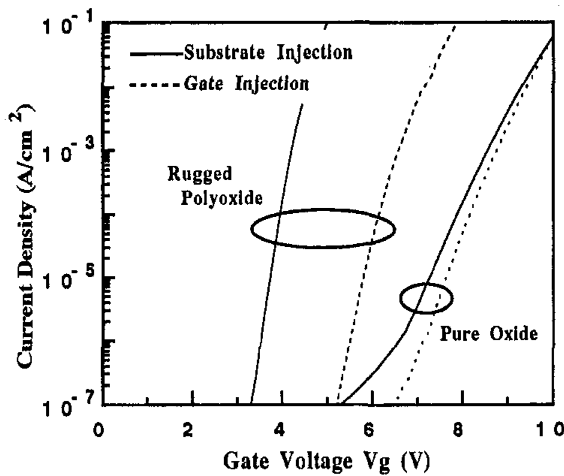

Fig. 3. I-V characteristics of the rugged polyoxide and pure oxide measured at positive and negative gate-bias for n- and p-type wafers, respectively.

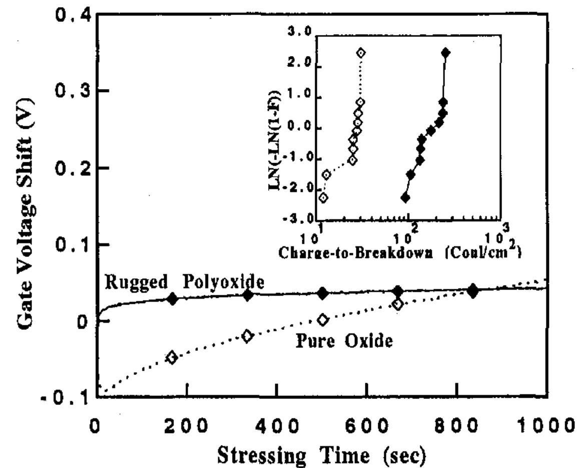

Fig. 4. The curves of the gate voltage shift versus stressing time of the rugged polyoxides under a constant current stressing of $+1$ mA/cm^2. The insert is the Weibull plots of the TDDB data at the constant stressing of $+100$ mA/cm^2 for the rugged polyoxides and pure oxides. The area of the capacitors is 3.14×10^{-4} cm^2.

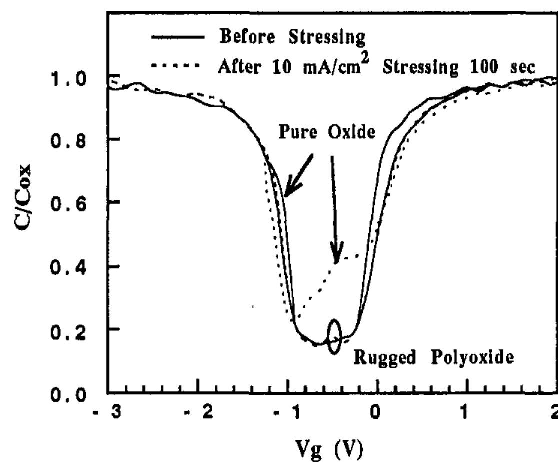

Fig. 5. The quasi-static CV characteristics of the rugged polyoxide and pure oxide before and after a constant current of 10 mA/cm^2 stressing for 100 s.

Fig. 3 shows the I-V curves of the rugged polyoxides and pure oxides. It is observed that the rugged polyoxides exhibit a much higher electron conduction efficiency than the pure oxide in both injection polarities. This high electron conduction will cause a significantly reduced voltage during writing/erasing cycles and make the 5-V-only application available. It is interesting that the electron injection from the bottom interface is much more efficient than that from the top interface. The reason is that the roughness of the bottom interface is much larger than that of the top interface, as shown in Figs. 1 and 2. This asymmetry of the leakage current is beneficial for the device operation. The spread in the voltage at a given current is ± 0.1 V for the rugged polyoxides and ± 0.06 V for the pure oxides, across a 3-inch wafer.

Fig. 4 shows the curves of the gate voltage shift versus the stressing time for the rugged polyoxides under a constant current stressing of $+1$ mA/cm^2. The pure oxide exhibits a positive and then negative charge trapping rate, but the rugged polyoxide demonstrates only a small electron trapping rate. It implies that the rugged polyoxide has a better immunity to the charge trapping under positive gate-bias stressing. The insert of Fig. 4 is the Weibull plots of the TDDB data at the constant stressing of $+100$ mA/cm^2 for the rugged polyoxides and pure oxides. Evidently, the rugged polyoxides exhibit about an order of magnitude higher reliability than the pure oxides under $+Vg$ stressing. As shown in Fig. 2, because the field enhancement of the microtips, most electrons flow via the microtips, where the oxide thickness is thinner, to the anode during the stressing. Furthermore, it has been reported [5] that the trapping rate is reduced as well as the TDDB characteristics is improved when the oxide thickness decreases. Therefore, injection on the small effective area with small oxide thickness that will cause a lower bulk field are the main factor to improve the charge trapping properties. Fig. 5 shows the quasi-static CV (QSCV) characteristics of the rugged polyoxides and pure oxides before and after a constant stressing of $+10$ mA/cm^2 for 100s. The initial midgap interface state densities ($D_{\rm itm}$) is 3.9 $\times$ 10^{11} eV^{-1} cm^{-2} for the rugged polyoxide and analogous to that of the N_2O-oxynitride. For the rugged polyoxides, no

significant degradation is observed in the QSCV curves after the stressing. In contrast, for $-Vg$ stressing, because the field enhancement through the local very-thin oxide doesn't exist, the behavior of charge trapping and reliability is similar to that of the polyoxide [6], [7]. The details should be further studied.

Because the microtips at the bottom interface are formed after the oxidation of the thin rugged polysilicon, the dielectric proposed in this letter possesses a low electron trapping rate, high conduction efficiency, and excellent reliability.

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