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Innovative methodologies of circuit edit by focused ion beam (FIB) on wafer-level chip-scale-package (WLCSP) devices

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Abstract As packaging technology advances to wafer level chip scale packaging (WLCSP) to enable reduced chip size and manufacturing cost, circuit edit has become a critical issue for the fully packaged integrated circuits (ICs). These advanced package types cannot be rebuilt on a single chip; therefore, function testing after circuit edit of WLCSP faces challenges. Furthermore, there are routings at the redistribution layer of WLCSP ICs. Circuit edit was applied on both the chip and the package level. In this paper the focused ion beam was applied to mill the organic material of the package structure to expose underlying ICs, instead of chemically destroying the packaging. Metal line cutting and conductive path deposition were also developed by a beam-based technique. These new approaches make the direct edit of electrical circuitry possible not only in ICs but also at package level. Therefore, for the debug process and for failure analysis, the WLCSP ICs have negligible damage and negligible signal integrity loss by retaining the original packaging structure.

1 Introduction

During the past 10 years, the wafer-level chip scale package (WLCSP) has developed an advanced package for low to mid-I/O devices, generating complete packaged and tested chips on wafer prior to dicing. This technology provides the smallest possible package close to the original die size. WLCSP provide an approach with a lower cost in manufacturing and testing than conventional single-chip packaging. In addition, the WLCSP scheme effectively decreases the overall circuit length between die to printed circuit board; therefore, it enhances transition efficiency of the high-frequency signal. This packaging technique uses a redistribution layer (RDL) to route to a ball grid array on whole chip area from the edge of die. Thus, the RDL offers a number of significant advantages: (1) improved electrical speed; (2) better mechanical properties of packaging level; (3) eliminating the use of underfill; (4) optional space to contain passive component embedded in the chip. A review of literature reveals that WLCSP has been increasingly applied to portable electronics, such as cellular phones, e-readers, and Pads' etc. [1]. However, WLCSP causes the circuit edit (CE) to be more difficult since it is performed on a fully packaged device. Conventionally, a focused ion beam (FIB) is employed to edit the circuits of a device, and to modify electrical interconnects inside a device from its front-side [2, 3]. Unlike wire bonding packages, WLCSP devices have a thick RDL consisting organic materials and metallic interconnect, and thus these materials form a barrier for the CE from the front-side of ICs. An alternative CE technique is backside editing, which is applicable for the high performance device such as logic ICs, ASIC and MPU [4–6]. But the problem is that the pattern density is much greater at IC lower metal layer, and it is difficult to find the edit target. That is, the application would be limited to the ICs original structural characteristics. As a result, the whole packaging structure protecting a chip must be removed firstly. Therefore, CE on a WLCSP chip always requires numerous sample preparation steps for the

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removal of packaging structures. When the CE finished, the processed bare IC must be packaged again to subsequent functional testing on electrical signals. However, the packaging removal was an irreversible process for WLCSP. Even though the conventional re-packaged technique, such as wire bonding, has been developed maturely, and it can be applied to the edited WLCSP ICs, the electrical properties of re-packaged ICs would drift from its original design because the packaging architectures are changed.

To develop a direct CE without removing packaging structure is essential. Yet, the challenge is that a long trenching time must be spent to contact circuit nodes directly on chip surface from the topside of packaging structure. In comparison to IC's passivation layers, the passivation layers of WLCSP are quite thick. Therefore, this process is not only time-consuming but also destructive to an IC device due to heat accumulation of the ion energy. Long ion milling time may lead to a damage of circuit in the chip level. Additionally, trenching through thick organic passivation layers on package level brings new challenges to chemistries used in FIB. CE was performed in direct access from the WLCSP surface to the IC front-side circuit nodes. To maintain the completeness of WLCSP, developing the techniques of direct CE on a fully packaged WLCSP device is essential. This paper aims to explore several innovative methodologies enabling direct CE and debugging on both chip and package levels on a fully packaged WLCSP IC. This study will lead a better application in CE for the advanced ICs. The electrical characteristics also would be remained intact and produce reliable analysis results.

2 Experimental

A schematic cross-section structure of the WLCSP contains redistribution with two dielectric layer is shown in Fig. 1. It can be seen that the WLCSP is situated on the bare chip. A lead-free solder ball, as electrical joint, was placed on under bump metallurgy (UBM) by electroplating or printing. The UBM was sputtered and consisted of gold, nickel and copper on a contact opening of 200 μm in diameter. The RDL connects the IC I/O pad to the UBM. RDL consists of electroplating copper and sputtering gold, and it functions as an interconnect, and embedded in the passivation material. The passivation materials usually are organic-based polymers, such as polyimide (PI) and benzocyclobutene (BCB). The thickness of the copper interconnect is 9 μm, and the line width is 200 μm. The width of the whole packaging structure ranges from 40 to 290 μm. The results reported in this article were obtained from WLCSP devices supplied by MaxRise Inc. in Taiwan.

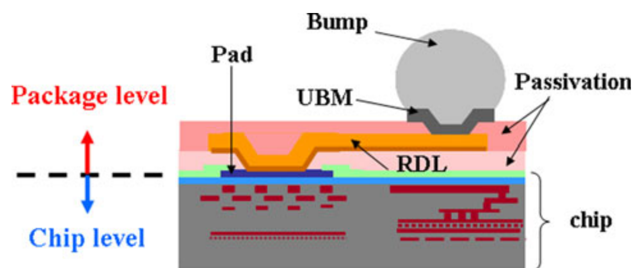

Fig. 1 Schematic illustration of a cross-sectional structure of WLCSP

As shown in Fig. 2, the CE procedure by FIB involves several steps. The region of interest was firstly approached by laser milling by deep trenching through passivation materials, which usually consisting organic compounds, The laser milling tool utilized to prepare the sample was Wentworth Laboratories Pegasus 300FA with wavelength of 355 nm. Traditionally, large area laser milling was adopted so that the FIB trenching time can be reduced. However, laser pre-removal is hard to manage due to the transparency of organic passivation. Thus, deep trenching to access the metal line of interest is the only practical option. Because the organic passivation materials are very thick, a chemical process is employed for etching through them. Bulk package passivation materials are removed locally to the IC passivation level by using FIB system. Then, milling through the dielectric materials and IC passivation layer need to be done in order to access the metal level.

To expose the target metal line inside the IC, the intermetal dielectric (IMD) must be removed firstly. We use a gas-delivery FIB system with a high etching rate to trench through IMD. After that, deposition of several microns of Pt is required for interconnection. Finally, circuit modification may be achieved by combining the steps mentioned above for cutting and connection. In this study, we used an FEI gas-injection system (GIS) V600 containing IEE, Idep2, and Pt etc. gases for these experiments.

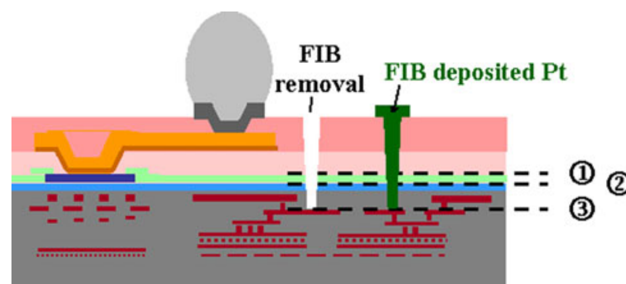

Fig. 2 Schematic diagram of FIB editing process for a WLCSP IC

3 Results and discussion

Development of direct CE by FIB on a fully packaged WLCSP device is firstly investigated. Figure 3 shows an etched deep trench through the package passivation layers, which requires a long trenching time. These trenches were etched with the following process parameters: chamber pressure is 2.66×10^{-6} mbar, beam current is 2.8 nA, ion acceleration energy is 30 keV, and delivered gas is IEE. As can be seen from Fig. 3, the opening area of the ion-milled trench was 4.87 µm by 7.47 µm, whereas the depth of the trench is approximately 43 µm. The highest aspect ratio of the ion-milled trench was large than 10. As it can be seen, the ion-beam milling featured extremely sharp and deep etching ability on the organic substrate. No any burnout or decomposition was found after the milling process. Conventionally, accessing IC metallic interconnect through a thick organic layer of WLCSP was usually hard to achieve. The challenge is that the wall of the deep trench must be maintained around 85–90° in vertical direction to allow ion-beam continuously incident to the bottom circuit. According to a review paper published by Micron, a long milling time would result in ion accumulation that may lead to serious trench deformation [7]. However, the approach we used can avoid the deformation and unnecessary deposition. Furthermore, during this time-consuming procedure, ion bombardment may damage the ICs. In the experimental results, the accumulation-induced damage can be ignored. By increasing the milling time and repeating the procedure with the above parameter, the target metal lines of IC can be exposed successfully without any damage caused by charging effects as shown in Fig. 4.

Due to the operating area at the trench bottom is deep and narrow, line cutting before Pt deposition can minimize the alignment step without metal redeposition. We can successfully cut the target metal line and perform the modification of circuits. The following circuit edit can be seen in Fig. 4a shows the cutting of the target metal line. Firstly, point C was cut by ion beam. Secondly, the reactive chemicals were introduced into the FIB chamber by gas injection system. Then a Pt metal line was deposited between point A to point B as the interconnect line. The finished edited circuit of the WLCSP IC is shown in Fig. 4b.

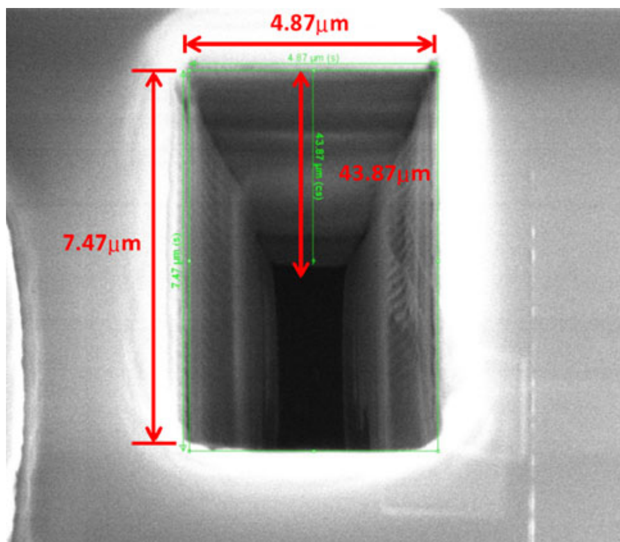

Fig. 3 FIB micrograph of package passivation removal in a fully packaged WLCSP device to expose IC metal. The opening trench area is 4.87 µm × 7.47 µm, whereas the depth is approximately 43.87 µm

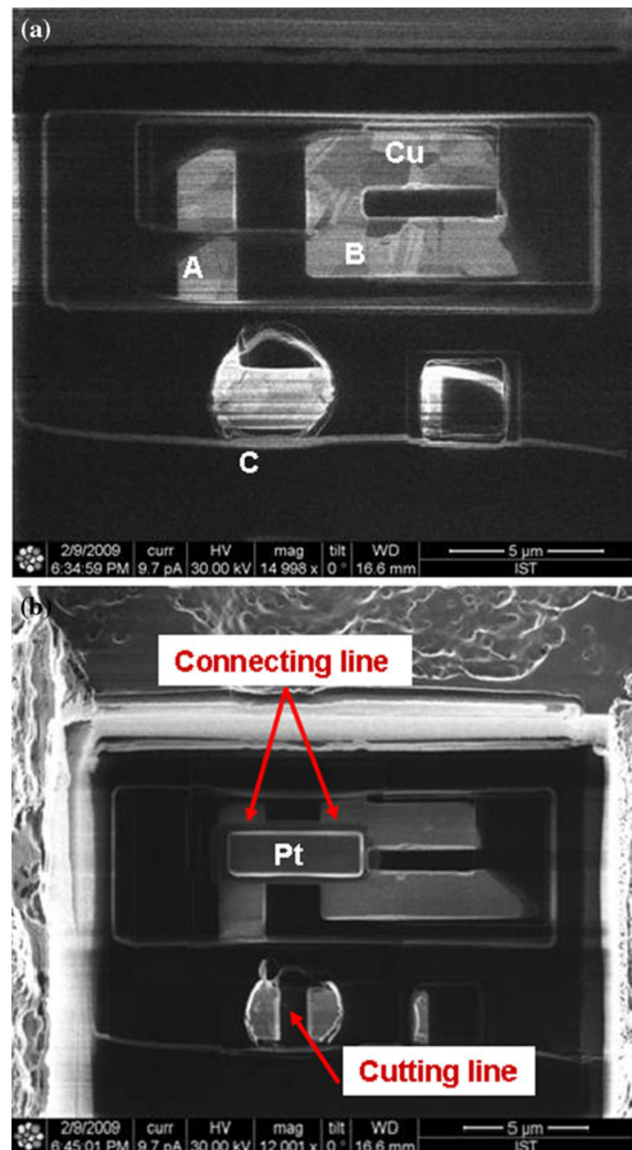

Fig. 4 **a** FIB micrograph of exposing three IC metals at edit location. **b** FIB micrograph of deposited Pt metal cross two metal line to form an interconnect on a fully packaged WLCSP IC

It is noteworthy that the results demonstrate that direct CE without the removal of package-level materials is feasible; however, the edit path is usually hindered due to the neighboring dense patterns. An alternative method is to connect the two far locations on packaging surface to produce the path of a new circuit. Figure 5 presents a successful circuit edit on a fully packaged WLCSP device. All the three trenches shown in Fig. 5a were etched for approximately 50 min. The two voids on the top surface of the package passivation were FIB marks, which functioned as markers to the milling target. One metal line at the middle location of bottom trench was cut. Then, Pt metal was filled into the two ultra-deep trenches in the figure. To prevent void formation in the long deposited metal line, the process should be separated into several steps. Dense Pt lines are eventually formed then connect on the package surface. Figure 5b shown that the original layout was modified successfully by the new interconnects.

The approaches proposed above offer a wide range of debugging applications. With deep milling capability, creation of probe pads on a fully packaged WLCSP device is also possible. Pad creating involves two steps. The first step is the removal of the package passivation above metal lines, and the second step is to deposit a new pad on the surface of an IC or package. The two cases can be seen in Figs. 6 and 7 in which creation of probe pads are done on IC metal by large area local removal and high aspect ratio trenching, respectively. The target metal line exposes in the top area of Fig. 6a. As shown in Fig. 6b, creation of a probe pad on chip level is made accessible by extensive removal of bulk WLCSP passivation materials. Figure 7a

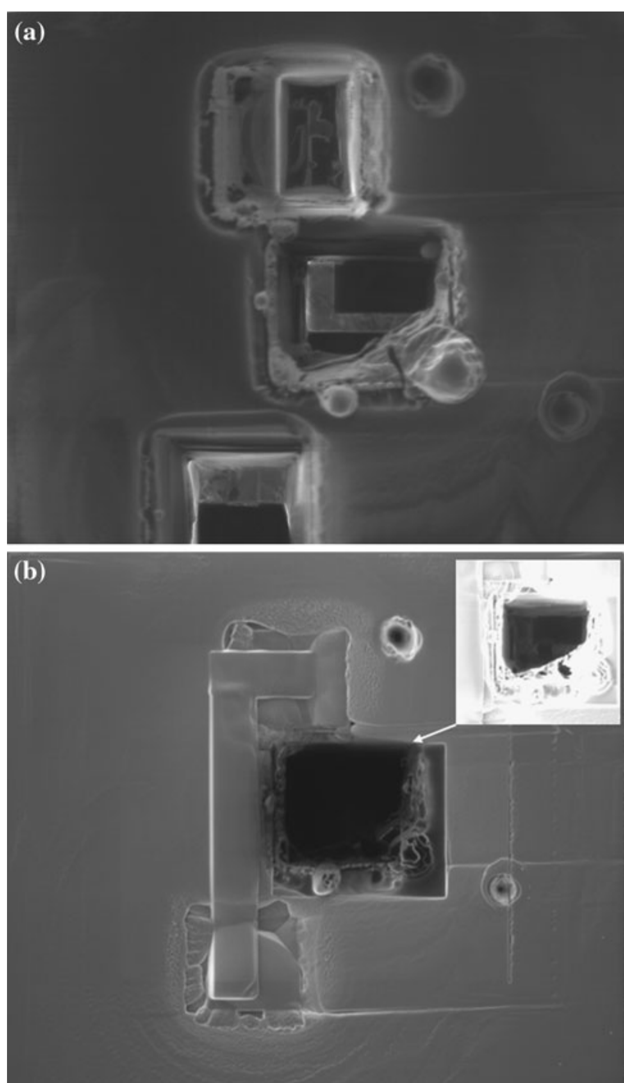

Fig. 5 **a** FIB micrograph of three trenches exposing two IC metals at edit location. **b** FIB micrograph of direct circuit edit performed on a fully packaged WLCSP IC. The inserted diagram on the *top right* area shows a metal cutting by gas-enhanced etching

Fig. 6 **a** FIB micrograph of target IC metal exposure. **b** FIB micrograph of creation of probe pad on target IC metal

shows the target IC metal line exposure via high aspect ratio trenching through bulk WLCSP passivation materials. From Fig. 7b, it can be seen that a probe pad of IC metal line is successfully performed. We can probe nodes not only at inside chip but also at package surface with a turnaround time short enough for debugging. Most importantly, the device behavior is minimally impacted by the FIB edit.

In contrast to traditional package, the location of I/O design on WLCSP is performed by means of RDL. The RDL extend the layout from the die edge to the centre area. In other words, RDL role as interconnect in package layer; as a consequence, circuit edit on package level is essential for WLCSP. Rewriting RDL on package level by FIB milling and deposition is critical to quick verification of the I/O design. As mention above, trenching through thick package passivation is practical. It seems achievable to edit RDL by developed techniques. First, localized access is achieved by exposure of the RDL Level. As it can be seen in Fig. 8a, target RDL exposes successfully by FIB milling. Prior to attempting a RDL edit, it is necessary to overcome the technical issue of RDL cutting. The difficulty of RDL cutting is due to the sizable width and thickness of RDL as compared with IC metal lines. FIB cutting of RDL presents challenges including not only time-consuming milling but also rapid redeposition of copper (Cu). Research work has reported that the application of FIB milling on Cu metal line presents a challenge including redeposition [8]. To avoid metal shorting caused by Cu redeposition, the two procedures should immediately follow the FIB cutting. One

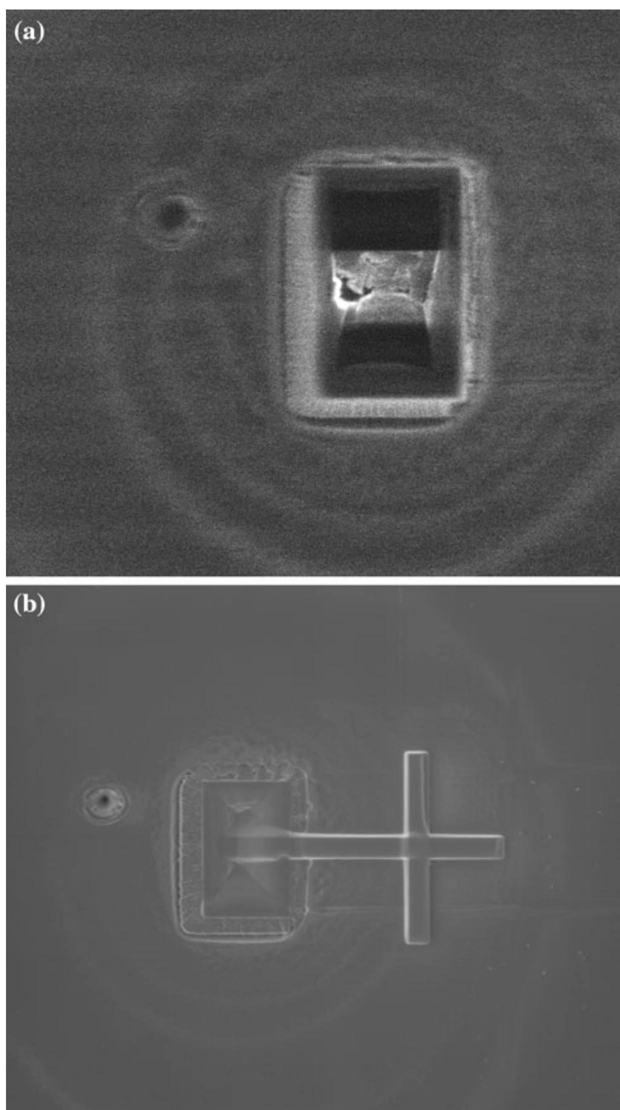

Fig. 7 **a** FIB micrograph of target IC metal exposure by local deep FIB milling. **b** FIB micrograph of creation of probe pad on the surface of passivation layer

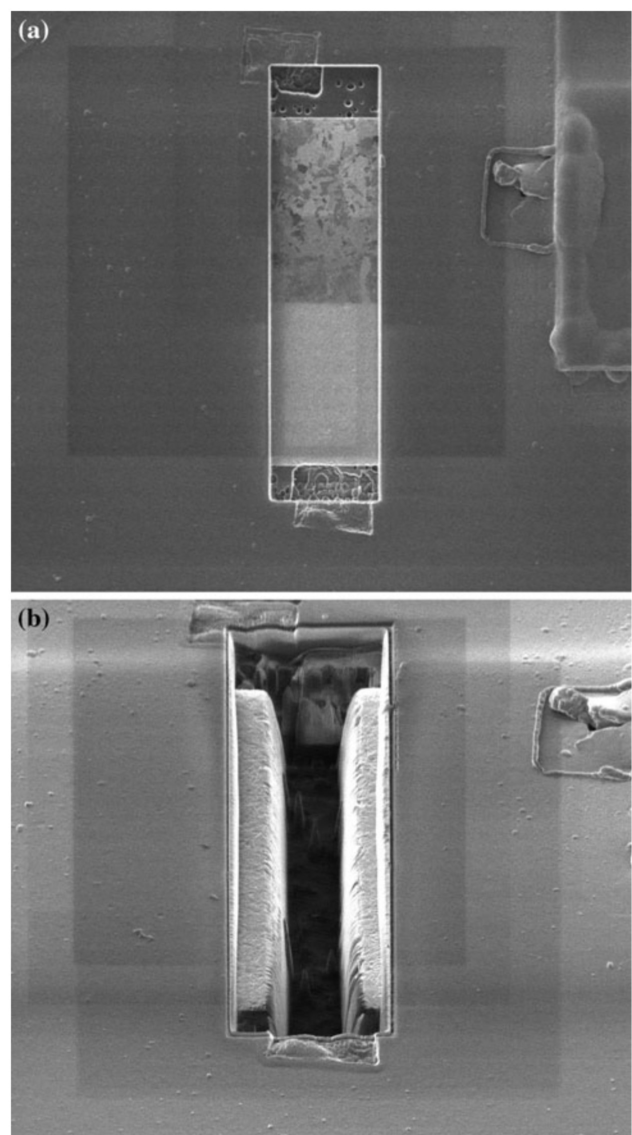

Fig. 8 **a** FIB micrograph of RDL metal exposure. **b** FIB micrograph of RDL metal cutting. No residues of Cu bridge the cut RDL

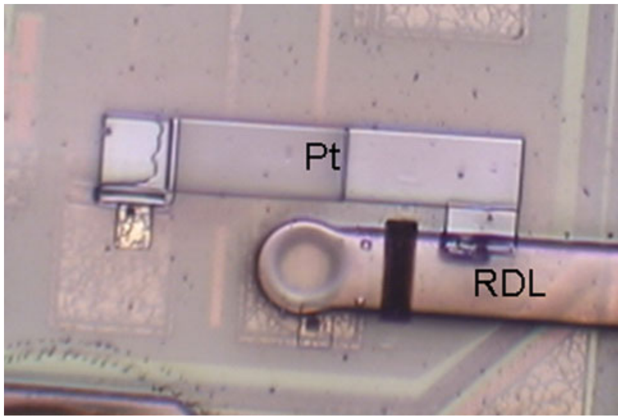

Fig. 9 The corresponding OM image of the RDL circuit modification

is removal of metal residues, and the other is insulator deposition. From Fig. 8b, it can be shown that no Cu residues appear in the FIB cutting region. After overcoming the challenges, we could perform a circuit modification on package level by means of the established FIB techniques for cutting and connection. As shown in Fig. 9, RDL repair connecting to the other IC pad is done by FIB induced deposition of Pt. Hence, the I/O site can be edited on a fully packaged WLCSP IC, and the electrical testing can be done as well.

4 Conclusion

To summarize: the results reported in this paper demonstrate that the limitation of circuit edit can be overcomed via direct FIB editing of WLCSP IC. The developed innovative methodologies can be implemented to modify the designed circuit on both chip and package level on a fully packaged WLCSP. In spite of the difficult tasks facing the IC design, circuit edit and creation of probe pads on not only IC metal line but RDL of packaging is indeed possible. The techniques developed herein can offer a wide range of application to circuit design, debugging, and failure analysis. The limitation, however, concern the methodologies reported in this study, that is, the solder balls must be removed carefully to access the target metal line if they cover the edit region. The consequence of impossibility of re-bumping the solder ball is that the passivation layer is easily damaged in SMT process. Thus, the electrical testing following circuit edit is a consideration. More advanced instrumentation is also necessary to support navigation during the circuit edit. Future research work on the subjects mentioned above is obviously indispensable.

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