Single-Crystal Silicon Nanostructure Fabrication by Scanning Probe Lithography And Anisotropic Wet Etching

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Abstract

Silicon nanostructures have been demonstrated by electric-field-enhanced localized oxidation on single crystal silicon wafer using a scanning probe microscope (SPM). In this study, we have demonstrated the use of scanning probe lithography (SPL) and orientation-dependent etching (ODE) can easily obtain nano-wire and nano-gap down to 24nm and 60nm on (110)-oriented silicon substrate. The scanning probe lithography (SPL) provides high resolution, which can be adjusted by tip bias, tip set force, scanning speed, and ambient humidity of environment, without damage in the substrate. The etching process employed the orientation-dependent etching (ODE), because of the etching rate of the (111)-plane is slower than any other crystallographic planes such that anisotropic etching profile can be obtained. The experimental samples were hydrogen-passivated by dipping in 10% aqueous HF solution to remove sample native oxide on the surface before SPM localized oxidation process. The SiO_x nano-patterns on (110)-oriented silicon substrate were generated by SPM localized oxidation. Then, the etching process employed the ODE with a 34 wt.% aqueous KOH solution. The nano-wire feature size is easily down to 24nm and aspect ratio larger than 4:1. The optimization line/space nanostructure is about 20 nm / 80 nm and the nano-gap is about 60nm. In this study, we also have demonstrated the influence of etching temperature on the feature size of nanostructures with same aspect ratio. At the same etching depth (100nm), the line-width decreases with increasing the etching temperature. The theoretic etching rate and experimental etching rate are proportional to temperature, the higher temperature the higher etching rate.

Keywords: nanostructure; scanning probe lithography (SPL); scanning probe microscope (SPM); localized oxidation; Orientation-dependent etching (ODE); KOH wet etching

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1 Introduction

As the trend of integration circuits (IC) industry, the sizes of electron devices and microelectromechanical systems (MEMS) are shrunk to nanometer-scale currently. Scanning probe lithography (SPL) techniques such as the scanning tunneling microscopy (STM) and the atomic force microscopy (AFM) have been widely investigated in nanostructures and nanofabrication technology. A number of investigators had studied this process in variety of applications including the direct writing of an oxide pattern for using as an etching mask, and the fabrication of metal and silicon based nanoelectronic devices [1,2,3].

In order to fabricate nanometer-scale structures, lithography and etching system with highly reliability and lower cost are required. To the lithography system of nanostructure fabrication, the most important issue we are facing is how to control critical dimension (CD) in nanometer-scale stably. To the etching system, the issues are the accurately transference of the mask patterns and highly uniform etching rate.

In this study, we have successfully demonstrated that the atomic force microscope (AFM) is used to define the desired patterns on the sliced single crystal silicon samples. The process with AFM to define patterns is to use the tip-induced localization oxidation. Then potassium hydroxide (KOH) orientation dependent etching (ODE) is introduced to transfer the patterns into the underlying single crystal silicon layer after patterns definition. Etching of them provides higher reliability and lower cost in nanometer-scale fabrication.

2 Experiments

In this study, silicon samples of experiment were sliced from n—type (110)-oriented 4 inches silicon wafer with 1~10 ohm-cm resistivity. Before samples sliced, the wafers were cleaned by standard RCA cleaning. Then sliced samples were dipped into 10% HF solution to remove native oxide for 20 sec and to form a hydrogen-passivated surface. This passivated layer prevents the formation of native oxide rapidly. The surface roughness of passivated sample is around 0.5 ~1 nm measured by atomic force microscopy (AFM).

2.1 Scanning Probe Lithography (SPL)

In this study, localization oxide patterns were performed by a commercial AFM/STM microscopy (M5 type, Park Scientific Instrument) in the open environment [4]. The patterning tip uses a highly doped silicon cantilever tip with resistivity 0.01~0.0025 ohm-cm and the diameter of tip is around 10~20 nm. The schematic of scanning probe lithography (SPL) is shown in Figure 1. The four parameters including sample/tip bias, scanning speed, tip contact force, and environment humidity are concerned for defining patterns by SPL. Because the humidity is an important parameter in controlling the resolutions, the resolution becomes worse with increasing humidity. So the environment humidity is stably controlled at 45 ± 1% during the time of SPL localization oxidation.

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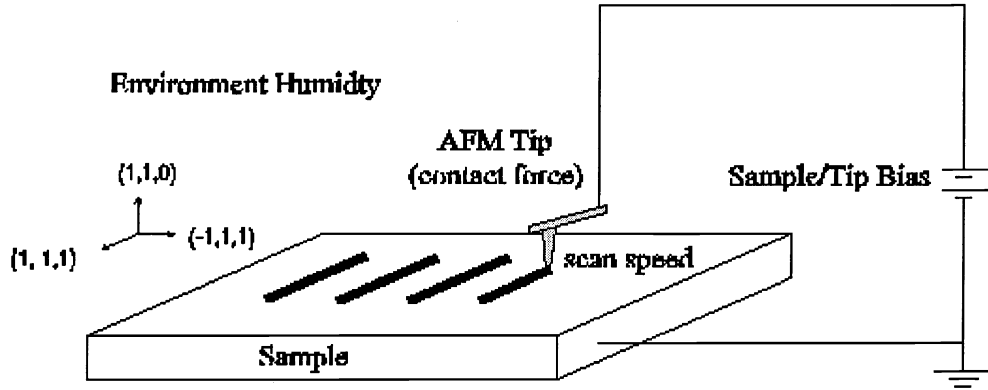

Figure 1 The setups of scanning probe lithography (SPL).

2.2 Orientation Dependent Etching (ODE)

The patterns were transferred into silicon by employing the orientation-dependent etching (ODE) method with the potassium hydroxide solution (KOH). It is well known that single crystal silicon is diamond structure and the different oriented plane has different atom density. In the $\{100\}$ and $\{110\}$ planes, there are two dangling bonds and two Si – Si back bonds per surface atom. In the $\{111\}$, there are one dangling bond and three Si – Si back bonds per surface atom. The Si surface oxidation caused by hydroxyl ions on $\{100\}$ and $\{110\}$ planes have the lower activation energy than $\{111\}$ plane. In other words, the etching rates of $\{100\}$ and $\{110\}$ planes are higher than that of $\{111\}$ plane [8]. Based on the different etching rates, the KOH wet etching of single crystal silicon performs the phenomenon of anisotropic etching, which results in the vertical sidewall of nano-gridline structure and higher aspect ratio.

3 Results and Discussion

In this study, the scanning probe lithography (SPL) and orientation dependent etching (ODE) were introduced for nanometer-scale fabrication. The main influence of the SPL is Sample/Tip bias, which will be discussed. The temperature influence and nanostructure fabrication will be discussed in the subsection, too.

3.1 Scanning probe lithography (SPL) control

For discussion the influence of sample/tip bias in a constant scanning speed (1 μm/sec), the ambient humidity and constant force are maintained at 45% and 10 nN, respectively. The relationship between the electric field and the applied voltage can be expressed as [4,5,6]:

$$E = \frac{a(a+b)(a+2b)}{b[(a+b)^2+\rho^2]^{\frac{3}{2}}}V, \tag{1}$$

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where a is the tip radius, b is the distant between tip and sample, V is the tip voltage, and ρ is the radial distant on the sample (with the tip above the origin of the sample plane). Figure 2 shows the result of the sample/tip bias variety from –6V to –10V and the scanning speed was maintained 1μm/sec. The oxide thickness combination of two parts, one is the oxide height and the other is the oxide depth. It is believed that localization oxide is formed by oxygen provided from water gas of environment. The electric fields induced by sample/tip bias force the oxygen ions to penetrate into the silicon surface, and stop by nuclear and electron collisions that form oxide depth. Then the penetrating oxygen store in silicon sample, and results in the expansion that form oxide height. According to Figure 3, it is demonstrated that the total oxide thickness is proportional to the electric fields induced by sample/tip bias.

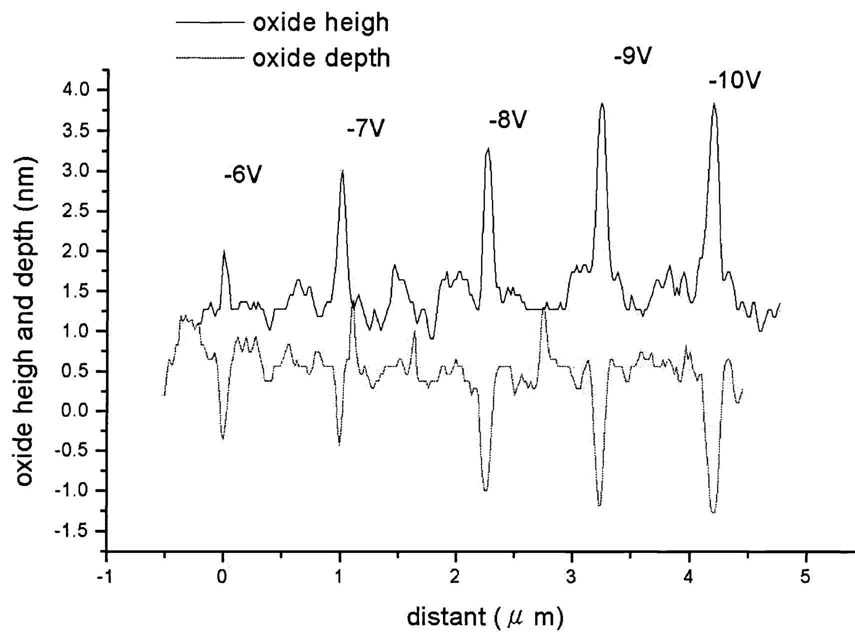

Figure 2 Cross-section profiles of oxide thickness measurement by AFM.

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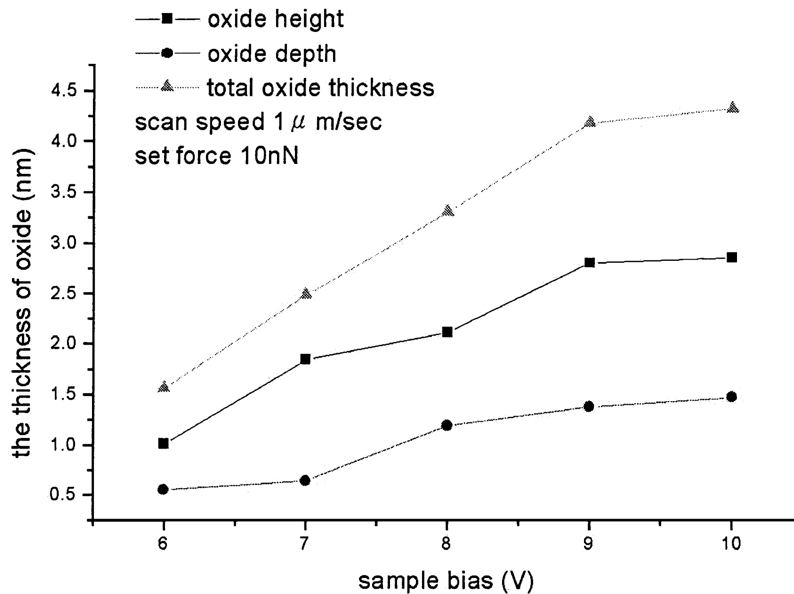

Figure 3 Comparison of oxide thickness and sample/tip bias.

3.2 Temperature influence of orientation dependent etching (ODE)

After patterns definition by scanning probe lithography localization oxidation, the patterns transference process was employed the orientation dependent etching (ODE) method with 34% KOH solution. The etching rate is given by the equation [7,8]:

$$R = R_0 \times \exp(-\frac{E_a}{kT}) \quad , \tag{2}$$

where R_0 is the pre-exponential factor coefficient, E_a is the activation energy, k is the Boltzman constant, and T is the absolute temperature. According to equation (2) and section 2, the activation energies of {111}, {100}, and {110} planes (0.52, 0.40, 0.33 eV) are different that result in different etching rates respectively at the same temperature. Figure 4 shows the vertical sidewall gridline etching at 50 ℃, which is formed by the different etching rates of {110} and {111} planes. Further more, we introduced the influence of etching temperature. It is found that etching rate ratios of {110} and {111} are 200 at 30 ℃ and 150 at 50 ℃. So the higher etching temperature results in shrinking phenomenon of the linewidth. However, the oxide mask also influences by temperature, that result the gridline patterns linewidth decreasing from 70 nm to 30 nm when the etching solution temperature increases from 30 to 50 ℃. In Figure 4 and Figure 5, the gridline linewidthes are 30 and 70 nm and the both of height is about 100 nm. Figure 6 shows the experimental and theoretical comparisons of the etching rate with different etching temperatures. It also includes the linewidth shrunk with etching temperature.

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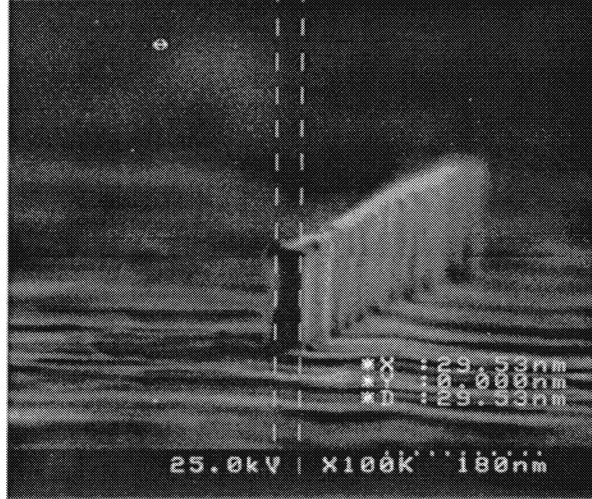

Figure 4 The sidewall SEM picture, gridline etching at 50°C.

Figure 5 The sidewall SEM picture, gridline etching at 30°C

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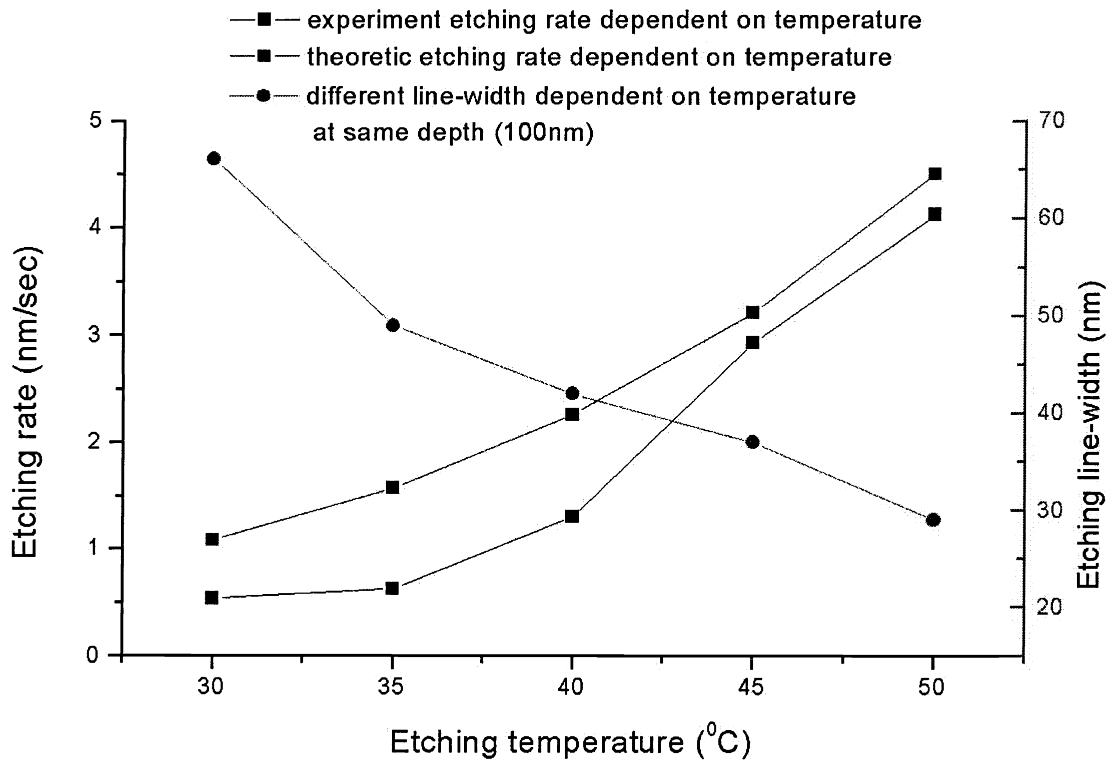

Figure 6 The experimental and theoretical comparisons of etching rates with different etching temperatures, and the linewidth shrunk with increasing etching temperature.

3.3 Nanostructure fabrication

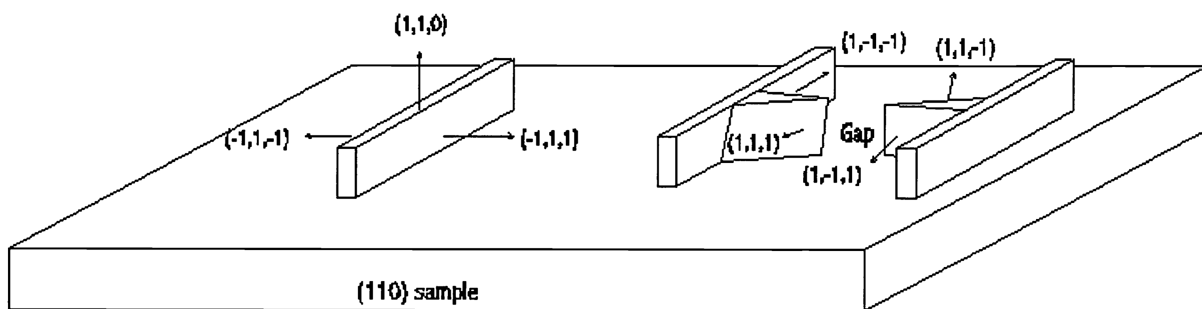

Figure 7 Some important planes on the (110)-oriented silicon sample.

For many mechanical sensor applications, single crystal Si, based on its intrinsic mechanical stability and feasibility of

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integrating sensing and electronics on the same substrate, often presents an excellent substrate choice. On the (110) silicon substrates, some important planes in the silicon lattice are mentioned in the Figure 7. There are three pairs of {111} planes on the (110) sample that we found. There are only (1, -1,1), (1, -1, -1), (-1,1,1), and (-1,1, -1)-oriented perpendicular to (110)-oriented. It is suitable to fabricate nano brush shown in Figure 8. The linewidth is about 20 nm and the space width is about 60~70 nm. Figure 9 shows the other structure, which uses (1,1,1) and (-1, -1, -1)-oriented to enclose a 109.47° angle with (110)-oriented.

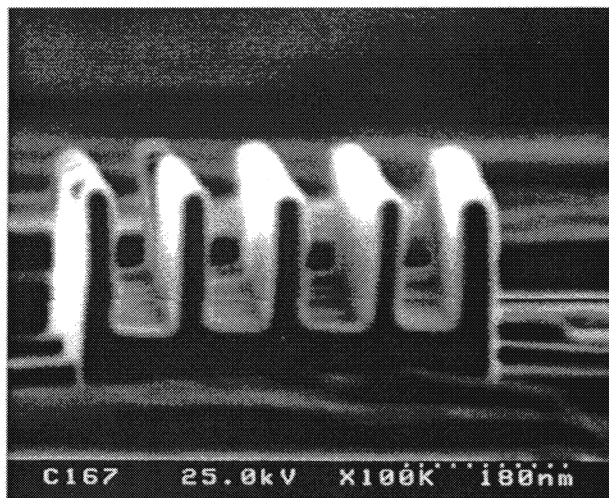

Figure 8 Cross-section SEM picture of fine line/space nanostructure.

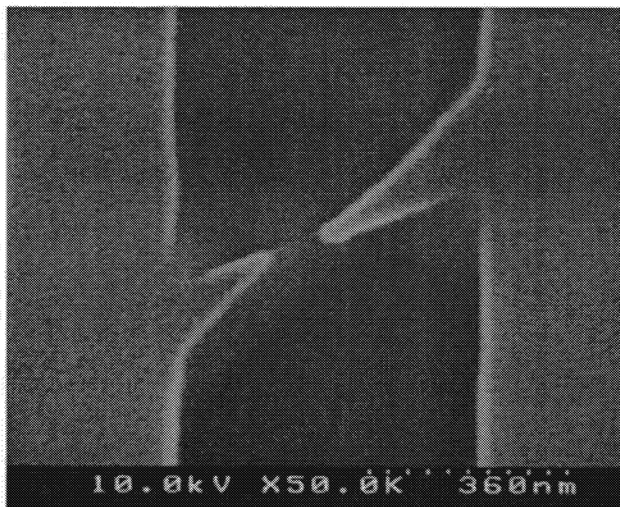

Figure 9 Top-view SEM picture of nanostructure.

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4 Conclusion

We have successfully that demonstrated the scanning probe lithography (SPL) is highly repeatable and reliability in nanometer-scale patterns definition. We also demonstrated the low-cost KOH solution wet etching systems with orientation dependent etching (ODE) method that perfectly performs the feature size of nanostructure shrunk below 30nm, and other nanometer-scale structures. It is believed that the integration of SPL and ODE processes will be widely investigated and used in nanoelectronic devices, biotechnology, and nanoelectromechanical systems (NEMS).

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