Smart Dielectrics of Fluorinated Silicon Glass Prepared by Liquid Phase Deposition Method

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ABSTRACT

Fluorinated silicon glass (FSG) film prepared by using liquid-phase deposition (LPD) is very potential for use as a smart dielectric owing to its high fluorine concentration (8.6 at %), low dielectric constant (3.46), low stress (43 Mpa), low leakage current density (4.6E-9 A/cm^2 at 2 MV/cm) and low deposition temperature (room temperature). By temperature difference and conventional water-adding methods, the LPD technologies and the key process parameters affecting the physicochemical properties and the electrical characteristics will be introduced. Furthermore, the LPD FSG has been applied as gate oxide to MOSFET's and polysilicon TFT's. Owing to its novel property of selective deposition, LPD FSG has been also employed to cap the sidewalls for degradation-free damascene trenches, and to fabricate micro contact holes for the n^+/p diodes and the Schottky diodes.

Keywords: LPD、FSG、selective、dielectric、damascene、RIE

1. INTRODUCTION

The formation of silicon dioxide (SiO_2) with low-temperature process (LTP) has already played an important role in microelectronic technologies, while high-temperature process can redistribute impurities and generate defects. Conventionally, CVD methods are the most typical to form LTP SiO_2. However, the high quality CVD SiO_2 usually requires complex process control and expensive equipment. In recent years, much attention has been paid to the liquid-phase deposited (LPD) oxide technology[1~3] for its room temperature process and much simple process control. Since fluorine atoms are naturally incorporated into the film during deposition, the fluorinated silicon glass is named LPD FSG ($SiO_{2-x}F_x$).

Liquid-phase deposition (LPD) can be a very novel process for future microelectronic/MEMS fabrication because (i) it is a room-temperature process, (ii) it never has plasma damage on material surface or the underlying devices, and (iii) FSG can be selectively deposited on silicon or silicon oxide instead of on photoresist, SiN or metal[4~10]. In this paper, we will introduce the essential process technology, physicochemical and electrical properties of LPD FSG. And then we will also introduce the applications of LPD FSG as gate insulator to LTP poly-Si TFT's and MOSFET's. In addition, we will introduce selective liquid-phase deposition (S-LPD) technology, and its applications to degradation-free damascene trenches for low-K Methylsilsesquioxane (MSQ), and to the formation of damage free micro contact hole.

2. PROCESS OF LPD FSG

To form FSG by using LPD method, the supersaturated silicic acid solution has to be prepared. As shown in Fig.1, two methods can be adopted to prepare the supersaturated silicic acid solution. The first one is conventional LPD (C-LPD). 70g of high purity (99.99%) silica powder (SiO_2) is added into 1,500ml 4mol/l H_2SiF_6 solution. After being stirred at 25°C for 17 hrs, the solution can become saturated with silicic acid [$Si(OH)_4$]. After removing the undissolved silica with filter and adding deionized water (H_2O), the originally saturated solution will become supersaturated. The second one is temperature-difference LPD (TD-LPD). Saturated silicic acid ($Si(OH)_4$) is mainly prepared at 0°C, and then heated to 25 °C for 1 hr to become supersaturated.

3. PROPERTIES OF LPD FSG

3.1. PHYSICOCHEMICAL PROPERTIES:

Figure 2 shows a typical FTIR spectrum for LPD $SiO_{2-x}F_x$ and thermal oxide, respectively. The absorption bands around 1090 cm^{-1} and 810 cm^{-1} are due to the Si-O-Si vibration. These absorption bands, which are similar to those found in the spectra of thermal oxide, indicate that LPD $SiO_{2-x}F_x$ is amorphous in structure. Another main absorption

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band around 930 cm^{-1} in the spectra of LPD $SiO_{2-x}F_x$ is due to Si-F. As shown in Fig. 3 and Fig. 4, the comparison between TD-LPD and C-LPD FSG in fluorine concentration, dielectric constant, and stress are summarized. Fluorine concentration in TD-LPD film can achieve a value as high as 8.62 atom %, which is obviously higher than 1.8 ~ 6.2 atom % in C-LPD film. This result also indicates that the TD-LPD method is rather effective for increasing the fluorine concentration. The dielectric constant and stress for C-LPD films are within 3.52 ~ 4.25 and within 83 ~ 104 MPa, respectively. However due to high fluorine concentration, TD-LPD film demonstrates low-k (3.46) and low-stress (43 MPa) characteristics[11~12]. Obviously, TD-LPD is superior to C-LPD in preparing low-k and low-stress FSG.

3.2. ELECTRICAL PROPERTIES :

As shown in Fig. 5, the J-E characteristics for the TD-LPD FSG films deposited at 15 & 25℃ are as low as 10^{-9}~10^{-8} A/cm^2. However, for the film deposited at 35℃, the current density is over one order of magnitude higher than those deposited at 15 & 25℃. This is because the film deposited at 35℃ is porous and contains many defects, forming electrically active traps.

Figure 6 shows the distributions of current density at 2 MV/cm for as-deposited (solid symbols) and annealed films. All the distributions for the as-deposited films are rather narrow in current density, indicating that the as-deposited films are uniform in electrical property. After annealing at 400℃ for 30 min in N_2, the median current density (J_{50}) for the film deposited at 15℃ increases slightly from 6.9×10^{-9} to 9.0×10^{-9} A/cm^2; J_{50} for the film deposited at 25℃ increases by a factor of 5, from 4.6×10^{-9} to 2.3×10^{-8} A/cm^2; for the film deposited at 35℃, J_{50} increases by a factor of 5.6, changing from 3.6×10^{-7} to 2×10^{-6} A/cm^2. Obviously, the annealing can degrade the insulating ability. In particular, the degradation is rather pronounced for the films deposited at 35℃. Since more electrically active traps in the bulk can induce a substantially higher leakage current[13], the increased J_{50} can be attributed to the increased trap density. In fact, the Si-O network is not easily decomposed in 400℃ annealing. In contrast, the weak terminating bonds can be easily removed in annealing with defects generated[14]. According to Fig. 5 & 6, the electrical property and the thermal stability are the best for the films deposited below 25℃.

4. LPD FSG AS GATE INSULATOR

4.1. LPD FSG AS GATE INSULATOR FOR LTP POLYSILICON TFT'S

Figure 7 shows a cross-sectional view of the LTP poly-Si TFT. An under-layer of SiO_2 (5000 Å thick) is thermally grown on a (100) silicon substrate. The polysilicon layer (1000 Å thick) is prepared by the SPC[15~16] method. After the polysilicon layer is patterned into islands, as gate insulator, 1000 Å-thick LPD oxide is deposited at 25°C with LPD method mentioned above[17]. Then gate polysilicon (3500 Å thick) was deposited by LPCVD at 620°C and patterned. P^+ (5×10^{15} cm^{-2}, 40 KeV) self-aligned implanted source and drain regions are formed by thermal annealing for 24 hrs at 600°C. After the interlayer of insulator is formed, the contact holes are opened, and an aluminum layer (5000 Å thick) is evaporated and patterned. Finally, hydrogenation is performed in a plasma reactor at 300°C for 60 min. Figure 8 shows the typical transfer characteristics (I_D-V_G) for W/L = 200 μm/10 μm poly-Si TFT's under constant drain voltage of 5 V and 10 V. For these LTP poly-Si TFT's, the excellent characteristic parameters like ON/OFF current ratio of 4.95×10^6 at V_D = 5 V, field effect mobility of 25.5 cm^2/V·sec at V_D = 0.1 V, threshold voltage of 6.9 V and subthreshold swing of 1.28 V/decade are obtained.

4.2. LPD FSG AS GATE INSULATOR OF MOSFET'S

N-channel MOSFETs with aluminum gates are fabricated on 1-5 Ω-cm (100) p-type silicon substrates. A typical cross-sectional view of the MOSFET device is shown in the inset of Fig. 9. The channel length (L) and the channel width (Z) is 20 μm and 942 μm, respectively. The devices are fabricated with conventional four-mask processes without channel implantation. 1000 Å-thick LPD FSG formed at 15°C is first used as gate insulator. Because the fluorine will disappear at a temperature over 700°C[17], the processing temperature has been carefully controlled to avoid affecting the LPD oxide. So in the MOSFET processes, thermal diffusion of phosphorus for the source and drain regions is performed before LPD. In addition, we adopt an aluminum gate to replace the polycrystalline silicon gate, because aluminum evaporation has hardly any thermal effect on LPD oxide. Post-metal annealing at 400°C is the only high temperature process used after LPD oxide. Through the evaluation on electrical

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characteristics, the device parameters including threshold voltage (V_T), subthreshold swing (S) and mobility (m) are all analyzed.

Figure 10 shows the typical I_D-V_D characteristics of our MOSFET with V_G varied in the range from 2 V to 4 V in 0.5 V steps. The triode characteristics and current saturation phenomena well reveals a typical drain characteristics for a long-channel MOSFET. With accurate plotting of transconductance (g_m) versus V_G, the 2.1 V of V_T is obtained. The value of V_T is lower than 4 V for the device with different LTP oxide[18] indicates that a few oxide charges are contained in the LPD oxide. As shown in Fig. 9, the typical I_D-V_G characteristics at $V_D = 0.05$ V and 5V, indicates the drain current varies exponentially with V_G in the subthreshold region. The peak transconductance at $V_D = 0.05$ V is 3.68×10^{-5} S. Moreover, the subthreshold slope is 134 mV/decade, which reveals superior to 170 mV/decade of others[18]. The peak μ_{eff} is 525 $cm^2/V \cdot sec$, while the peak μ_{FE} is 580 $cm^2/V \cdot sec$. In comparison with other works, our peak μ_{FE} is larger than 413 $cm^2/V \cdot sec$ but is less than 700 $cm^2/V \cdot sec$[18] of another works. The result shows that the interface properties of Si/LPD FSG are superior to those of Si/PECVD SiO_2. In total the MOSFET with LPD oxide exhibits comparable performance to other low-temperature processed MOSFET.

5. NOVEL APPLICATIONS OF S-LPD FSG

5.1. SIDEWALL CAPPING FOR DEGRADATION-FREE DAMASCENE TRENCHES

As device geometry is scaled down to deep submicron region, a novel intermetal dielectric (IMD) with a low dielectric constant (*k*) is required to reduce the parasitic capacitance. MSQ, a spin-on organic dielectric, is very promising as a novel IMD, due to its low *k* value (2.8~1.9) and superior thermal stability (>500℃)[19~22]. Therefore, damascene interconnection with MSQ dielectrics and copper (Cu) wires, which has a low resistivity, is very promising to solve the RC delay issue. In damascene process, the MSQ film must be first patterned into trenches. However, MSQ film can be easily degraded after resist ashing step[21~23].

We have proposed sidewall capping technology for degradation-free damascene trenches. Four key process steps, shown in Fig.11, are used to illustrate the preparation of degradation-free MSQ trenches. They are: (a) trench patterning, (b) sidewall cleaning, (c) sidewall capping and (d) resist stripping. A layer of 0.8 μm-thick MSQ was first coated on a 0.6 μm-thick wet oxide. Next, a layer of 0.04 μm-thick SiN was deposited on the MSQ by plasma-enhanced chemical vapor deposition (PECVD). The MSQ trenches with 0.6 μm linewidth/space were then patterned by using I-line lithography and dry etching (Fig.11(a)). After dry etching, the thin residual polymers left on the sidewalls and the bottoms of MSQ trenches were removed via O_2-plasma cleaning,. However, the surface layer on the sidewall of MSQ would also have been slightly oxidized by the treatment, and it should be completely cleared off by wet cleaning in HF-based etching solution (Fig.11(b)). Then a capping layer was selectively deposited on the MSQ sidewalls and the bottoms against the resist by using selective LPD method (Fig.11(c)). This selective deposition is based on the mechanism that the LPD film can be only deposited on the surface containing Si-OH bonds[24]. After sidewall capping, the resist on MSQ was stripped by using conventional ozone ashing (~1atm, 300℃, 65 sec), and cleaned in H_2SO_4/H_2O_2 solution, and the degradation-free MSQ trenches was finished (Fig.11 (d)). Figures 12(a)~(d) show the cross-sectional SEM images of degradation-free MSQ trenches corresponding to the four key process steps. It reveals that a thin LPD FSG film has been capped on the sidewalls. Most importantly, S-LPD FSG never caps the resist, therefore there is no problem in stripping resist. MSQ trenches with LPD FSG films on the sidewalls and nitride films on the tops were never exposed and degraded in an oxidizing ambient.

5.2. DAMAGE-FREE CONTACT HOLE FORMATION:

Reactive ion etching (RIE) is widely used to etch silicon oxide to form contact holes because of its anisotropic etching ability. However, RIE process will make surface be damaged and contaminated, resulting in the generation of interface trap at SiO2/Si interface and in oxide[25~26]. In addition, the selectivity issue of RIE will become more critical in ultra-shallow junction, because the overetch is less allowed. We have successfully employed a novel selective LPD method to prepare contact holes for the n^+/p diodes and the Schottky diodes.

As shown in the left side of Fig.13, for the S-LPD samples, the photoresist on the site of contact hole region are first patterned, then the LPD oxide is selectively deposited on the region without photoresist. After oxide deposition and removing photoresist, the contact holes are automatically formed. For the RIE samples, as shown in the right side of Fig.13, LPD oxide is globally deposited all over the wafers, and the contact holes are formed by using RIE technique

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through lithography photoresist patterns. To buffer the damage generation due to RIE, a partial RIE method is adopted. This means that the 85% oxide is etched by RIE, and then the rest 15% oxide is etched by wet-etching in BHF solution. After metallization, some n^+/p junction diodes are sintered at 400℃ in N_2 for 30min. For Schottky junction diodes, the N-type (100) wafers with 1~5 Ω-cm resistivity are adopted. Their fabrication procedures are similar to those of n^+/p junction diodes except no ion-implantation process. For both n^+/p and Schottky junction diodes with contact holes prepared by S-LPD or RIE method, the I-V characteristics are investigated and compared.

Figure 14(a) shows the comparison of typical I-V characteristics before/after sintering between n^+/p diodes with contact holes fabricated by S-LPD and RIE. Before sintering, for S-LPD sample the reverse current at 5V reverse bias one order smaller than that for RIE sample. The ideality factor η of S-LPD sample in the forward bias -0.4~-0.5V approaches to 1. These results implies that very few G-R centers exist in S-LPD sample, but a lot exist in RIE sample. Besides, the S-LPD samples also exhibit larger forward current. This indicates that there is smaller series resistance in the neutral region of S-LPD diodes. It has been reported that on Si surface RIE easily induces defects, which will result in donor-like charge states. These states will play as G-R centers and increase reverse current if they locate near the band-gap center.

To further study performance of the Si near-surface region for ultra-shallow junction, Schottky diodes were first used for this investigation. Figure 14(b) depicts the performance of S-LPD and RIE Schottky diodes before/after sintering. Before sintering (dash curves), RIE sample nearly loses the rectifying characteristics of Schottky diode under reverse bias, while S-LPD sample exhibits satisfactory Schottky characteristics. However, after sintering (solid curves), the S-LPD sample still exhibits about four orders smaller than that of RIE sampe in reverse current. It is believed that the donor-like bonding defects and the polymer residues make the depletion region be thin and cause the potential barrier lowing, and thereby degrade both reverse and forward I-V characteristics. These results indicate that for the RIE Schottky diodes the sintering is essential to release some of the residues and the defects from the Si surface, but unnecessary for the S-LPD sample. Accordingly RIE process indeed becomes more critical, and requires additional post-treatment. S-LPD can avert these problems and is a good candidate as plasma-damage free, energetic-impurity free and polymer-residue free technology.

6. CONCLUSIONS

LPD FSG technology has been investigated, and its novel applications have also been developed. Using the optimized LPD conditions, the FSG film can be innovatively formed with excellent physicochemical and electrical properties. TD-LPD FSG demonstrates high fluorine concentration (8.6 %), low-k (3.46) and low-stress (43 MPa) and low leakage current density (4.6E-9 A/cm^2 at 2 MV/cm) characteristics. In practical, the applications on poly-Si TFT's and MOSFET's devices have also proved LPD FSG is a good candidate as LTP gate dielectrics. Besides, the S-LPD technique has overcome many undesirable problems such as RIE-induced damage on contact-hole and ashing-induced degradation on MSQ. The S-LPD method indeed has the following superiorities in forming contact-holes or degradation-free damascene trenches. From the points of (i) plasma free process, (ii) damage free process, and (iii) residue and contamination free process, the S-LPD will also replace conventional RIE. It is believed that the LPD technologies are able to supply smart dielectrics to various applications in microelectronics/MEMS.

7. ACKNOWLEDGMENTS

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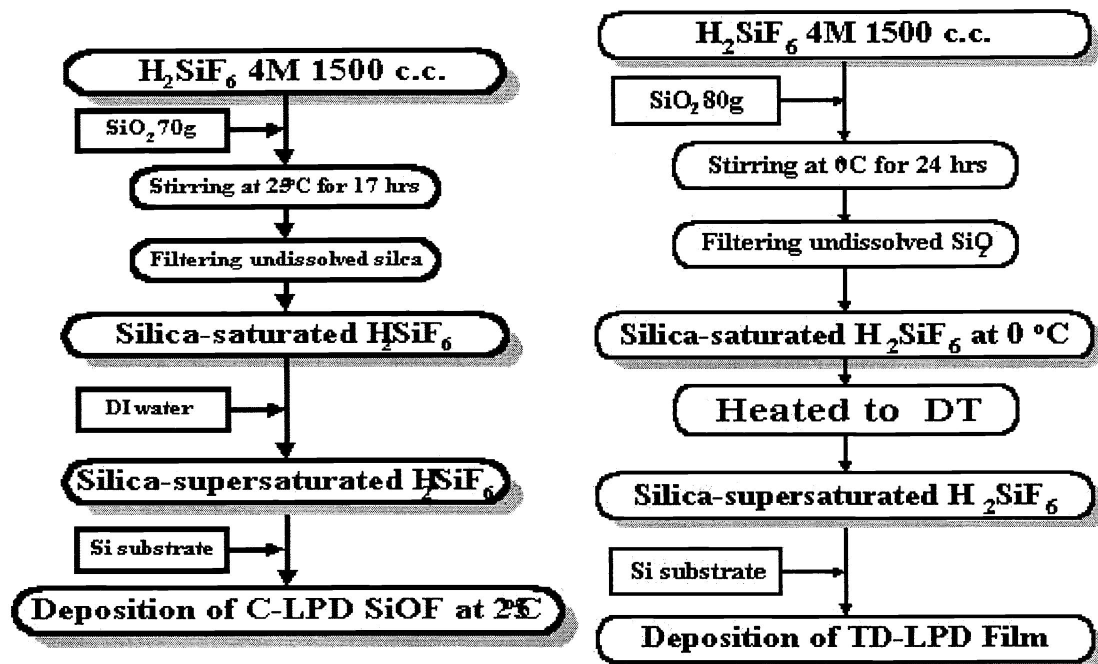

Fig.1 Flow diagram of C-LPD and TD-LPD process

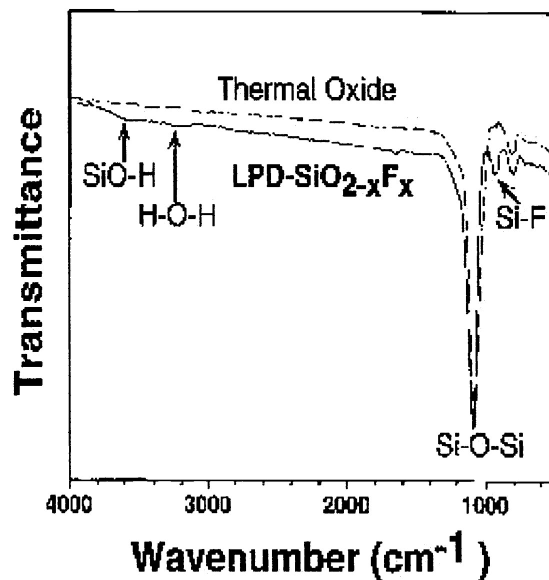

Fig.2 The typical FTIR spectrum of LPD FSG and thermal oxide

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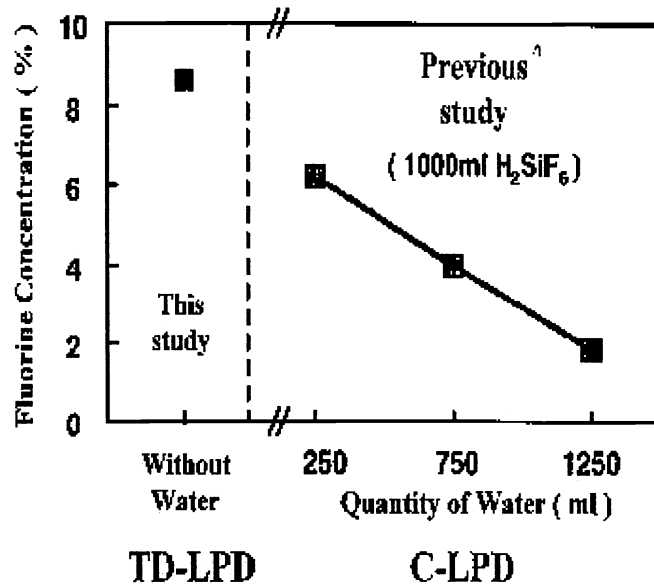

Fig.3 The comparison of fluorine concentration between TD-LPD and C-LPD

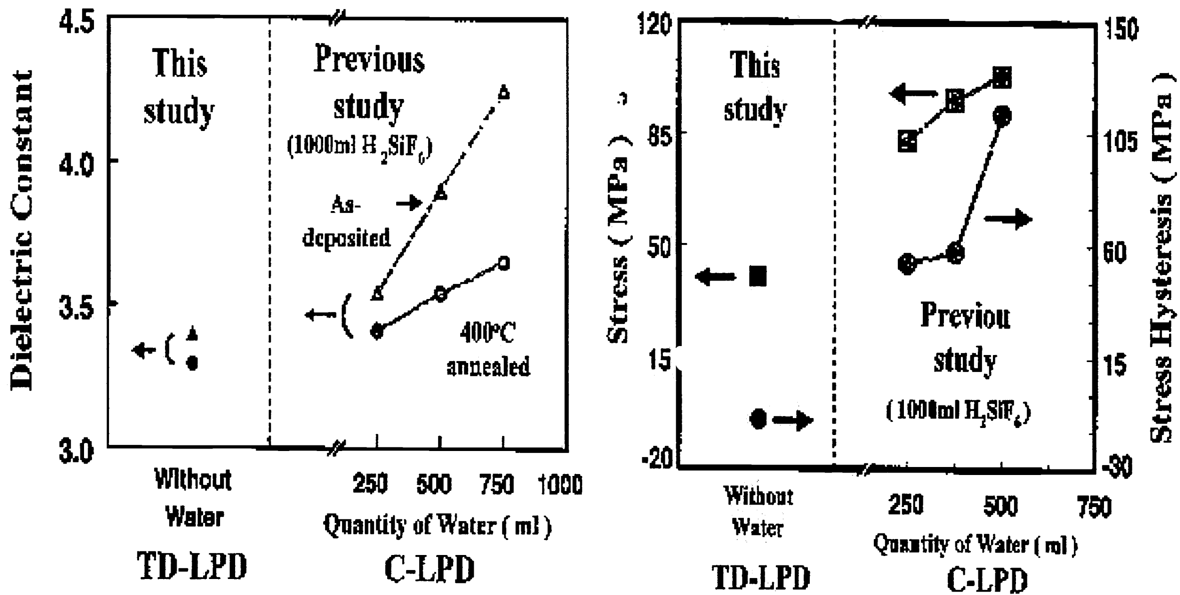

Fig.4 The comparison of dielectric constant and stress between TD-LPD and C-LPD

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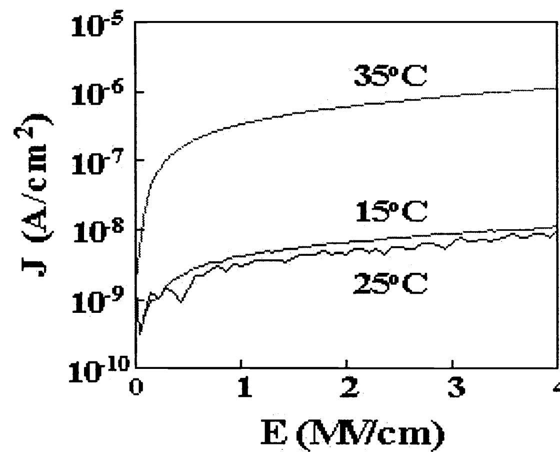

Fig.5 J-E characteristics for films deposited at 15, 25, and 35°C

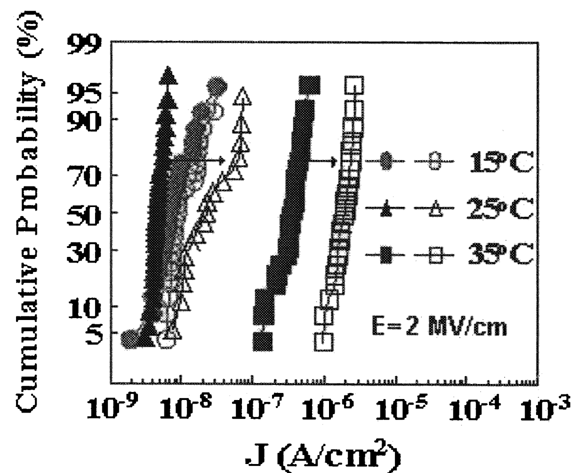

Fig.6 Distributions of current density at 2MV/cm for the as-deposited films (solid symbols) and the annealed films (empty symbols), with deposition temperature as a parameter.

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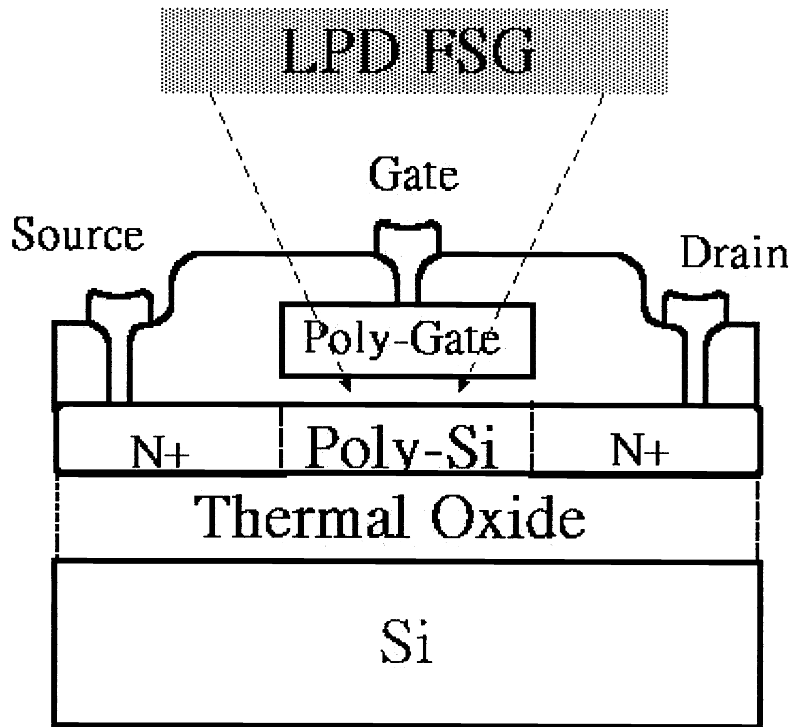

Fig.7 The cross-sectional view of the fabricated poly-Si TFT's

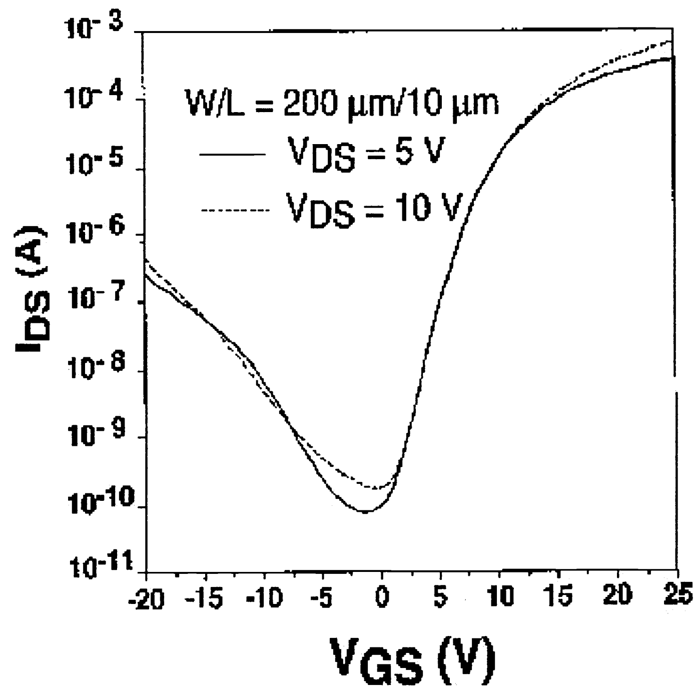

Fig.8 Trensfer characteristics of the n-channel poly-Si TFT with LPD FSG as gate insulator

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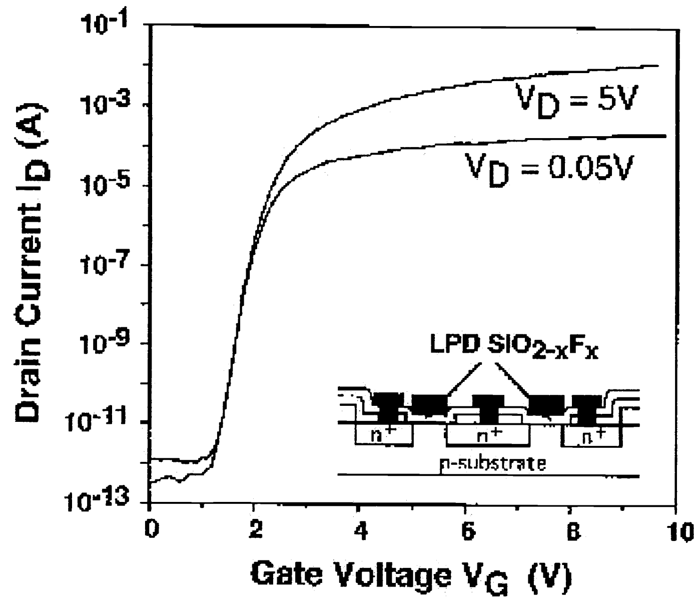

Fig.9 Id-Vg characteristics of MOSFET's using LPD FSG as gate insulator

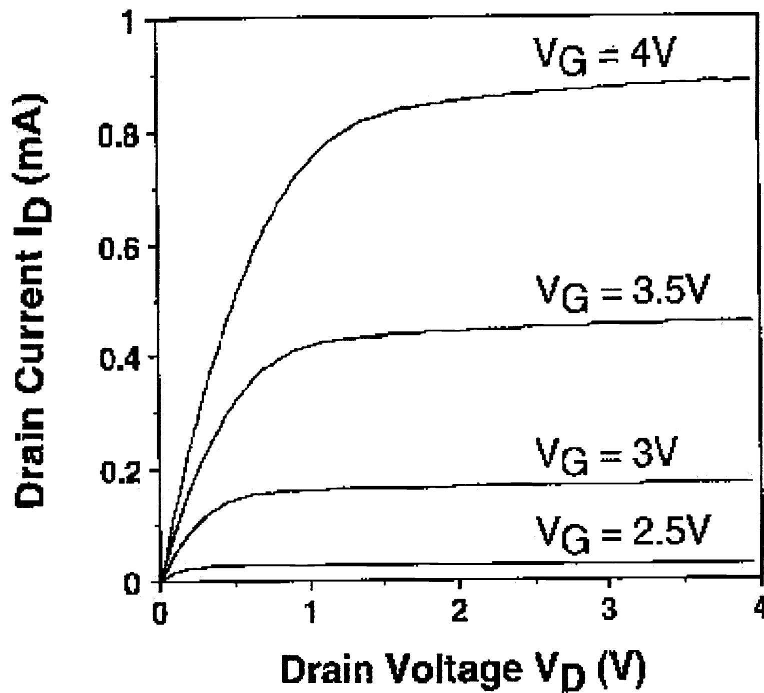

Fig.10 The typical I_D-V_D characteristics of our MOSFET's with LPD FSG as gate insulator

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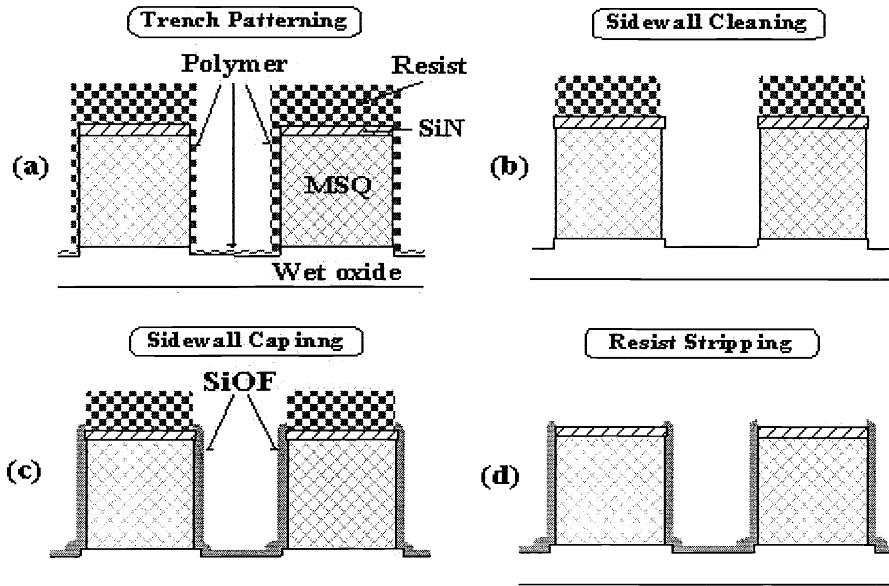

Fig.11 Cross-sectional demonstration for MSQ trenches after (a) trench patterning, (b) sidewall cleaning, (c) sidewall capping, and (d) resist stripping

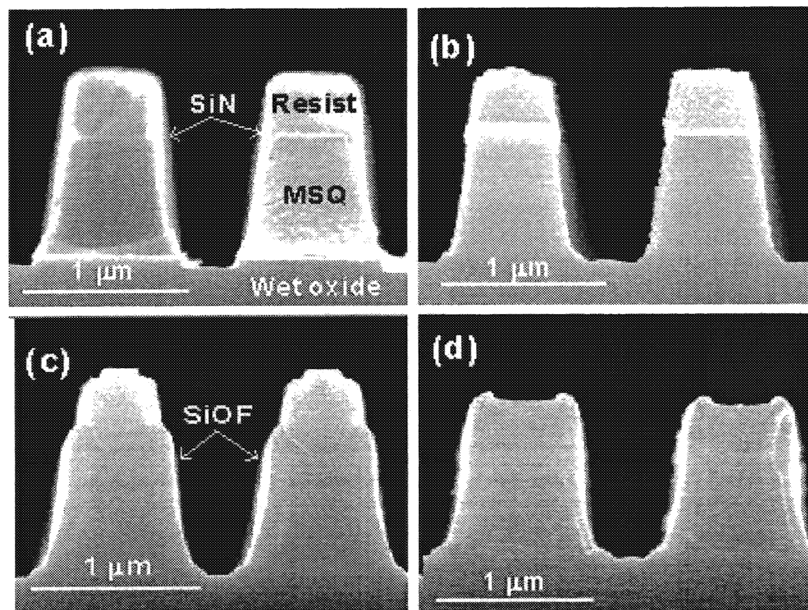

Fig.12 Cross-sectional SEM images for MSQ trenches after (a) trench patterning, (b) sidewall cleaning, (c) sidewall capping, and (d) resist stripping

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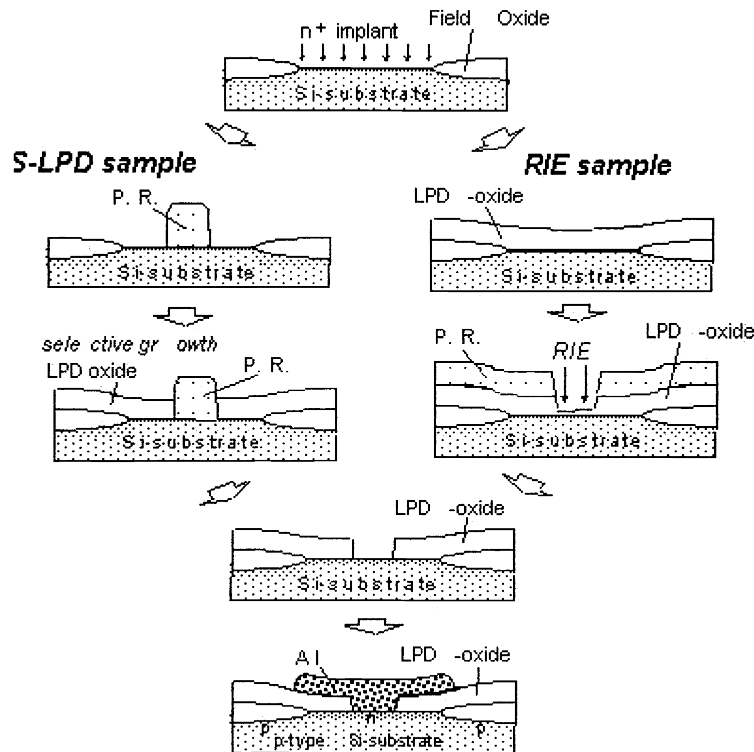

Fig.13 Process-Flow Diagram of n^+/p junction diode with contact hole fabricated by S-LPD (left) or conventional RIE (right).

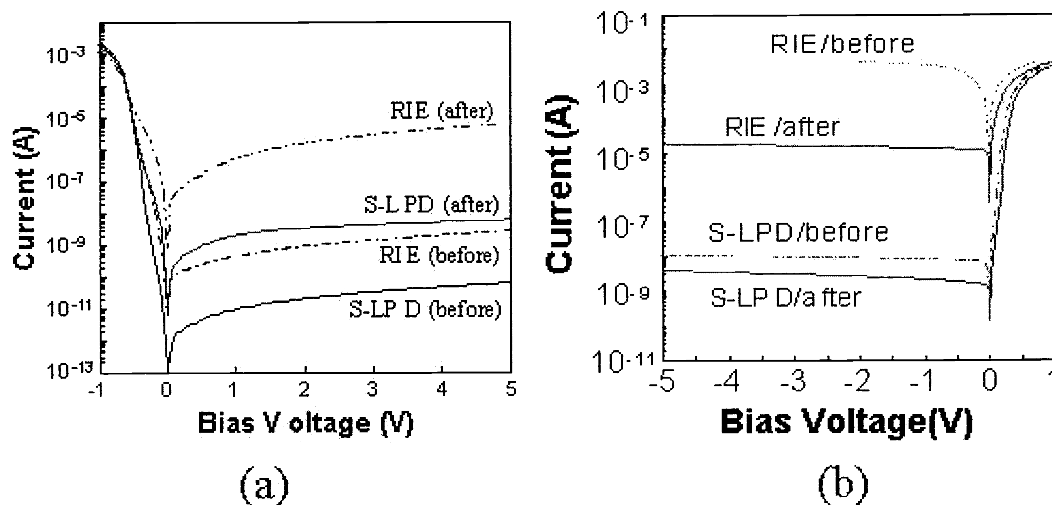

Fig.14 (a) Comparison of I-V characteristics between n^+/p diodes with S-LPD and RIE contact holes ; (b) Comparison of I-V characteristics between Schottky diodes with S-LPD and RIE contact holes (before and after sintering for 30min at 400℃ in N2).

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