Parameters Study to Improve Sidewall Roughness in Advanced Silicon Etch Process

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ABSTRACT

In ICP-RIE process, there have been many investigations on etching rate. However, only few published reports mentioned the sidewall roughness, which is a critical issue for optical devices. Here, experimental investigations about fabrication parameters in the STS Advanced Silicon Etch (ASE) process for sidewall roughness are performed.

In our experiments, the photoresist of AZ1500 is used, and several parameters in the ASE process like over time, ramping time, Ar flow rate, platen power, and etching cycle time have been systematically studied. It is found that sidewall mean roughness can be down to 9.11 nm at etching rate of 2.5 μm/min. Comparing with other published works at similar sidewall roughness (around 10 nm), our experimental data have the highest etching rate. For the same STS ICP-RIE systems, our data have smallest sidewall roughness, comparing to previous literatures.

1. INTRODUCTION

Dry etching technology is essential for the fabrication of microelectro- mechanical systems (MEMS) devices. In order to satisfy the goals of high etching rate and high aspect ratio, high density plasma systems like electron cyclotron resonance (ECR), helical resonator, and inductively coupled plasma (ICP) were developed for the demanding requirements in the MEMS applications. There are three major issues in the drying etching process: etching rate, silicon profile control, and sidewall roughness. The silicon profile control was first demonstrated by Jansen et al. in 1995. The proposed procedure is called the black silicon method, which uses the fact that the silicon is turned black when the vertical wall recipe is found.

For high etching rate development, the Advanced Silicon Etch (ASE) process invented by Lärmer and Schilp in 1996 provides the alternative etching, and passivation steps. By using the STS ASE process, several experiment works were reported to improve silicon etching rate, and silicon etching rate to 7 μm/min has been achieved (Asharf et al., 1998; Bhardwaj et al., 1997; Hynes et al., 1999). Although there have been many investigations on high etching rate and vertical profile, only few published reports are mentioned the sidewall roughness (Chabloz et al., 2000; Takashi and Masayoshi, 2000; Hynes et al., 1999).

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Sidewall roughness is a critical issue for optical devices. For STS Multiplex ICP system, parameter study of ramping control was performed by Hynes et al. in 1999, where a set of process conditions was reported by varying from a starting recipe to a final recipe to yield optimal results at both high and low aspect ratios. The sidewall roughness down to 40 nm and etching rate 1.7 μm/min were achieved by ramping control. In 2000, Chabloz et al. proposed a 3-step high-aspect-ratio silicon etching process to use the Plasma-Therm Shuttle Lock etch tool equipped with an inductively coupled plasma source operating at 2 MHz. The sidewall roughness along the entire etching depth was around 8 nm, and the silicon etch rate was about 1.4 μm/min. For material other than silicon, another investigation concerned the sidewall roughness was performed by Takashi and Masayoshi in 2000, where the sidewall roughness was shown to be 2 nm at the AT-cut quartz plate by using the ICP-RIE developed by Masayoshi et al. at etching rate about 0.5 μm/min.

Here, experimental investigations about fabrication parameters to improve sidewall roughness are performed in a STS ICP-RIE system. Several parameters in the ASE process like over time, ramping time, Ar flow rate, platen power, and etching cycle time will be systematically studied.

2. SYSTEM DESCRIPTION

The ASE process here is carried out in a Surface Technology System (STS) Multiplex inductively coupled plasma system. In the STS Multiplex inductively coupled plasma system, the source plasma is generated by an inductively coupled coil generator (1 kW, 13.56 MHz). The platen electrode is powered by a 13.56 MHz generator, which allows independent control of the bias potential of the wafer relative to the source plasma. The wafer temperature can be maintained at 80℃ below by pressuring helium to the back of the wafer. Wafer is mechanically clamped to the platen electrode. Typical base pressure is 10^{-7} Torr.

The system is equipped with an automatic pressure control valve, which can be operated in one of two modes. In manual mode, opening percentage from 0 to 100% corresponding to an angle between 0.1 and 90 degrees can be selected. In automatic mode, the angle is pressure dependent. The valve is automatically adjusted to maintain the chamber pressure. After performing the dry silicon etching, the etch profile of the trench is evaluated by a Scanning Electron Microscope (SEM), and sidewall roughness of the trench is measured by an Atomic Force Microscope (AFM).

3. ASE PROCESS

The ASE process is based on the technique invented by Lärmer and Schilp, and the sidewall passivation layer is necessary for an anisotropic etching deposited in a separate step from the silicon etch process. Figure 1 shows the mechanisms of ASE process. SF_6 and C_4F_8 are used as the etching and deposition gases. The SF_6 gas supplies fluorine radicals for spontaneous isotropic etching of exposed silicon. The C_4F_8 plasma deposits a $(C_xF_y)_n$ polymeric passivation layer on all substrate surface. The directional ion energy supplied by the capacitively coupled platen electrode during the etch step preferentially removes the passivation layer from the bottom of the trench hence exposing silicon for spontaneous etching. The balance between etching and deposition determines the final process results and this balance

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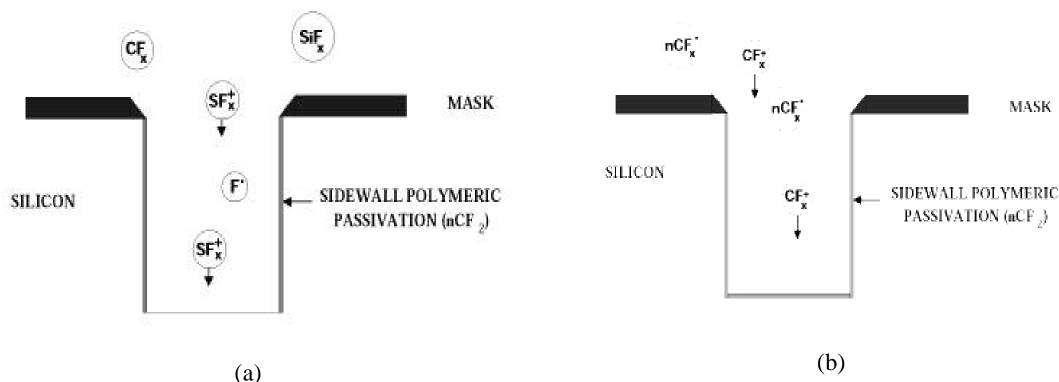
can be controlled through a wide variety of process parameters, which will be studied here.



(a) (b)

Fig. 1 Mechanisms of ASE process. (a)Etching step of ASE process(b) Deposition step of ASE process.

4. PARAMETERS STUDY

In order to investigate the fabrication process to have smooth sidewall roughness and high etching rate, parameters study is performed. After preliminary experimental study, it is found that ramping time, over time, Ar flow rate, platen power, SF_6 flow rate, and etching cycle time have obvious effect to sidewall roughness. The standard recipe used here is supplied by STS. Table 1 lists typical results of the ASE process by standard recipe. From our experimental investigations, these parameters are adjusted one by one to improve sidewall roughness.

Table 1 Typical results of the STS ASE process with standard recipe

Parameter	value	Parameter	Value
Etch rate	1.3μm/min	Selectivity to resist	50 to 100:1
Selectivity to SiO_2	120 to 200:1	Sidewall profile	90° ± 2°
Aspect ratio	up to 30	Feature size	1 to 500 μm
Etch depth capability	500 μ m	Sidewall roughness	100-150 nm

4.1 Ar flow rate and platen power

In RIE process, etching mode contains ion-bombardment and chemical etching. Ar can be added to increase the effect of ion- bombardment. In standard recipe, it does not contain Ar flow rate. Here, Ar is added to observe its effect on

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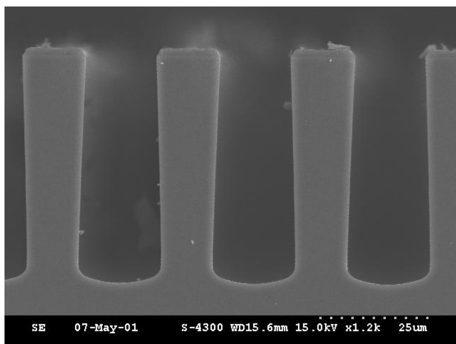
sidewall roughness. Figure 2 shows the difference with and without Ar in ASE process, where the platen power and coil power are 12 w and 1000 w, respectively. In Fig. 2(a), 40 sccm of Ar flow rate is set in the etching step. From Fig. 2(a-2) and Fig. 2(b-2), adding Ar in ASE etching step is shown to improve surface roughness. However, it is found that, with Ar, sidewall inclined angle is worse than the result of recipe without Ar, and 5% of Ar flow rate is suitable for sidewall roughness and profile control. The sidewall inclined angles are 88.85° in Fig. 2(a-1) with Ar and 89.7° in Fig. 2(b-1) without Ar. Anyway this negative taper profile can be improved by increasing the concentration of oxygen, so-called the black silicon method proposed by Jansen et al. in 1995.

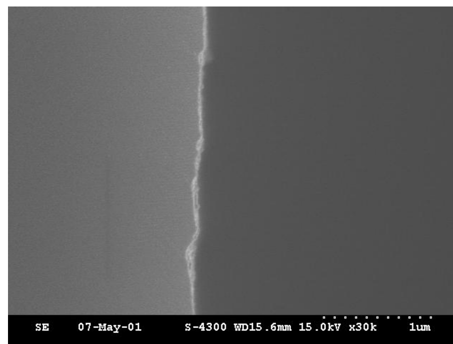
Not only Ar flow rate but also platen power is found to enhance the effect of ion-bombardment. The platen power source is located at the bottom of system. Figure 3 shows the relationship between the platen power and sidewall perpendicularity. Ar flow rate and coil power are set at 40 sccm and 1000 w, respectively, to observe the effect of platen power. Better sidewall perpendicularity is achieved at lower platen power. Because a strong electric field in the sheath provides heavier ion-bombardment to the surface close to the platen power source when a larger platen power is applied. It is also can be found that the selectivity of photoresist to silicon becomes worse, and the phenomenon of undercut is more serious at deeper etching depth. When the platen power is 48 w and coil power is 1000 w, sidewall incline angle is 85°, and it becomes 88.85° at 12 w platen power, as shown in Fig. 3(a) and Fig. 3(d).

4.2 Etching cycle time

Here the influence of the etching cycle time to the sidewall roughness is studied. Figure 4 shows the trench profiles at different etching cycle time. With longer etching cycle time, the etching rate is higher and sidewall roughness is better, but sidewall perpendicularity becomes worse at the same time. At etching cycle time of 16 seconds, the inclined angle is 89.5°, etching rate is 2.8 μm/min, and sidewall roughness is 50 nm, as shown in Fig. 4(c). When the etching cycle time is 20 seconds, the inclined angle is 88°, etching rate is 3.1 μm/min, and sidewall roughness is 40 nm, as shown in Fig. 4(d). From the experimental investigations in section 4.1 and 4.2, additional Ar flow rate, lower platen power, and longer etching cycle time are all found to be able to improve the sidewall roughness, but longer etching cycle time has less effect to sidewall perpendicularity.



(a-1)



(a-2)

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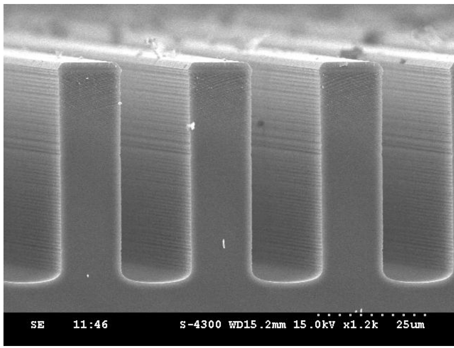
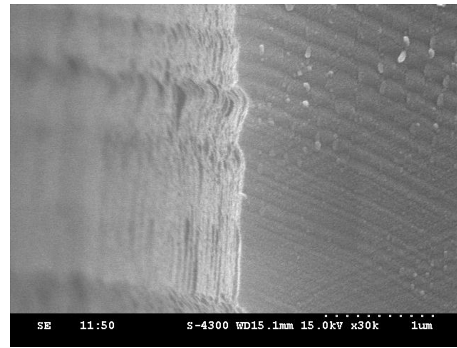
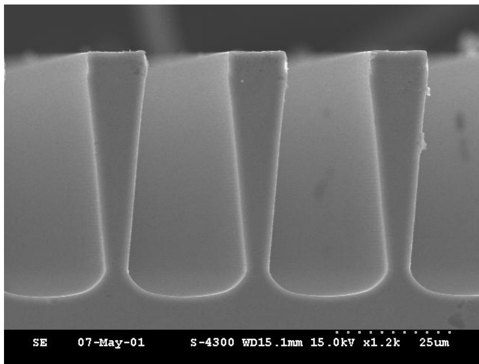


(b-1)

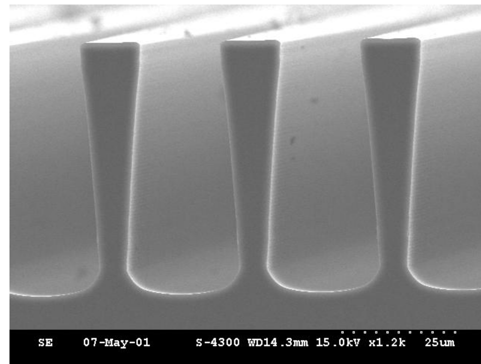


(b-2)

Fig. 2 The effect of Ar in ASE etching step. (a)Trench and sidewall roughness with 40 sccm Ar flow rate (b)Trench and sidewall without Ar in process



(a)



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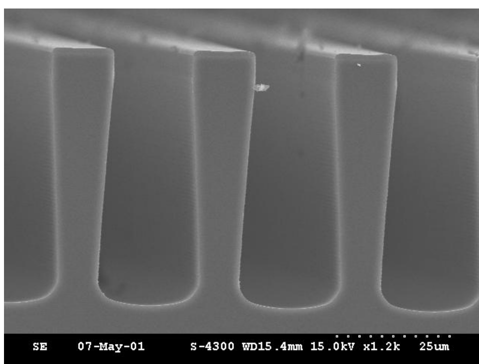
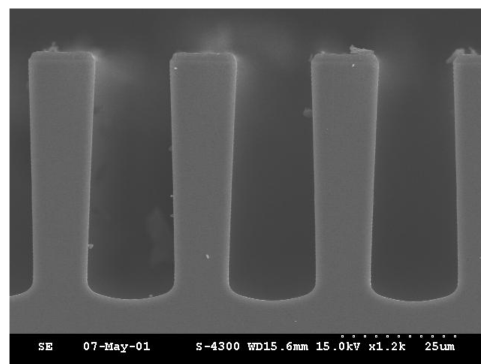


(c)



(d)

Fig. 3 The effect of platen power on sidewall perpendicularity at 1000 w coil power and platen power at (a) 48 w, (b) 36 w, (c) 24 w, (d) 12 w.

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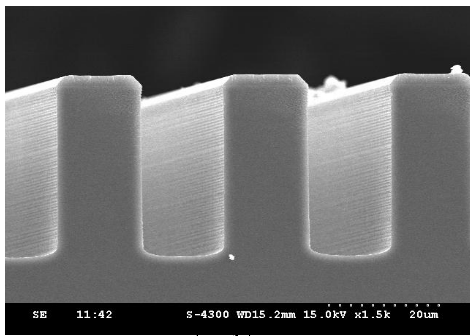
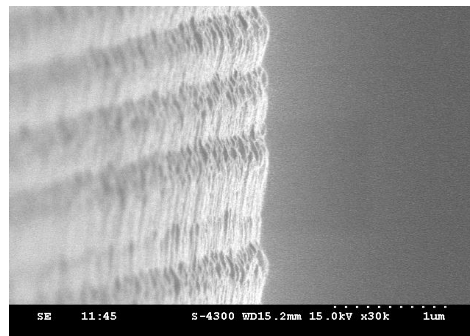
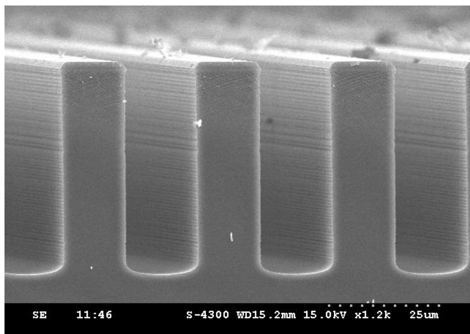


(a-1)



(a-2)



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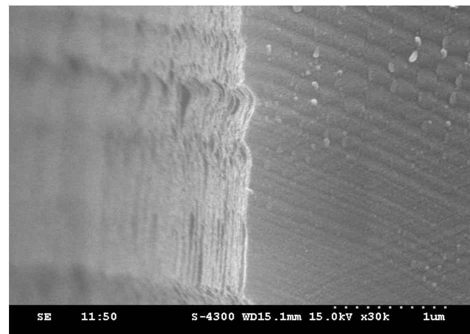
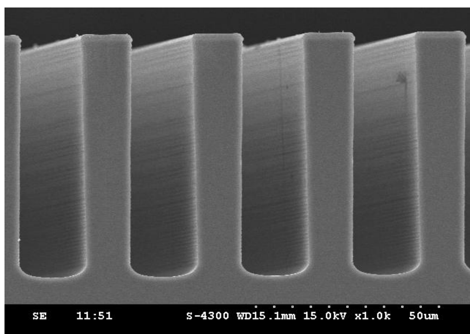


(b-2)



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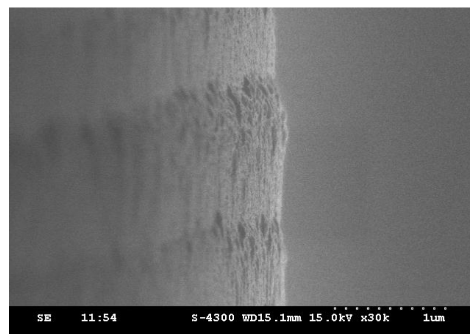

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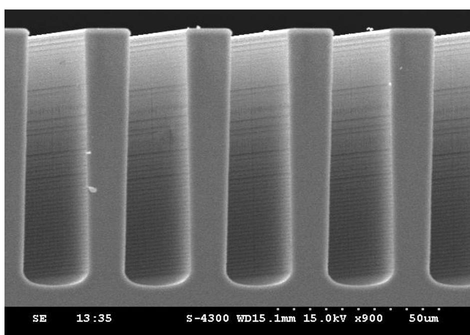
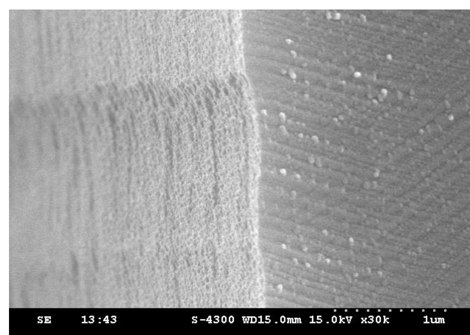


(d-1)



(d-2)

Fig. 4 The relationship between the sidewall roughness at different etching cycle time. (a)Trench profile and sidewall roughness at 8 sec (b)Trench profile and sidewall roughness at 12 sec (c)Trench profile

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4.3 Ramping time and over time

In the STS ICP-RIE system, ramping time means that parameter can automatically vary from a starting recipe to a final recipe. Over time means the overlap of etching and passivation cycle time. Figure 5 shows the SEM of trench sidewalls under different ramping time and over time. The tendency of sidewall roughness is evident. The sidewall roughness becomes smaller at longer over time and shorter ramping time in general. It is found that adjusting the over time and ramping time can effectively improve the surface roughness, as shown in Fig. 5. For example, with the standard recipe where the ramping time and the over time are all zero, the mean roughness is around 130 nm. When the ramping time is 0 second and the over time is 2 seconds per cycle, the mean roughness is calibrated as 19.1 nm, as shown in Fig. 6.

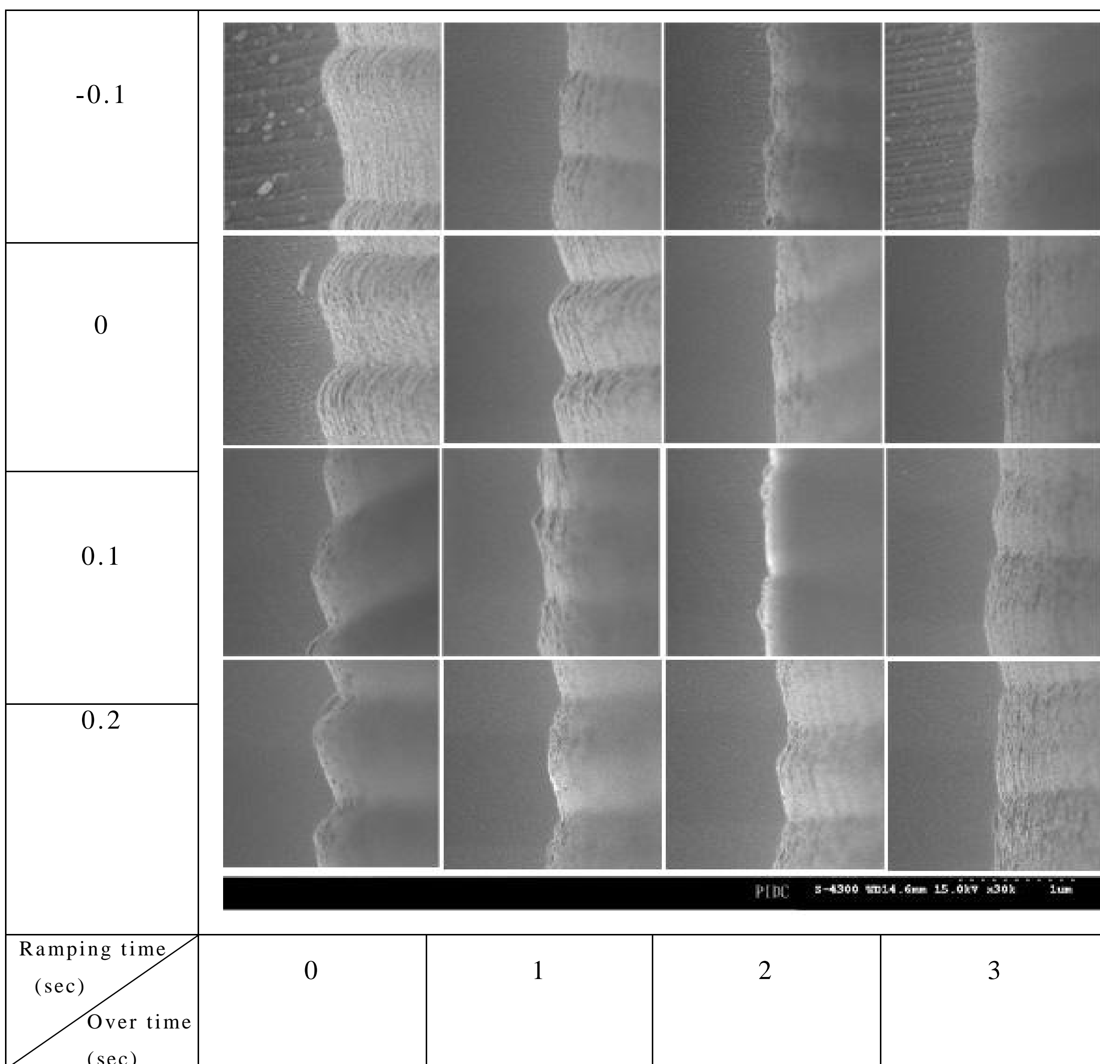

Fig. 5 The sidewall roughness at various ramping time and over time.

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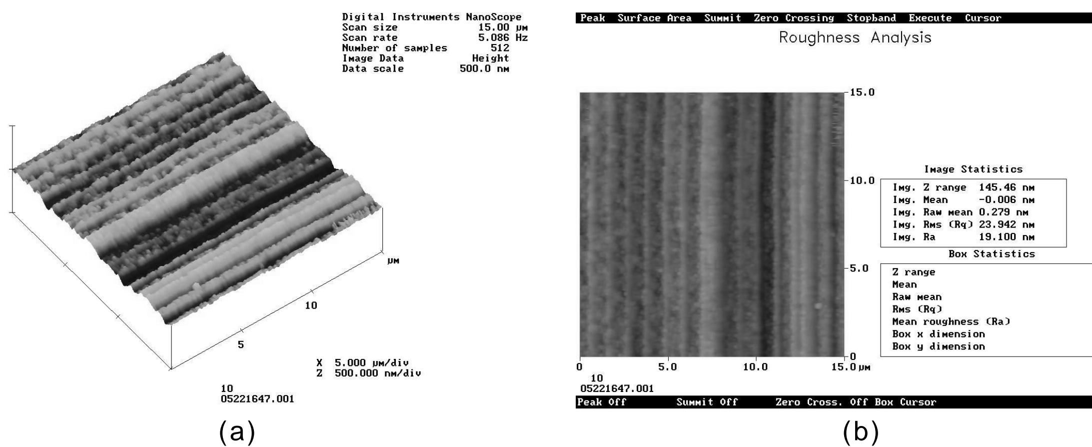
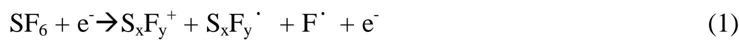


Fig. 6 AFM images of trench sidewall at 2 seconds over time and zero ramping time. (a) 3-D diagram of sidewall surface. (b) Roughness analysis of sidewall surface.

4.4 SF_6 flow rate

In etching cycle, SF_6 gas supplies fluorine radicals ($F^{\cdot}$) for spontaneous isotropic etching of exposed silicon by mechanism illustrated below.



$$SF_6 + e^- \rightarrow S_xF_y^+ + S_xF_y^{\cdot} + F^{\cdot} + e^- \quad (1)$$

$$Si + F^{\cdot} \rightarrow Si\text{-}nF \quad (2)$$

$$Si\text{-}nF \rightarrow Si\text{-}F_{x\,(adsorb)} \quad (3)$$

$$Si\text{-}F_x \rightarrow Si\text{-}F_{x\,(gas)}\,. \quad (4)$$

Etching rate is limited by the ratio of F radical and $SiF_{x(gas)}$, and the mean free path of F radical. When the SF_6 flow rate is getting larger, etching rate is increased due to the higher concentration of F radical. However, too much F radical may dilute the $SiF_{x(gas)}$ concentration and decrease the mean free path of F radical, so that the diffusion control will dominate the etching process to reduce the etching rate. Figure 7 shows the effect of SF_6 flow rate to etching rate. From experimental data, the highest etching rate is achieved at a proper SF_6 flow rate, where the maximum etching rate of Si is 2.5 μm/min at SF_6 of 130 sccm. This phenomenon also appears at the effect of SF_6 flow rate to sidewall roughness. Figure 8 shows sidewall roughness at different SF_6 flow rates, where sidewall roughness at SF_6 flow rates of 130 sccm and 195 sccm are better than the surface roughness at SF_6 flow rates of 65 sccm and 260 sccm.

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4.5 Summary

By the experimental study above, the mean roughness can be effectively improved by adjusting SF_6 flow rate, etching cycle time, Ar flow rate, platen power, ramping time, and over time. When Ar flow rate is between 5%~10% of SF_6 flow rate, platen power is 12 w, and over time is 2 seconds, the sidewall can have a smoother surface, and the better sidewall perpendicularity. At this recipe, the sidewall mean roughness is 9.177 nm with etching rate 2.5μm/min, as shown in Fig. 9.

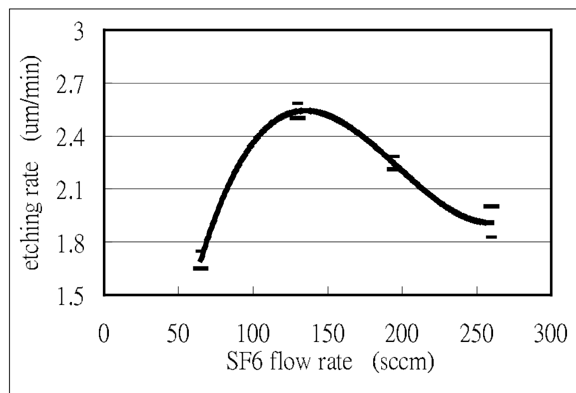
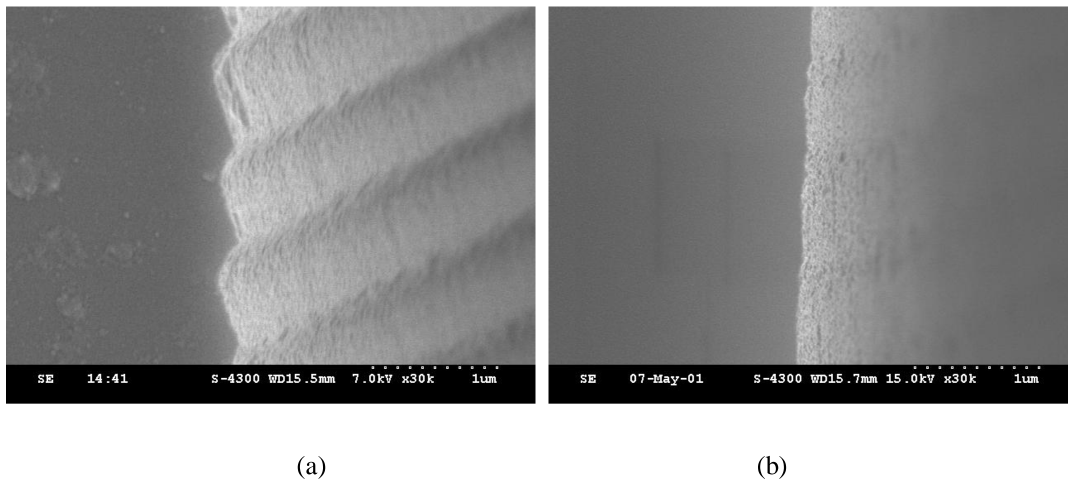


Fig. 7 Silicon etching rate at different SF_6 flow rates with fixed pressure of 25 mTorr.



(a) (b)

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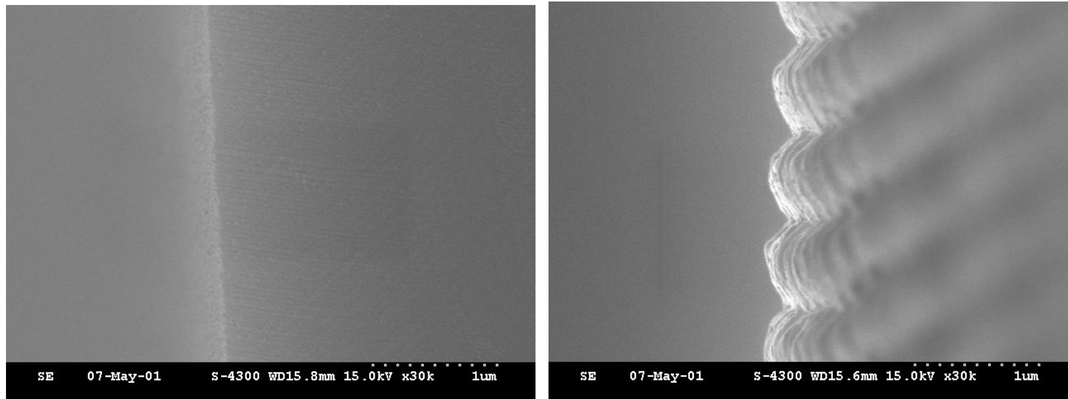
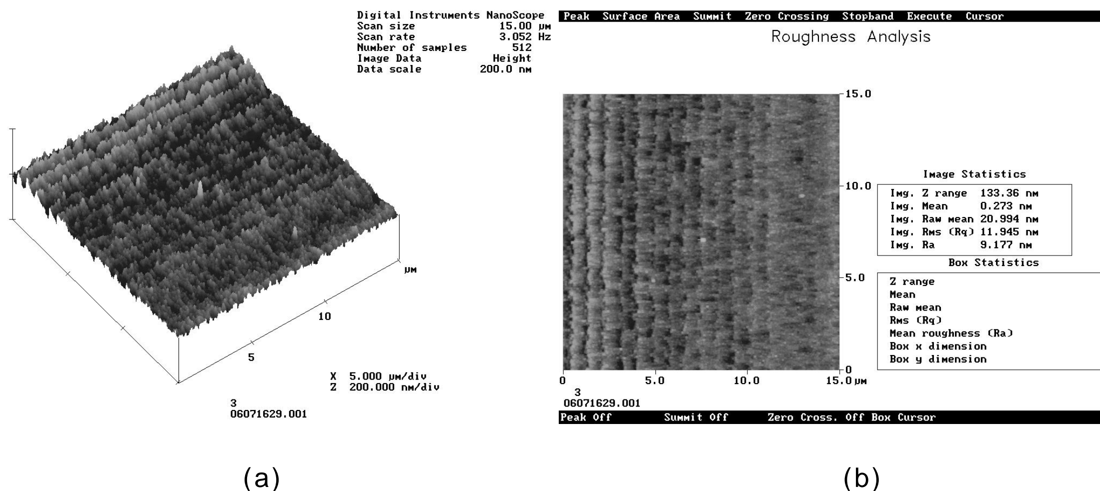


(c) (d)

Fig. 8 Sidewall roughness at SF_6 flow rate of (a) 65 sccm (b) 130 sccm (c) 195 sccm (d) 260 sccm



(a) (b)

Fig. 9 The AFM image of trench sidewall surface. The sample used here was obtained at the proper conditions of Ar flow rate is 20 sccm and over time is 2 sec. (a) 3-D diagram of sidewall surface (b) roughness analysis of sidewall surface.

5. CONCLUSION

A series of experiments are performed to improve the sidewall roughness by adjusting various parameters in an STS ICP system here. The effects on parameters like gas flow rate, power, process cycle time are discussed. The sidewall mean roughness is demonstrated to be lower than 10 nm with etching rate about 2.5 µm/min. Comparing with other published works at similar sidewall roughness (around 10 nm), our experimental data have the highest etching rate. For the same STS ICP-RIE system, our experimental data have smallest sidewall roughness, comparing to previous literatures.

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REFERENCE

1. H. Asharf, J.K. Bhardwaj, S. Hopkins, A.M. Hynes, I. Johnston, S. Mcauley, G. Nicholls, L. Atabo, M.E. Ryan, “Advances in deep anisotropic silicon etch process for MEMS,” *Surfece Technology Systems Limited*,1998
2. A. Takashi, E. Masayoshi, “One-chip multichannel quartz crystal microbalance (QCM) fabricated by Deep RIE,” *Sensors and Actuators* 82, 2000
3. J. Bhardwaj, H. Ashraf, A. McQuarrie, “Dry silicon etching for MEMS,” *Surface Technology Systems Limited* 1997
4. M. Chabloz, Y. Sakai, T. Matsuura, K. Tsutsumi, ”Improvement of sidewall roughness in deep silicon etching,” *Microsystem Technologies*, 2000
5. A.M. Hynes, H. Ashraf, J.K. Bhardwaj, J. Hopkins, I. Johnston, J.N. Shepherd, “Recent advances in silicon etching for MEMS using the ASE process,” *Sensors and Actuators*, 1999
6. Henri Jansen, Meint de Boer, Rob Legtengerg and Miko Elwenspoek, “The black silicon method: a universal method for determining the parameter setting of a fluorine-based reactive ion etcher in deep silicon trench etching with profile control,” *J. Micromech. Microeng*. 5, 1995
7. W. H. Juan, S. W. Pang, “High-aspect-ratio Si etching for microsensor fabrication,” *J. Vac. Sci. Technology* A13, 1995
8. F. Larmer, A. Schilp, “Method of Anisotropically Etching Silicon,” *German Patent DE4241045*, 1996
9. K. Richter, M. Orfert, S. Howitz, S. Thierbach, “Deep plasma silicon etch for microfluidic applications,” *J. Surface and Coating Technology* 1999

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