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Fabrication of MOSFETs Using Low-Temperature Liquid-Phase Deposited Oxide

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Low-temperature, high quality liquid-phase deposition (LPD) oxide was developed. The MOSFETs with such a new LPD oxide as gate insulators were investigated. The electrical characteristics, including threshold voltage of 2.1 Volts, peak effective mobility (μ_{FE}) of 580 $cm^2/V\cdot s$, and subthreshold swing of 134 mV/decade, show the devices exhibit comparable performance to other low-temperature processed MOSFETs. This demonstrates that LPD oxide can be an suitable candidate for future gate insulators in low-temperature processed MOSFETs.

I. INTRODUCTION

Current trends in scaled MOSFET fabrication have stimulated interested in low-temperature silicon processing [1]-[5], because high-temperature processing may generate defects due to larger thermal stress. To date, a few MOSFET studies have looked at deposition of gate oxide at low temperatures [2]-[5], but they all needed expensive apparatus and complex processing to get high quality oxide film. Recently, a novel room-temperature liquid phase deposition (LPD) technique using inexpensive apparatus was developed for silicon oxide [6], [7]. The newest deposition mechanism of LPD oxide was proposed by authors [8] and briefly described as follows:

$$[SiF_6 \times SiF_4]^{2-} + 4H_2O + SiF_4 \rightarrow 2SiF_6^{2-} + Si(OH)_4 + 2HF + 2H^+$$

$$Si(OH)_4 + Si(OH)_4 \rightarrow 2SiO_2 + 4H_2O$$

According to this new mechanism, the key factors which will influence the reaction of LPD oxide were clarified. The high quality LPD oxide film may then be gotten by controlling these parameters in detail. Thus, we were interested in applying this low-temperature high quality LPD oxide to MOSFET gate insulators. This paper present the electrical characteristics of MOSFETs made with such a new LPD gate oxide, and compares them with those of other types of low-temperature processed MOSFETs.

II. EXPERIMENTAL

In the conventional deposition apparatus of LPD oxide, the polysilicic may form a spatial network in the solution and then precipitate on the surface. This phenomenon will make the LPD oxide more roughness and less integrity. Thus, the new deposition apparatus, which can circulate and filter out particles to deposit high quality LPD oxide, was developed in this study, Figure 1 shows the schematic figure of this new apparatus.

N-channel MOSFETs with aluminum gates were fabricated on 1-5 Ω-cm, (100), p-type silicon substrates. A typical cross-sectional view of the fabricated device is shown in the inset of Fig. 2. The fabrication used conventional four-mask processes without channel implantation. The LPD oxide was first used as gate insulator. Specifics concerning the deposition process of LPD oxide were the same as those in our previous works [6][7], except the different deposition apparatus. Because the structure of LPD oxide

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will change after treating at a temperature over 700°C [8], the processing temperature had to be carefully controlled to avoid affecting the LPD oxide. So in our MOSFET processes, thermal diffusion of phosphorus for the source and drain regions was adopted and performed before gate oxide deposition. In addition, we adopted an aluminum gate to replace the polycrystalline silicon gate, because aluminum evaporation has hardly any thermal effect on LPD oxide. Post-metal annealing at 400° C was the only high temperature process used after LPD oxide deposition.

III. RESULTS AND DISCUSSION

In order to investigate the advantage of new deposition apparatus, the LPD oxide deposited with new apparatus was characterized. Fig. 3 shows the surface inspection of LPD oxide with atomic force microscope (AFM), we found that the LPD oxide had much smoother surface and no particles precipitated on the surface. And from the distribution of breakdown field, as shown in Fig. 4, we found that LPD oxide exhibited no low field breakdown. From above results, we may conclude that the film deposited uniformly and no weakspots existed in the film.

According to our new reaction equilibrium, we inferred that H_2O added into the silica-saturated hydrofluosilicic acid (SSF) and the reaction temperature will majorly influence the reaction of deposition, i.e., the deposition rate. To investigate the influences of H_2O added quantity and deposition temperature on the deposition rate of LPD oxide, different deposition conditions including H_2O added quantity of 25 ml ~ 150 ml in the SSF solution of 100 ml and deposition temperature of 5°C ~ 35°C was adopted. The results were shown in Fig. 5 and 6, respectively. The figure showed that the deposition rate increased linearly with H_2O added quantity and exponentially increased with temperature. It reveals that the increment of reactant or reaction temperature would level up the reaction rate in the solution. In the same time, from the measurement results of refractive index, p-etch rate and electric field breakdown, we found that the better integrity of LPD oxide was formed at a lower deposition rate. According this, the LPD oxide with 30 nm thickness deposited at extremely low deposition rate was developed. Its I-V characteristics was shown in Fig. 7. From this figure, we may concluded that the LPD oxide deposited with new apparatus and best deposition conditions show comparable characteristics with other oxides. Thus, we were interested in applying this low-temperature LPD oxide to MOSFET gate insulator. In the same time, from the FTIR spectrum, as shown in Fig. 8, the peak of 930 cm^{-1} was found. The peak in this position is Si-F bonds, indicating us that fluorine were incorporated in the LPD oxide film.

Fig. 9 shows the typical I_D-V_D characteristics of our MOSFET with V_G varied in the range from 2 V to 4 V in 0.5 V steps. The I_D-V_D curve exhibiting triode characteristics and current saturation phenomena well, reveals a typical drain characteristics for a long-channel MOSFET. Next, with plotting of transconductance (g_m) versus V_G, the 2.1 V of V_T was obtained. The fact that this value of V_T is lower than the 4 V of in other studies [2] indicates that there are fewer fixed oxide charges contained in the LPD oxide. The typical I_D-V_G characteristics of our MOSFET with V_D = 0.05 V, are also shown in Fig. 10, show the drain current varies exponentially with V_G in the subthreshold region. We also found that the curves in the subthreshold region show virtually no dependence on the drain voltage. The peak transconductance calculated at V_D = 0.05 V is 3.68×10^{-5} S. Above results imply that MOSFETs with LPD oxide gate insulator have electrical characteristics that compare favorably with conventional MOSFET. Moreover, the subthreshold slope calculated from the I_D-V_G curve is 134 mV/decade, which reveals superior to the 170 mV/decade recorded in other device with low-temperature Ar/O_2 sputtered oxide [2].

Since the MOSFET mobility is strongly influenced by the surface states, it is essential to evaluate the mobility when investigating the interface quality. Fig. 11 shows the field-effect mobility (μ_{FE}) vs. the V_G-V_T. The μ_{FE} is given by $\mu_{FE} = g_m \cdot L/Z \cdot C_{ox} \cdot V_D$, where C_{ox} is the gate capacitance per unit area. The mobility curves are highly consistent with those of MOSFETs with thermal gate oxide [9]. The peak μ_{FE} is 580 $cm^2/V \cdot s$. The fact that mobility decreasing with gate voltage can be attributed to the enhanced surface roughness scattering with increased gate voltage [9]. In comparison with other works, our peak μ_{FE} is larger than 413 $cm^2/V \cdot s$ [5] but is less than 700 $cm^2/V \cdot s$ of another work [2]. These results show that the

interface properties of Si/LPD oxide are superior to those of Si/PECVD SiO_2, but inferior to those of Si/O_2-Ar sputter-deposited oxide. We may confirm this result from the D_{it} data, as shown in Table I, where the parameters calculated from MOSFET with LPD oxide were summarized. The results of other MOSFETs with various low-temperature deposited gate oxides were also shown for comparison. It reveals that the D_{it} of our device is lower than that of sputtered oxide device, but higher than that of PECVD oxide device. The least D_{it} for the sputter-oxide device may be attributed to a high-temperature annealing, which was performed at 800°C after oxide deposition. The LPD oxide devices having less D_{it} may be due to fluorine incorporated in the film [10], as shown in the above section. That is, the fluorine may passivate some interfacial dangling bonds, as well as remove some Si-Si and Si-O weak bonds, via its incorporation and Si-F formation. Thus, the MOSFET with LPD oxide has excellent interface properties.

IV. CONCLUSION

We have applied a novel room-temperature LPD oxide to low-temperature processed MOSFET without high-temperature annealing. Its I_D-V_D and I_D-V_G curves exhibit excellent triode-like characteristics and subthreshold characteristics, respectively. All the device parameters were compared well to those of other low-temperature processed MOSFETs. These results reveal the great possibility of applying LPD oxide as a gate insulator in low-temperature processed MOSFET in future.

ACKNOWLEDGMENT

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TABLE I. SUMMARIES OF DEVICE PERFORMANCES FOR MOSFETs UTILIZING VARIOUS GATE OXIDE DEPOSITION METHODS

	LPD gate oxide	O_2-Ar sputter-deposited gate oxide [2]	PECVD gate oxide [5]
Gate electrode	Aluminum	Polysilicon	Aluminum
Deposition temperature	20° C	200° C	350° C
Post-annealing Temperature	400° C	800° C	400° C
Midgap D_{it} ($eV^{-1}cm^{-2}$)	1.8×10^{11}	5.0×10^{10}	2.7×10^{11}
Peak mobility μ_{FE} ($cm^2/V \cdot s$)	580	700	413

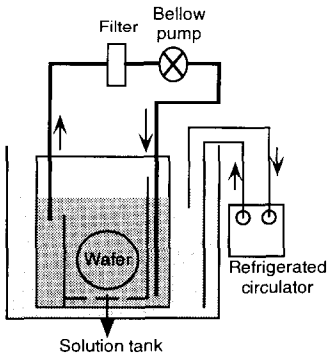

Figure 1. Schematic diagram of the circulation apparatus for LPD oxide.

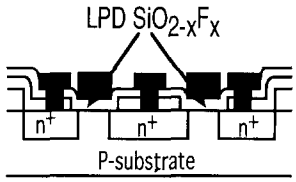

Figure 2. The cross-sectional view of the fabricated MOSFET device.

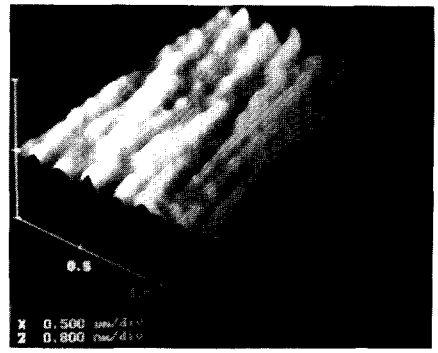

Figure 3. AFM surface inspection of LPD oxide deposited with the circu-lation apparatus.

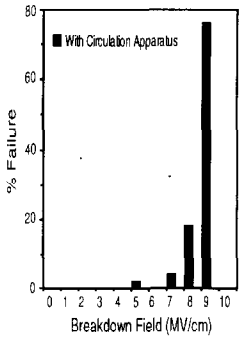

Figure 4. Breakdown field distribution of LPD oxide deposited with the circula-tion apparatus.

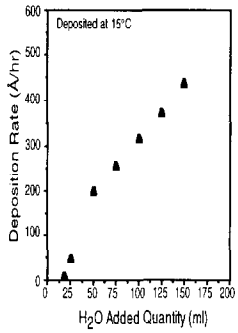

Figure 5. Relationship bet-ween deposition rate of LPD oxide and H_2O added quantity.

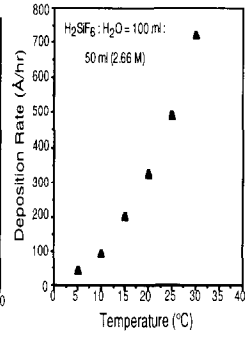

Figure 6. Relationship between deposition rate of LPD oxide and deposition temperature.

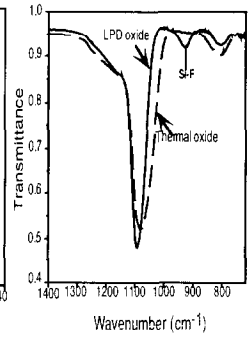

Figure 7. FTIR spectra of LPD oxide and thermal oxide in the region of 700 ~ 1400 cm^{-1}.

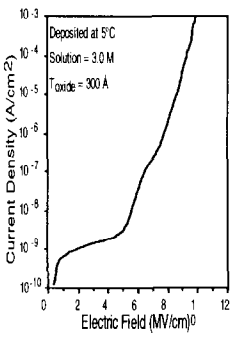

Figure 8. J vs. E characteristics of MOS diode with LPD oxide as gate insulator.

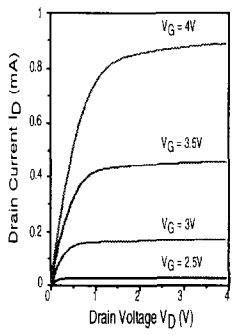

Figure 9. The typical I_D-V_D characteristics of MOSFETs with LPD oxide as gate insulator.

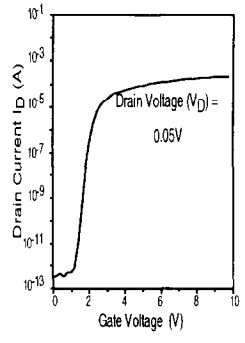

Figure 10. The typical I_D-V_G characteristics of MOSFETs with LPD oxide as gate insulator.

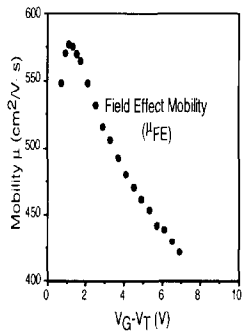

Figure 11. μ_{FE} versus V_G-V_T of MOSFETs with LPD oxide as gate insulator.