Nitridation of the Stacked Poly-Si Gate to Suppress the Boron Penetration in pMOS

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***Abstract*—Nitridation to create nitrogen-rich layers in-between the stacked layers of the poly-Si gate to suppress the boron penetration for pMOS with the gate BF_2^+-implantation is proposed and demonstrated. The MOS capacitors fabricated by using this nitridized stacked poly-Si gate have better thermal stability and much improved electrical characteristics.**

I. Introduction

P^+ poly-Si gates are commonly used in submicron CMOS technology to prevent short channel effect [1]. However, the boron used to dope this p^+ poly-Si gate penetrates easily through the gate oxide into the underlying Si substrate, especially for the BF_2^+-implanted poly-Si gate [2]. Oxynitride can be used to suppress the boron penetration [3]. But NH3-nitridized oxide causes increase of the electron trapping rate and interface state generation under stress [3]. Previously, we had proposed a stacked poly-Si gate structure to effectively suppress the boron penetration [4]–[5]. In this work, it is shown that nitridation of the stacked poly-Si gate to create nitrogen-rich layers in-between the stacked layers further reduced the boron penetration and much improves the electrical characteristics. Moreover, the negative effects of the NH3-nitridized oxides [3] are not found for this structure.

II. Experiment

The p^+ poly-Si gate MOS capacitors were fabricated on (100), 5 ~ 10 Ω-cm, n-type Si wafers with a 80 Å gate oxide. The gate oxide was grown in diluted dry O_2 (O_2/N_2 = 1/6) at 900°C and annealed in N_2 at the same temperature for 15 min. After that, an undoped polysilicon was deposited at 625°C in a low pressure chemical vapor deposition (LPCVD) system in three steps, 1000 Å in each step, and a nitridation in low pressure (120 mTorr) NH_3 at 900°C for 80 min was performed between the second and the third layers of the poly-Si (PPHP). The nitridized silicon layer was soaked in diluted HF before the third poly-Si layer deposition. For comparison, capacitors with the same stacked poly-Si gate but without the nitridation (PPP) were also fabricated [4]. Then, all the samples were implanted with BF_2^+ of a dose 5×10^{15} cm^{-2} at 50 KeV, and annealed at 800°C in O_2 for 30 min first and then at 900°C in N_2 for 10, 20, 30, and 40 min respectively to activate the implanted dose. After the polyoxide was removed, Al was deposited and annealed at 400°C in N_2 for 30 min to make capacitors.

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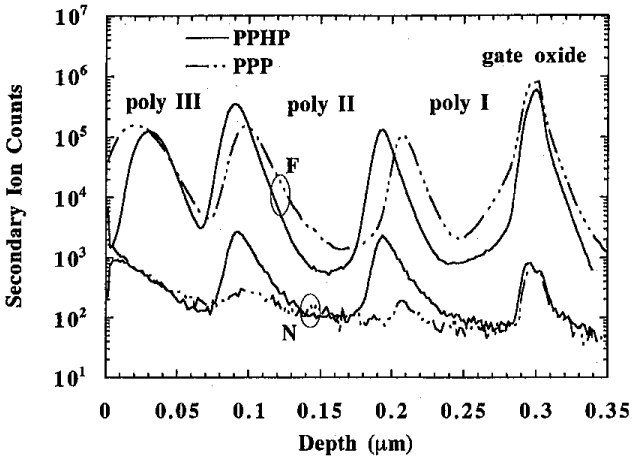

Fig. 1. The nitrogen and fluorine profiles of the 900°C, 40 min annealed PPHP (solid curves) and PPP (dotted curves) samples.

III. Results and Discussions

Fig. 1 shows the SIMS nitrogen and fluorine profiles of the 900°C, 40 min annealed PPHP and PPP samples, respectively. The PPHP curve had much higher nitrogen peaks at the interface of the stacked poly-Si due to NH_3 nitridation as compared to the PPP curve. These nitrogen-rich layers blocked the fluorine diffusion in the poly-Si gate, and thus reduced the amount of fluorine in the gate oxide. This is seen from the figure that the PPHP had a less fluorine peak at the oxide. Consequently, the fluorine enhancement on boron penetration is reduced [5]–[7] for the PPHP sample. Moreover, it is seen that much nitrogen was incorporated into the gate oxide due to oxidation in diluted O_2. But for the PPHP sample, its poly-Si/SiO_2 interface was slightly more nitridized than that of PPP.

Fig. 2 shows the normalized quasistatic C–V curves for PPHP and PPP samples annealed for different times respectively. The shifts of the C–V curves, which were due to the negative fixed charge generated by F–B complexes and a very shallow p type layer in the silicon substrate as a result of the boron penetration [8], of the PPHP samples were much less than those of the PPP samples. Also, the C–V curve distortion did not occur for the PPHP samples even for long

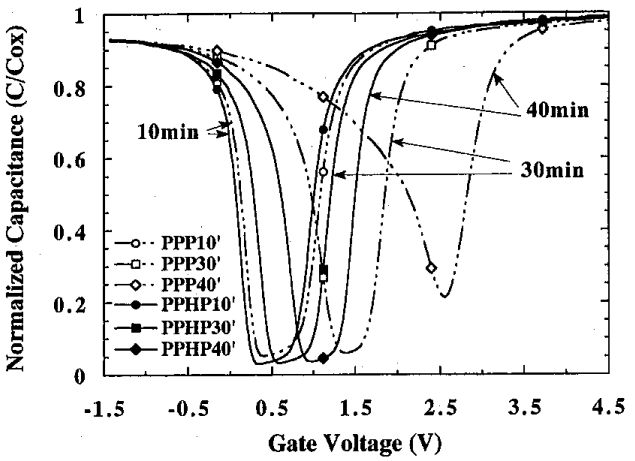

Fig. 2. The normalized quasistatic C–V curves of the PPHP and PPP samples with different post-implant annealing times at 900°C.

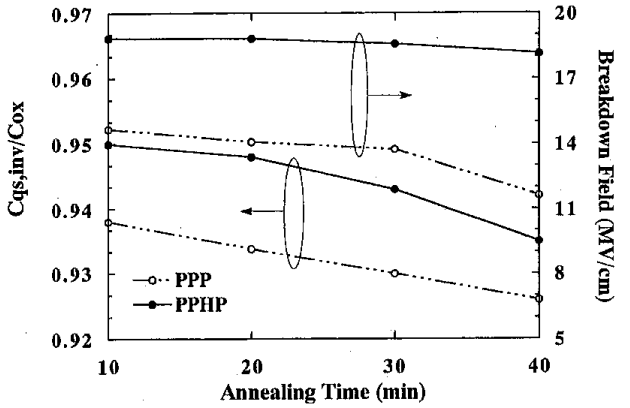

Fig. 3. The normalized quasistatic inversion capacitances ($C_{qs,inv}/C_{ox}$) and breakdown fields (MV/cm) of the PPHP and PPP samples annealed at 900°C for different times.

annealing time, meaning that the gate oxide interface sustained no degradation [4]. Thus, the nitridation of the stacked poly-Si gate further suppresses the boron penetration than does the stacked gate structure only [4].

Fig. 3 compiled the polysilicon depletion effect, as monitored by the normalized inversion capacitance ($C_{qs,inv}/C_{ox}$) as a function of the post-implant annealing time at 900°C. The values of $C_{qs,inv}/C_{ox}$ were larger for PPHP than for PPP. That is, PPHP is better than PPP in considering the polysilicon depletion effect. This implies that the nitrogen-rich layers created by the nitridation of the stacked poly-Si gate blocked only the fluorine diffusion but not the boron diffusion.

The PPHP capacitors also had better electrical characteristics on the gate oxide since a better integrity of the gate oxide was preserved due to less boron penetration and the slightly more nitridation at the poly-Si/SiO_2 interface which relaxed the stress between the poly-Si and the gate oxide [9]. In Fig. 3 where the breakdown fields are also shown, for PPHP, they were much larger than those of PPP and they were nearly unchanged as the annealing time was increased. Fig. 4 shows the gate voltage shifts (ΔV_g) during the constant current (10 mA/cm^2) stress for PPP and PPHP respectively. The time to breakdown of PPHP, even for the sample with 40 min

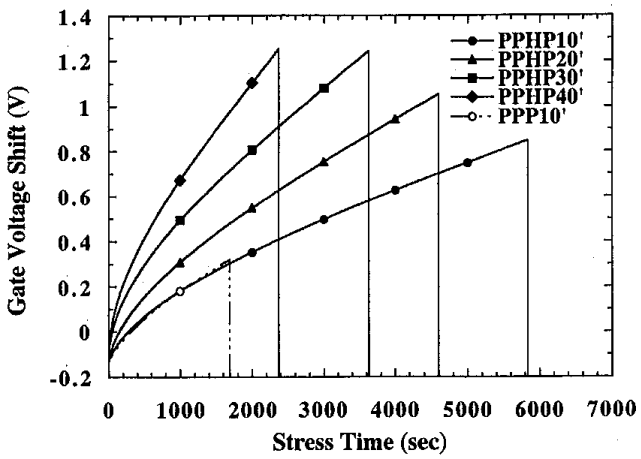

Fig. 4. Comparison of the gate voltage shifts (ΔV_g) under the constant current (10 mA/cm^2) stress for PPHP and PPP samples with different annealing times at 900°C.

annealing, were larger than that of the PPP sample annealed at 900°C for 10 min. Moreover, the electron trapping rates were nearly the same for both the 10 min-annealed PPP and PPHP samples. This is in contrast to the conventional NH_3-nitridized oxides which had higher electron trapping rates [3].

IV. Conclusion

Based on the above results and discussions, we conclude that the nitridation to create nitrogen -rich layers in-between the stacked layers of the stacked poly-Si gate is very effective in suppressing the boron penetration for the $BF2^+$-implanted pMOS.

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