New Experimental Evidences of the Plasma Charging Enhanced Hot Carrier Effect and Its Impact on Surface Channel CMOS Devices

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Abstract- Plasma etching of poly-silicon gate in CMOS devices induces the *plasma edge damage*. This damage will be enhanced in the successive plasma processes. New experimental evidences of this effect will be examined in this study. Results have been verified for both surface channel n- and p-MOSFETs. First, from the measurements of high-density antenna structures, this enhanced edge damage has been characterized by the charge-pumping (CP) profiling technique. Then, a 4-phase edge damage mechanism has been proposed. *For the first time*, it was found that a *two-peak* spatial distribution of the interface state was found near the device drain region. We call it Plasma Charging Enhanced Hot Carrier (PCE-HC) effect. This enhanced damage effect will induce further device degradation, in particular for the scaled devices.

1. Introduction

It is known that two kinds of plasma damage will be introduced during the plasma etching process [1-2]. One is the plasma charging damage (in the gate oxide and channel region), and the other one is the plasma edge damage (near the poly-Si gate region). The former is due to the plasma-induced FN tunneling current flowing through the gate oxide, while the latter is caused by the direct plasma ions bombardment or chemical reaction with the Si-substrate. In previous studies, the HC effect is found independent of plasma charging damage [1,3]. However, our experimental results show that this type of plasma damage will enhance the HC effect, in particular for short channel devices.

In this study, based on the measured results, we propose a new degradation mechanism to describe the aforementioned PCE-HC effect. For both surface channel n- and p-MOSFET's, new results of the plasma enhanced damage will be demonstrated and verified by the CP profiling technique [4-5].

2. Device Fabrication and Measurements

The devices used in this work were fabricated for the surface channel n- and p-MOSFETs. Two dfferent types of antenna structure were used as shown in Fig. 1. Device (1) is the control sample and device (2) has high-density comb-like antenna structure. The oxide thickness and the channel length for the n-MOSFETs (p-MOSFETs) are 38Å and 0.35μm (46Å and 0.70μm), respectively. All of these devices are passivated by the poly-reoxidation process to reduce the plasma edge damage. To test the HC reliability of these devices, $I_{B,max}$ stress was used. Note that the HC effect is dominated by interface states under this stress condition.

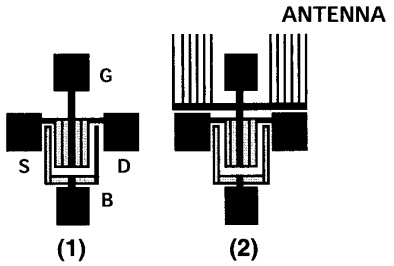

Fig. 1 Two kinds of antenna structures used in this study. Device (1) is the control sample and device (2) has high-density comb-like antenna structure.

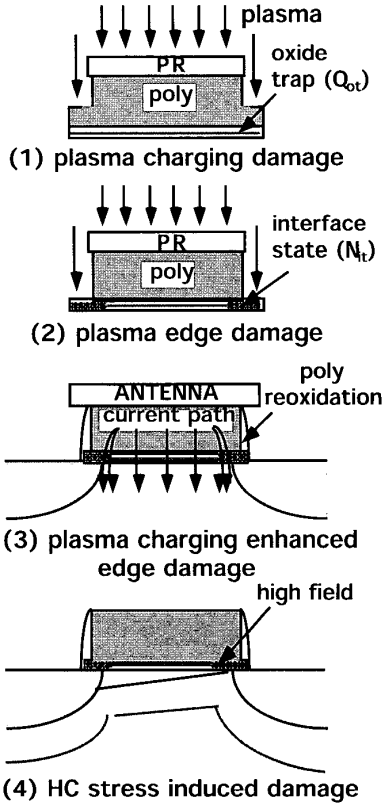

Fig. 2 Three phases inducing the plasma damage: (1) plasma charging damage; (2) plasma edge damage; (3) plasma charging enhanced damage; and (4) HC stress induced damage.

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3. The Mechanism- A 3-phase Plasma Damage Mechanism

From the device fabrication processes given in Fig. 2, a 3-phase plasma damage generation mechanism is proposed. From the beginning, plasma charging degrades oxide quality by FN current (Fig. 2(1)). Then, plasma edge damage is generated by direct ion bombardment (Fig. 2(2)). This edge damage was repaired after the poly-reoxidation process. During the subsequent etching of the antenna structures (e.g., capacitances, interconnected lines), it will induce the plasma charging damage, again. This will enhance edge damage at the poly-Si gate edge, since most of the current path goes through the gate edge due to the weaker oxide barrier (Fig. 2(3)). We name this phenomenon as *plasma charging enhanced edge damage* (PCE-ED). After the manufacturing processes, the HC experiment is performd to test the plasma induced reliability. The maximum electric field will enhance the plasma damage near the drain region and induce much more serious HC effect (Fig. 2(4)).

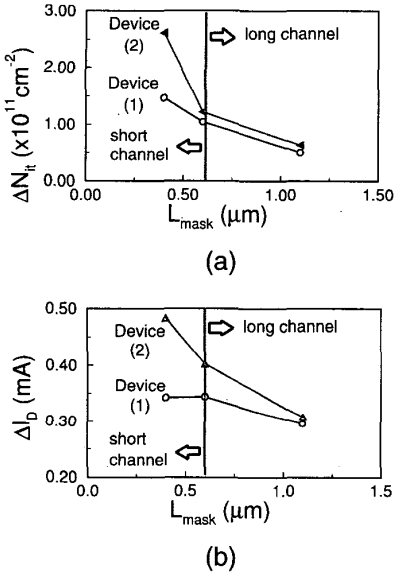

Fig. 3 (a) Length dependence of N_{it}, and (b) length dependence of I_D degradation.

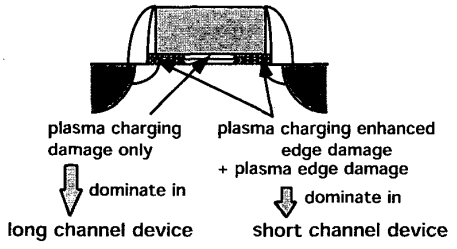

Fig. 4 Mechanisms for describing the length dependent HC effect.

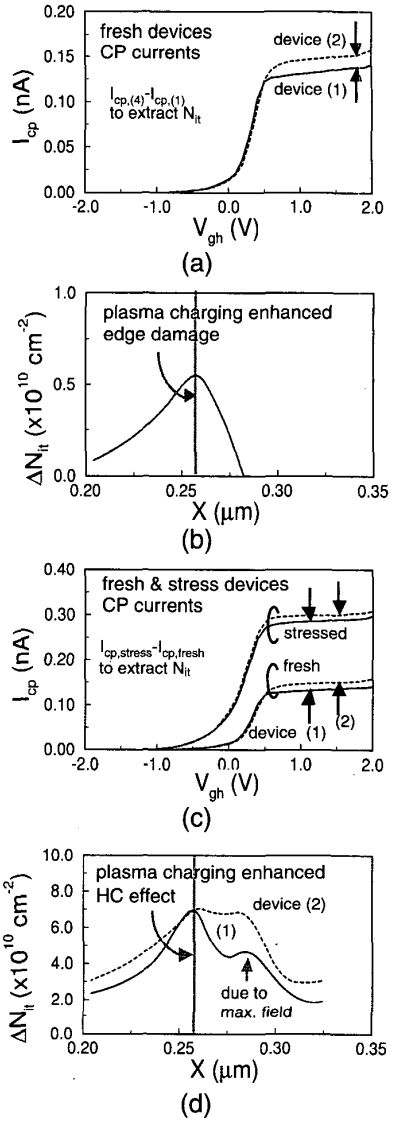

Fig. 5 (a) and (b): I_{cp} and N_{it} for plasma charging enhanced edge damage. (c) and (d): I_{cp} and N_{it} due to plasma charging enhanced HC effect. Note that 2 peaks of N_{it} are observed.

4. Results and Discussion

A. PCE-HC Effect for Scaled n-MOSFET's

Figs. 3(a) and 3(b) show the calculated interface states (N_{it}) by CP measurement and the measured drain current (I_D) degradation respectively for the long and short channel devices. The N_{it} and ΔI_D are functions of channel length. It was found that: (1) Antenna effect induced N_{it} generation and I_D degradation is enhanced for short channel devices, but not for long channel devices. (2) The device with high-density comb-like antenna structure has large HC degradation due to electron shading effect [6-7] and a large peripheral length. (3) The I_D

degradation is proportional to the interface state generation. Therefore, we conclude in Fig. 4 that, for long channel device, the plasma charging damage dominates the device degradation, while for short channel devices, plasma charging will also enhance the edge damage and the edge damage will dominate the device degradation. So, the PCE-HC effect is promiannt only in short channel devices as described in Fig. 4(b).

B. Verification of Plasma Charging Enhanced Edge Damage

To justify the above reasoning, the CP profiling technique [4] has been employed to calculate the interface states (N_{it}) generation. To calculate the PCE-ED, I_{cp} currents for devices (1) and (2) are measured in Fig. 5(a). Fig. 5(b) shows the distribution of N_{it} generation for this type damage whose peak is at 0.26μm. To calculate the PCE-HC, I_{cp} currents for fresh and stressed devices (1) and (4) are measured in Fig. 5(c). Major findings are given in Fig. 5(d), in which the edge damage has a 2-peak distribution. The left peak, at 0.26μm, is due to the PCE-HC effect, while the right peak, at 0.30μm, is located at the maximum electric field. Fig. 6 shows the position of the maximum electrical field, where conventional HC effect occurs. It was found that *the peak N_{it} of PCE-HC is even larger than that of conventional HC.* This implies that PCE-HC effect plays an important role of the device degradation in short channel devices.

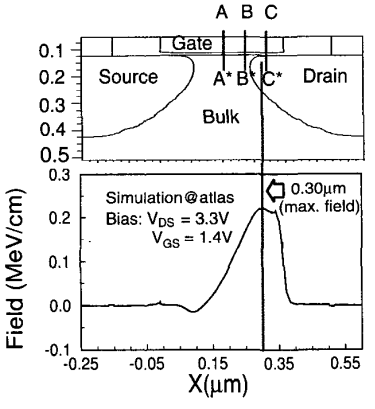

Fig. 6 Simulated electric field for device under HC ($@I_{B,max}$) stress.

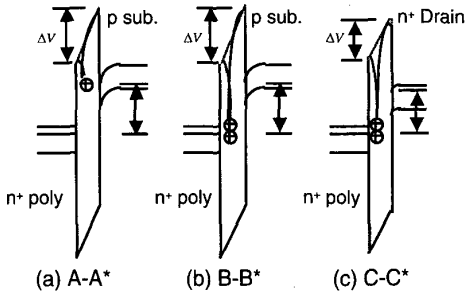

Fig. 7 Energy band diagrams for three regions in Fig 6: (a) A-A* ; (b) B-B* ; (c) C-C*. Note that B-B* has larger ΔV and oxide trap.

To explain the position of PCE-HC, Fig. 7 shows the energy band diagrams of the metal-oxide-silicon cross-section at three positions in Fig. 6. At the B-B* cut-line, it has larger positional drop (ΔV) and larger amount of oxide traps to pull-down the oxide barrier, which is vulnerable to the plasma induced FN currents. Therefore, the PCE-ED is occurred at the B-B* (0.26μm).

C. PCE-HC Effect in Surface Channel p-MOSFET's

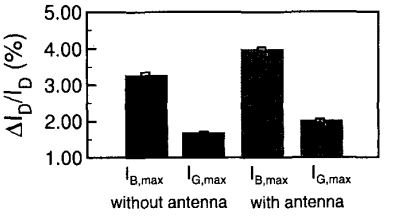

Fig. 8 Device degradations for 2 types of antennas under $I_{B,max}$ and $I_{G,max}$ stresses.

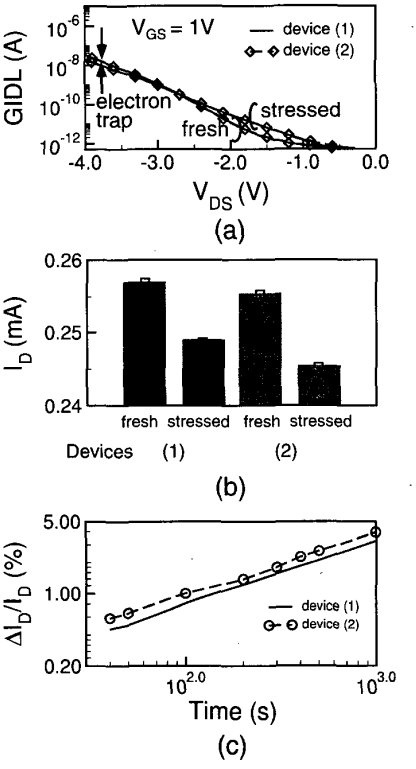

Fig. 9 GIDL and drain current degradations for two kinds of antenna structures. (a) GIDL current, (b) drain current, and (c) time dependent $\Delta I_D/I_D$ degradation.

Fig. 8 shows the drain current degradations for the surface channel p-MOSFET's under $I_{B,max}$ and $I_{G,max}$ stress conditions. The devices stress under $I_{B,max}$ condition show a larger HC degradation for larger antenna structure devices. Therefore, the surface channel p-channel evices are stressed at

$I_{B,max}$ condition for studying the PCE-HC effect. The GIDL currents are used to monitor the oxide trap generation near the gate edge. Fig. 9(a) shows that: (1) only small amount of electron traps is generated in this stress condition, and (2) no difference in GIDL currents for these devices even in fresh or stressed conditions. Fig. 9(b) shows the decreasing drain currents. From the Figs. 9(a) and 9(b), we can find that the interface states is dominant of the HC effect. However, in previous study [3], the HC effect is independent of antenna ratio in this stress condition. This implies that the PCE-HC effect also exists in surface channel p-MOSFETs. Fig. 9(c) shows the time dependence drain current degradation. Device (2) with antenna structure still has larger HC degradation.

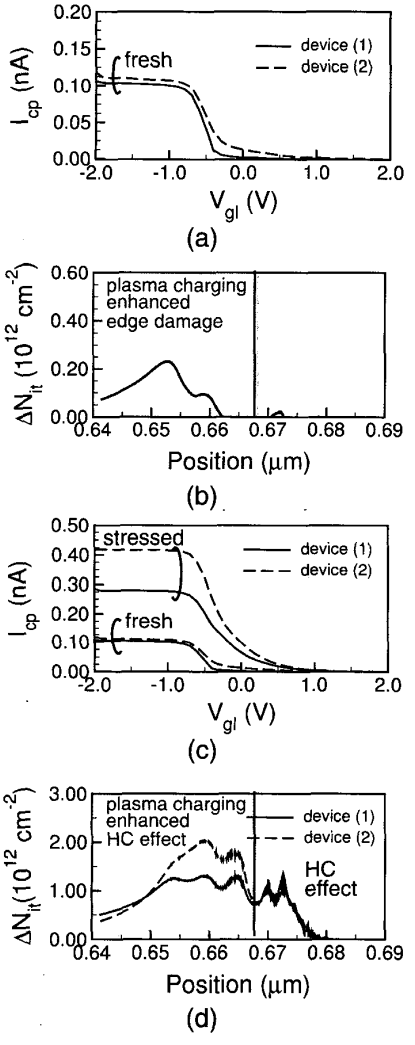

Fig. 10 (a) and (b): I_{cp} and N_{it} for plasma charging enhanced edge damage. (c) and (d): I_{cp} and N_{it} due to plasma charging enhanced HC effect. Note that 2 peaks of N_{it} are observed.

In a similar way to that of n-MOSFET, Fig. 10(b) shows the calculated N_{it} due to PCE-ED, and Fig 10(d) shows the associated N_{it} due to PCE-HC effect. Fig. 11 shows the position of the maximum electrical field. Note that two N_{it} peaks are also observed in Fig. 10(d). We conclude that antenna structure in both n- and p-MOSFET will enhance the same HC degradation.

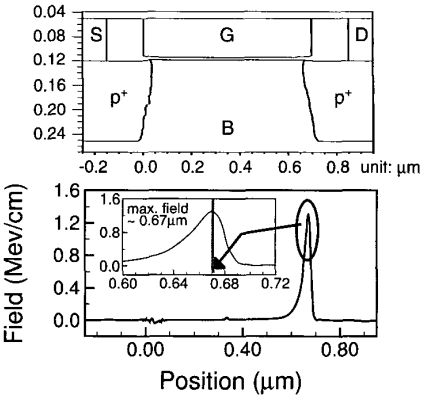

Fig. 11 Simulated electric field for device under HC ($@I_{B,max}$) stress.

5. Summary and Conclusion

In summary, a new 3-phase plasma induced damage mechanism (Fig. 2) has been proposed for antenna effect studies in both n- and p-type MOSFETs. It was found that with the scaling of device channel length, the *PCE-ED* (Fig. 5(d)) will dominate the device degradation. In other words, the plasma charging through the antenna structure will enhance the damage at the poly-Si gate edge, which makes the gate oxide be more fragile in this region. As a consequence, devices will exhibit a much larger interface state at the near drain region after plasma process, and then gives rise to a larger I_D degradation. The developed profiling technique can be used as a good monitor of the plasma charging induced damage. Also, the PCE-HC effect should be considered as an important factor for designing plasma damage immune process.

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