Fig. 2a and b shows the DC characteristics of a 0.7 × 50μm² Cd-gate JFET. The threshold voltage taken at 5 mA/mm of drain current is ~0.0V and the forward gate turn-on voltage (I_{GS} = 1mA/mm) is 0.95V. The extrinsic transconductance (V_{GS} = 1V and V_{DS} = 1.5V) is 165mS/mm with a saturation current of 130mA/mm under the same bias conditions. The DC output conductance taken for V_{DS} = 1 – 2V and 1V on the gate is 13mS/mm and the subthreshold slope is 100mV/decade. f_t and f_{max} of 0.7 × 100μm² Cd-gate JFETs, determined from measurements up to 50GHz on a HP 8510 C network analyser with V_{GS} = 0.8V and V_{DS} = 1.5V, are 26 and 42GHz, respectively. These frequency metrics are both higher than for a similar 0.7 × 100μm² Zn-gate JFET with f_t and f_{max} of 21 and 41GHz, respectively, processed in parallel with the Cd-gate JFET reported here.

The application of Cd-implantation to GaAs JFETs is shown to yield very shallow p^+-gate profiles with junction depths on the order of 35 nm after the implant activation anneal. No evidence of in-diffusion of the Cd is seen in SIMS profiles when co-implanted with P. Self-aligned GaAs JFETs employing Cd-gate regions demonstrate excellent DC characteristics and show high frequency performance superior to previous Zn-gate JFETs.

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High-barrier Pt/Al/*n*-InP diode

Wen Chang Huang, Tan Fu Lei and Chung Len Lee

Indexing terms: Schottky-barrier diodes, Indium phosphide

A new Pt/Al/*n*-InP contact diode, which has a good I-V characteristic is studied. It has a barrier height of 0.74eV, which increases to 0.99eV when it is treated with HF, an ideality factor of 1.18, and a reverse leakage current of 5.5 × 10^{-8}A/cm² at –3V. This good performance is believed to be due to the combined effects of the formation of an interfacial oxide layer and fluorine passivation on the surface.

Owing to the surface Fermi level pinning, which arises from the presence of large surface states and other nonstoichiometric defects, a barrier height >0.5eV is very difficult to obtain on *n*-InP. Such a small barrier height causes a large reverse leakage current and hinders the development of InP device applications. Various techniques such as adding an interfacial oxide layer [1] on the InP surface, were employed to increase the Schottky barrier height. Recently, a low temperature (77K) deposition was reported [2] for the metal/*n*-InP contact, giving a barrier height of 0.96eV, and Ag/Al was used to make contacts to *n*-InP, giving a barrier height of 0.65eV [3].

In this Letter, we report a Pt/Al/*n*-InP diode made with a simple process and with a barrier height of 0.99eV with an ideality factor of 1.18 and a reverse leakage current of 5.5 × 10^{-8}A/cm² at –3V.

For the experiments, the devices were made on undoped (100) InP substrates with a concentration of 5–9 × 10^{15}cm^{-3}. Ohmic contact was first formed on the backside of the substrate by evaporating AuGeNi and annealing at 400°C for 3min. The wafers were then degreased with acetone (ACE), methanol and deionised water in sequence and then soaked in H_2SO_4 (98%) for 3min and etched in NH_4OH:H_2O_2:H_2O = 3:1:15 for 3min. 2000Å of SiO_2 was then deposited on the wafers and contact patterns were defined. The multilayer Pt(500Å)/Al(85Å) metal was deposited sequentially on the samples in a vacuum of 4 × 10^{-6}torr. The diode area was equal to 4.4 × 10^{-5}cm². The wafers were then annealed in an N_2 gas flow in a furnace. Finally, the wafers were dipped in an HF:H_2O = 1:1 solution for a few seconds and rinsed in water.

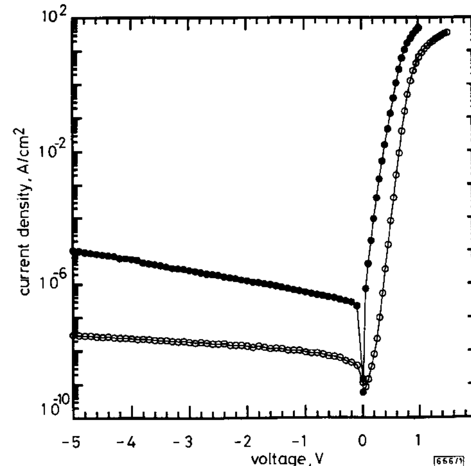

Fig. 1 *I-V characteristics of Pt/Al/n-InP diodes*

● after annealing at 400°C for 10min
○ after annealing at 300°C for 10min followed by HF dipping for 3sec

Fig. 1 shows the current-voltage (I-V) characteristics of the fabricated Pt(500Å)/Al(85Å)/*n*-InP diodes. For the 400°C annealed diode, the barrier height, the ideality factor and the reverse leakage current density at –3V were 0.75eV, 1.26 and 2.74 × 10^{-6}A/cm², respectively. For the HF-dipped diode, the barrier height was 0.99eV. This value appears to be the highest value ever reported for the metal/*n*-InP barrier height. The ideality factor was 1.18 for

over seven decades of current and the reverse leakage current was 5.5×10^{-8}A/cm² at the bias of −3V. The barrier heights derived from the corresponding C-V characteristics were 0.88 and 1.17eV for the 400°C annealed diode and the HF-dipped diode, respectively. They were substantially larger than the values obtained from the I-V characteristics. This might be due to the existence of the interfacial layer at the contact surface, as discussed later.

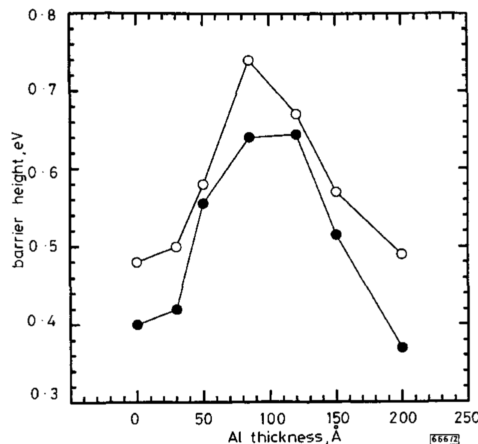

Fig. 2 *Barrier dependence against Al thickness*

● as-deposited Pt/Al/*n*-InP diodes
○ 400°C annealed diodes

Fig. 2 shows the dependence of the barrier height on the Al thickness of the Pt/Al/*n*-InP diode, where the thickness of Pt was kept constant at 500Å and the thickness of Al was varied from 0 to 200Å for both the as-deposited and annealed diodes. For the Pt/*n*-InP contact, i.e. the thickness of Al was zero, the barrier height was 0.4eV. As the Al thickness increased to 85Å, the barrier increased to 0.64 and 0.75eV for the as-deposited and annealed diodes, respectively. It was reported in [4] that for the InP wafer, after the final rinse in the de-ionised water, a thin native oxide, $InPO_4$, exists on the surface. It is speculated that this native oxide reacted with the deposited Al during the deposition process to form an aluminum oxide at the contact surface, and that this aluminum oxide serving as the sandwiched insulator between the InP substrate and the Pt layer which was deposited afterwards, increased the barrier height. As the thickness of deposited Al increased, the thickness of the interfacial layer increased also and, as a result, the effective barrier height increased further. However, as the thickness of the Al layer was great, for example larger than 120Å, some unreacted Al remained. Hence, the contact would have a Pt/Al/interfacial-layer/InP contact structure. The diode electrical characteristic would become that of the Al/interfacial-layer/InP diode, which has a very low barrier height and a large leakage current. So for the plots of Fig. 2, $Ø_b$ increased and then decreased with increasing Al thickness. Furnace annealing promoted the reaction between the Al and the oxide. This is shown in Fig. 2, where for the annealed devices, all the barrier heights were higher. Fig. 3 shows the in-depth SIMS profiles of the Pt/Al/*n*-InP diode after having been annealed at 300°C for 10min and then HF-dipped for 3s. There existed a significant amount of oxygen at the interface. This supports the formation of aluminum oxide at the contact surface. There also existed a fluorine peak at the interface. It was reported that in the metal/SiO_2/Si system, the presence of fluorine reduces the number of interface traps, since fluorine can passivate the interfacial dangling bonds and weak bonds of the interface. It was also reported in [5] that fluorine can passivate the dangling bond on the GaAs surface to reduce the density of surface states. Hence, it is speculated that the presence of fluorine in this HF-dipped Pt/Al/*n*-InP diode improved the diode characteristics by passivating the interface states. The passivation of interface states reduced the Fermi level pinning effect and thus gave a greater barrier height for the high work function metal.

In summary, we have prepared a new Pt/Al/*n*-InP contact structure in a simple process that gave a good diode performance. It was found that, for this diode, as the thickness of Al increased

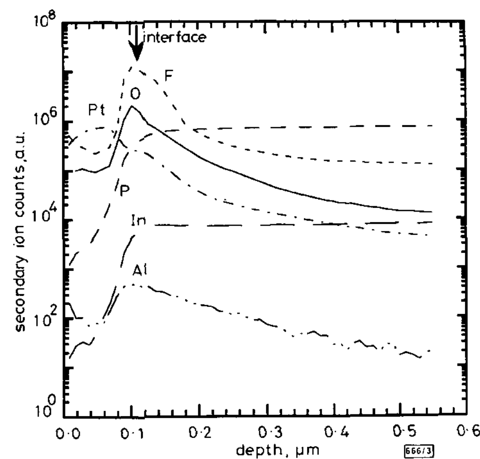

Fig. 3 *SIMS in-depth profile of Pt/Al/n-InP diode after annealing at 300°C for 10min followed by HF-dipping for 3s*

over the range 80–120Å, a high barrier value (>0.65eV) was obtained. For the diode of Pt(500Å)/Al(85Å)/*n*-InP, a barrier height of 0.99eV could be obtained if the device was HF-dipped. This performance is believed to be due to the combined effects of the formation of an interfacial oxide layer and fluorine passivation of the surface.

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Improved source resistance in InP-based enhancement-mode HEMTs for high speed digital applications

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Indexing terms: High electron mobility transistors, Indium phosphide

A new approach to reducing the source resistance in InP-based InAlAs/InGaAs enhancement-mode HEMTs is developed using Pt-based buried-gate technology. Source resistance as small as 0.2Ωmm is obtained, which results in an excellent transconductance of 1170 mS/mm for a 0.5µm long gate enhancement-mode HEMT.