Random Line selected Charge Accumulation (RLCA) CCD readout structure for high frame rate infrared image application

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ABSTRACT

A 512×512 monolithic Platinum Silicide Schottky Barrier detector array with random line selectable operation was proposed. The device modified from an interline CCD configuration by adapt a Random Line selected Charge Accumulation charge-coupled device on the vertical register and four tap readout on the horizontal CCD register to achieve a high frame rate and high fill factor operation. A 9-bit digital decoder is used to select which line of the sensor array that transfer their signals to the vertical CCD register. Accompanied with the vertical reset drain circuitry, either one line or up to 512 lines of the video signals can be selected and transferred to the vertical CCD register. All of the video signals on the unselected lines are then transferred to the vertical CCD channel simultaneously and finally dumped to the vertical reset drain. Since this unique readout structure, a frame rate of up to 240 frames/second can be achieved for 128×128 of the SBD array under 5 MHz of clock frequency. A high-speed sub-frame readout format can be easily fulfilled under this architecture. This architecture not only maintains the advantages of line-addressed charge-accumulation structure but also provides the capability to readout any portion of the array.

Keywords:PtSi Schottky-barrier detector, Random line selected charge accumulation, Charge coupled device, Line-addressed charge-accumulation

1. INTRODUCTION

PtSi/p-Si Schottky-Barrier Detector (SBD) have long been recognized to detect the infrared wavelength in the range of 3 μm to 5 μm. Due to the comparable fabrication process with standard Silicon process, large two-dimension PtSi arrays combined with charge coupled device (CCD) multiplexer has been reported by several workers[1-5]. The most common structure used in a Schottky barrier array is an Interline-Transfer CCD (ITCCD) readout structure[1]. In this manner, one stage of CCD register associated with one SBD. When a frame is being read out, the charge of each SBD is transferred into its corresponding CCD register simultaneously. The charge handling capacity of the CCD register needs to be bigger than the saturation charge of the SBD in order to prevent any blooming effect. In this case, the area of the SBD and vertical CCD channel has to compromise. Therefore, it is very difficult to achieve a high fill factor with high charge handling capacity and high dynamic range under ITCCD structure. To overcome this problem, a Charge-Sweep Device (CSD) readout structure was proposed by Mistibushi[2]. In CSD readout structure, the array is read out one row at a time by a scanning register. When a row of SBDs are addressed by the scanning register, the signal charge of each SBD is then transferred into the CSD register. The charge is distributed over all of the gates in the CSD register. Since the signal charges spreads over all of the vertical CSD gates, the CSD channel can be designed very narrow. As a result, arrays with high fill factor can be built even the pixel size is very small. In additional to solve high fill factor problem on CSD readout structure, a high frame rate of up to 75 frames/sec can also be obtained under the Line-Addressed Charge-Accumulation (LACA) readout structure that proposed by W.L. Wang et al. [3]. The LACA readout structure combines the advantages of the ITCCD structure, its low speed requirement on the vertical register, and the advantages of the CSD structure, its high fill factor.

In this paper, a Random Line selected Charge Accumulation (RLCA) CCD readout structure is proposed. A 9-bit digital decoder is used to select which line of the sensor array that transfer its signal to the vertical CCD register. Accompanied with the vertical reset drain circuitry, either one line or up to 512 lines of the video signals can be selected and transferred to the vertical CCD register. All of the video signals on the unselected lines are then transferred to the vertical CCD channel

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In *Infrared Detectors and Focal Plane Arrays VI*, Eustace L. Dereniak, Robert E. Sampson, Editors,
Proceedings of SPIE Vol. 4028 (2000) • 0277-786X/00/$15.00

simultaneously and finally dumped to the vertical reset drain. Therefore, a high-speed sub-frame readout format can be easily fulfilled under this architecture. The RLCA CCD readout structure combines the advantages of the both ITCCD, CSD and CMOS multiplexer. Section 2 describes the mechanism of a random line selected charge accumulation readout structure. Section 3 explains the device architecture and operation. The experimental results will be presented in section 4. Section 5 draws a conclusion.

2. RANDOM LINE SELECTED CHARGE ACCUMULATION (RLCA) READOUT STRUCTURE

In the RLCA structure, each SBD associated with its corresponding CCD gate as in the LACA structure. It means that only one phase of the vertical CCD register corresponding to one SBD. Several CCD gates are grouped together to form one stage of the vertical CCD. The operation of the phase number in the vertical CCD is determined by how many counts of the grouped gates. Four gates to form one stage of a four-phase vertical CCD register are used in this design.

A 9-bit decoder is used to select any row of the SBD array. When a row of SBD array is selected, the signal charges of that row are then transferred into vertical CCD channel through its associated transfer gate. The transfer gates on each row of the SBD are tied together and controlled by the combination of the decoder output and vertical transfer pulse. The charge transferred from SBD to vertical CCD register will spread over three gates of the four-phase vertical CCD. Therefore, the requirement on the vertical CCD channel width is decreased to less than 1/3 of the channel width on ITCCD readout structure. Four-phase clock pulse on the vertical CCD moves that charge toward and collected on the storage gate. After several clock cycles later, the storage gate accumulated all of the original charge from SBD. In this readout mechanism, the original charge on the SBD is spread over on the vertical CCD and then collected back on the storage gate. Those charges are then transferred from storage gate into horizontal CCD. Through the horizontal CCD transfer, the signal charge is converted to the voltage signal by the charge integrator.

2.1. Charge accumulation and separation process

The vertical CCD channel is narrow in the RLCA structure, the charge accumulation process is required to compromise the charge loss due to poor charge transfer efficiency. Since only one row of the SBD array is selected during one line of the transfer period, the signal charge can not mixed together no matter what the number of clock pulses are chosen. As a result, two adjacent rows of SBD array is then separated by the over-clocking number of the CCD stages. Figure 1 shows the charge separation mechanism. If the charge loss is neglected, the total collected charge of each SBD in the storage gate can be calculated. For example, when the charge package "Q" is transferred to the stage # 1 of vertical CCD. The charge loss is $Q(1-\varepsilon)$ in stage # 1 and the charge transfer to stage # 2 is $Q\varepsilon$ after one charge transfer cycle. Where ε is charge transfer efficiency per stage on vertical CCD. After second transfer cycle, the charges on stage # 1, stage # 2, and stage # 3 are $Q(1-\varepsilon)^2$, $Q[(1-\varepsilon)\varepsilon+(1-\varepsilon)\varepsilon]$, and $Q\varepsilon^2$, respectively. Therefore, for five over-clocking cycles, the total charge accumulated on the storage gate can be expressed as $Q_1 = \varepsilon^5[1+5(1-\varepsilon)+15(1-\varepsilon)^2+35(1-\varepsilon)^3+70(1-\varepsilon)^4]$, $Q_2 = \varepsilon^6[1+6(1-\varepsilon)+21(1-\varepsilon)^2+56(1-\varepsilon)^3+126(1-\varepsilon)^4]$ and so on. A diagonal matrix is used to describe the charge transfer mechanism. This matrix is illustrated below,

$M(1,1)$

$M(2,1)\ M(2,2)$

$M(3,1)\ M(3,2)\ M(3,3)$

$M(4,1)\ M(4,2)\ M(4,3)\ M(4,4)$

. . . .

$M(m,1)$ .....$M(m,n)$

. . . .

$M(512,1)\ M(512,2)$..... $M(512,512)$

M(1,1) is treated as the beginning of the charge packet "Q". M(2,1) is the lost charge and M(2,2) is the transferred charge after first transfer period. Therefore, M(2,1) equals to M(1,1)*(1-ε) and M(2,2) equals to M(1,1)*ε. M(3,3) is the charge transfer from M(2,2). M(3,2) consists of two components, one is the transfer loss of M(2,2) and the other is the charge transfer of M(2,1). Thus M(3,2) should be M(2,2)*(1-ε) + M(2,1)*ε. M(3,1) is the charge loss of M(2,1). Following this transfer mechanism, a general relationship of M(m,n) can be expressed as M(m,n) = M(m-1,n-1)*ε + M(m-1,n)*(1-ε), where m is treated as the number of transfer from the original charge packet "Q" transferred to vertical CCD, n is the charge location stage during m transfer. The total transfer efficiency (TTE) of each row is then calculated from the computer simulation.

2.2. Random line selection process

Each row of transfer gates between SBD sensor and vertical CCD register is connected together to form a transfer address line. There are 512 transfer address lines in the 512×512 array. A 9-bit decoder is used to control 512 transfer address lines. By select a pattern on 9-bit decoder, one address line can be turned on and transferred the signal charge into its corresponding vertical CCD register. Therefore, one complete line of the SBD is read out simultaneously. Figure 2 shows the RLCA readout architecture. The timing diagram to operate this device is shown in figure 3. A 9-bit decoder driven by the address bits denoted by A_0 to A_8. Only one address line is selected at a time. The address line controlled by both the decoder output and vertical transfer pulse, Φ_{TV}. The transfer gate of the selected row turned on by the vertical transfer pulse, Φ_{TV}. The charge is then transferred into vertical CCD register during the transfer gate is turned on. After charge transferred, transfer gates turned off by the clock pulse, $\overline{\Phi}_{TV}$. The channel potential of the SBD is reset into a level controlled by $\overline{\Phi}_{TV}$. The signal charge on the vertical CCD register is shifted toward the storage gate by several over-clocking pulses. After all of the original charge collected by the storage gate, the second selected line is activated and the selected signal charge is also transferred into the vertical CCD register. Therefore, two adjacent rows of the signal are separated by several vertical CCD stages. Since each transfer line addressed by the decoder, the readout sequence of the SBD array can be randomly selected. Accompanied with the vertical reset drain circuitry, only one or up to 512 lines of the SBD array can be easily selected and readout. The unselected lines of the sensor array are then transferred into vertical CCD channel simultaneously and dumped into vertical rest drain through the vertical CCD register. As a result, high-speed sub-frame operation can be achieved under this readout structure.

3. DEVICE DESIGN AND CONSTRUCTION

The device is fabricated with 1μm double poly and double metal buried channel CCD process. It consists of seven components. First component is a CMOS 9-bit decoder. Second components is a 512×512 PtSi SBD elements. Third component is 514 vertical CCD columns (512 active columns and two dummy columns to eliminate the edge effect) with each column consisting of 128 four-phase CCD stages. Fourth component is 512×1 storage gate and their horizontal transfer gates. Fifth component is vertical reset drain circuitry accompanied with the storage gate. Sixth component is four 128×1 horizontal CCD registers. Seventh component is four resets and two-stage source follower amplifiers. The block diagram of the device construction is shown in Fig. 2. Each pixel size is 25×20μm^2. Each pixel size consists of one well of CCD stage and one SBD. Four CCD wells are grouped together to form four-phase vertical CCD operation. A fill factor of more than 45% obtained under this architecture. In addition to the high fill factor, a high charge handling capacity is also achieved in this design. Since the number of charge handling wells of vertical CCD register is determined by the time period of ON stage on Φ_{TV}, the charge handling capacity of vertical CCD is only limited to the storage gate. This design architecture really provides the flexibility of the requirements on fill factor and charge handling capacity.

In the horizontal register, a four tap-output structure is designed. Each tap-output consists of 128-stage horizontal CCD, one pixel sense and reset circuitry and one on-chip amplifier. Since this unique design, one can achieved a high frame rate operation without applying a high speed clocking. A requirement of very powerful driver to drive the horizontal CCD gates at high frequency is also eliminated.

On the RLCA readout structure, line readout sequence is controlled by the selection pattern of a 9-bit decoder. Each line transfer period depends on the clock frequency of the horizontal CCD. When the clock frequency of the horizontal CCD is 2.5MHz, each line period of 128 stages is 55.2μs. This time period also decides one clock cycle of the vertical transfer

pulse. If over-clocking stages in vertical CCD is n, the relation between time period of vertical transfer pulse, t_{VTP}, and the vertical CCD clock period t_V is expressed as follows.

$$t_{VTP} = (\frac{4n-1}{4})t_V, \quad (1)$$

If the over-clocking stages is equal to six and t_{VTP} is 55.2μs, then vertical CCD clock period, t_V, is calculated to 9.6μs. Under this operation condition, one can obtain a 33 frames/sec of readout format. If the operation frequency on horizontal CCD is increased to 5MHz, the frame rate is also increased to 66 frames/sec. Using RLCA structure accompanied with vertical reset drain circuitry, a high-speed sub-frame operation can be fulfilled. Each sub-frame rate is determined by how many rows of the SBD signal is going to readout. The time period, t_N, for N rows of signal readout can be presented as the following equation,

$$t_N = t_{VTP}[N + \mathrm{mod}(\frac{N}{4n})], \quad (2)$$

where, t_{VTP} is one line transfer period, N is number of selected readout rows of SBD signal, $\mathrm{mod}(\frac{N}{4n}) * t_{VTP}$ is the time needed to shift the Nth row of the signal into storage gate. After the Nth row of the signal transferred into horizontal CCD, the vertical reset drain circuitry is turned on. All of the unselected signals in SBD array are transferred into vertical CCD channel and dumped to the vertical reset drain. As a result, a high-speed sub-frame operation can be achieved in this design. The sub-frame rate of up to 240 frames/sec can be designed for 5 MHz of horizontal CCD clock frequency on 128×128 resolution.

4. EXPERIMENTAL RESULTS

Figure 4 shows the Total Transfer Efficiency (TTE) comparison between RLCA architecture and conventional ITCCD structure. For 0.99 of CTE per stage, the TTE after 30 stages transferred for both RLCA and conventional ITCCD are 99.99% and 73.97%, respectively. It is obviously that total transfer efficiency is improved a lot in the RLCA readout architecture. Figure 5 describes a simulated result of the TTE as a function of the row stages of SBD pixels for different charge transfer efficiency. Based on this simulation, the CTE per stage and the number of over-clocking pulses can be optimized. For a 512 CCD gates with a CTE of 0.99 per stages, the storage gate will accumulate 99.99% of the charge when five over-clocking stages.

To evaluate this device, a 9-bit decoder is operated on the sequential scan mode. The horizontal clock frequency is setting on 2.5 MHz, and the over-clocking of the vertical CCD is arranged to six clock cycles. The detailed timing diagram to operate this device is shown in figure 3. There is four video outputs on this device. They are Video # 1, Video # 2, Video # 3, and Video # 4. Each video output covers the video signal of 128 x 512 SBDs. Video # 1 displayed left-hand side of the video signal (from first column to 128th column). Video # 2 represented left-middle side of the video signal (from 129th column to 256th column). Video # 3 demonstrated right-middle side of the video signal (from 257th column to 384th column). Video # 4 showed the right-hand side of the video signal (from 385th column to 512th column). The video signal from the array is connected to the corrected double sampling (CDS) circuitry to cancel the reset noise. Every one of four video outputs can be individually displayed on the X-Y monitor and showed a portion of the infrared imager. Figure 6 shows an example of the raw (before correction) infrared imager. In order to re-configure four portions of the imager into one imager and displayed the whole imager on a screen. An image processing board is required to combine four outputs into one output. Figure 7 shows a block diagram of the image processing circuitry. A Datel PCI-431 image processing board is used in this design. Four video outputs after CDS circuitry are connected to four inputs of the 12 bit A/D converter and convert the video signal from analog signal to digital data. On the calibration procedure of two-point correction, the digital data of both dark field and bright field are stored on two flash memories. The digital data of the real imager is then processed by digital signal processing (DSP) for two-point correction. Four corrected videos data are then re-combined into one and displayed on the VGA monitor. In-house software program was written to combine four video outputs into one video output as well as two-point correction. A combined video signal is displayed on figure 8.

5. CONCLUSION

A random line selected charge accumulation structure was designed and demonstrated for high frame rate, high fill factor, and sub-frame rate infrared image application. This architecture provides both high fill factor and high charge handling capacity. Accompanied with vertical reset drain circuitry, high-speed sub-frame operation is also achieved. The frame rate can reach up to 240 frames/sec for 5 MHz horizontal clock frequency on 128×128 SBDs resolution.

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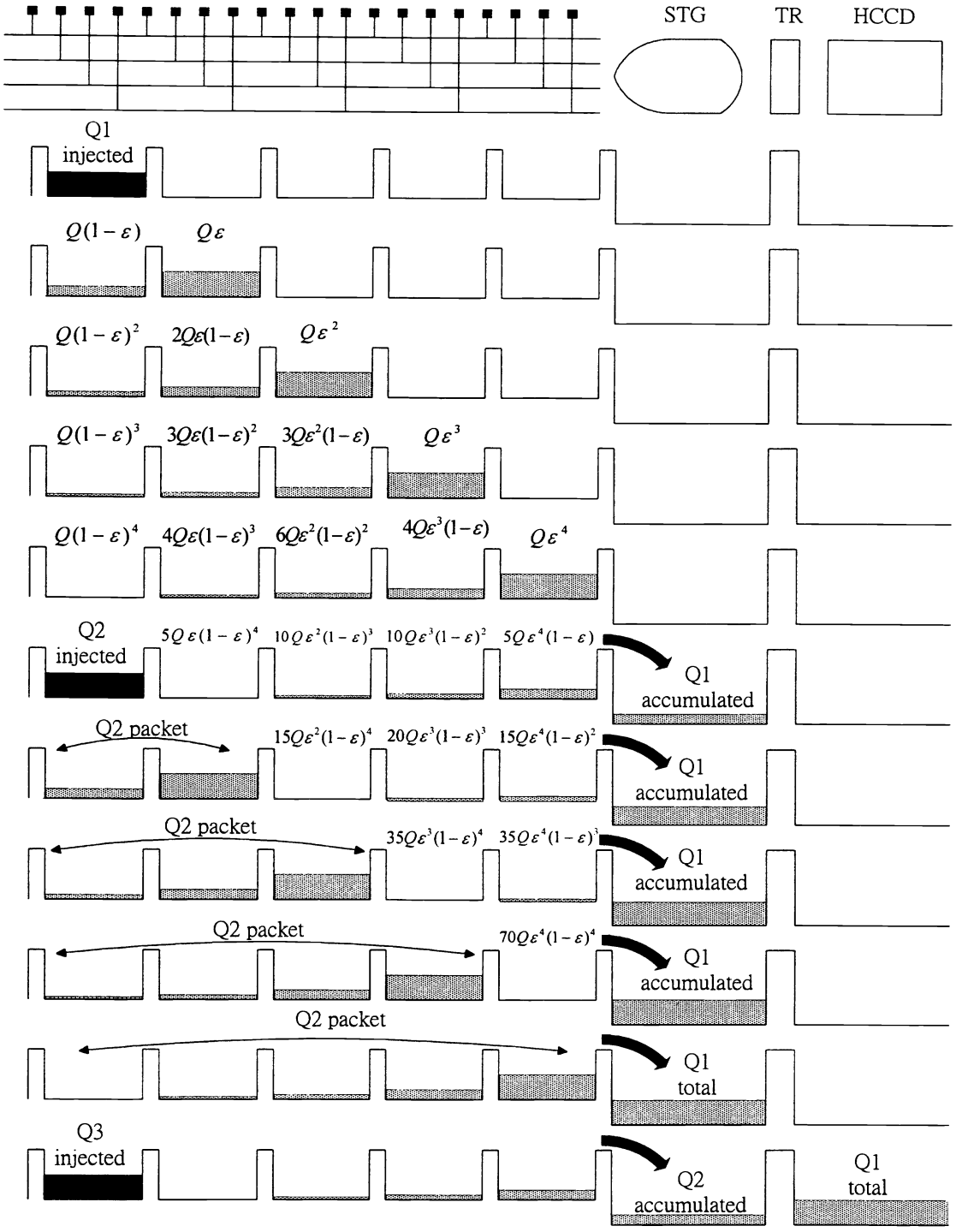

Fig. 1. The charge transfer and accumulation mechanism for RLCA structure

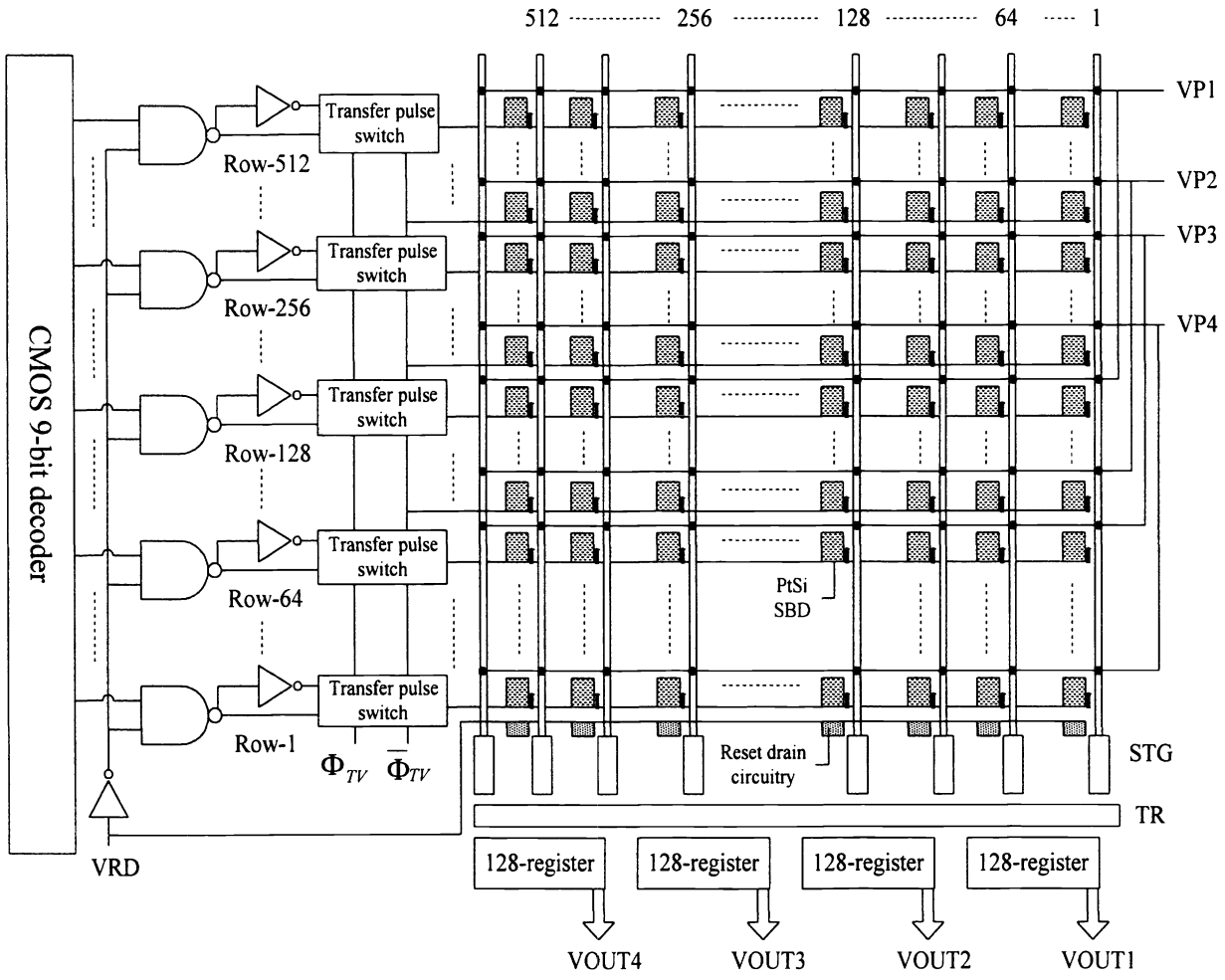

Fig. 2. The Schematic diagram of RLCA structure

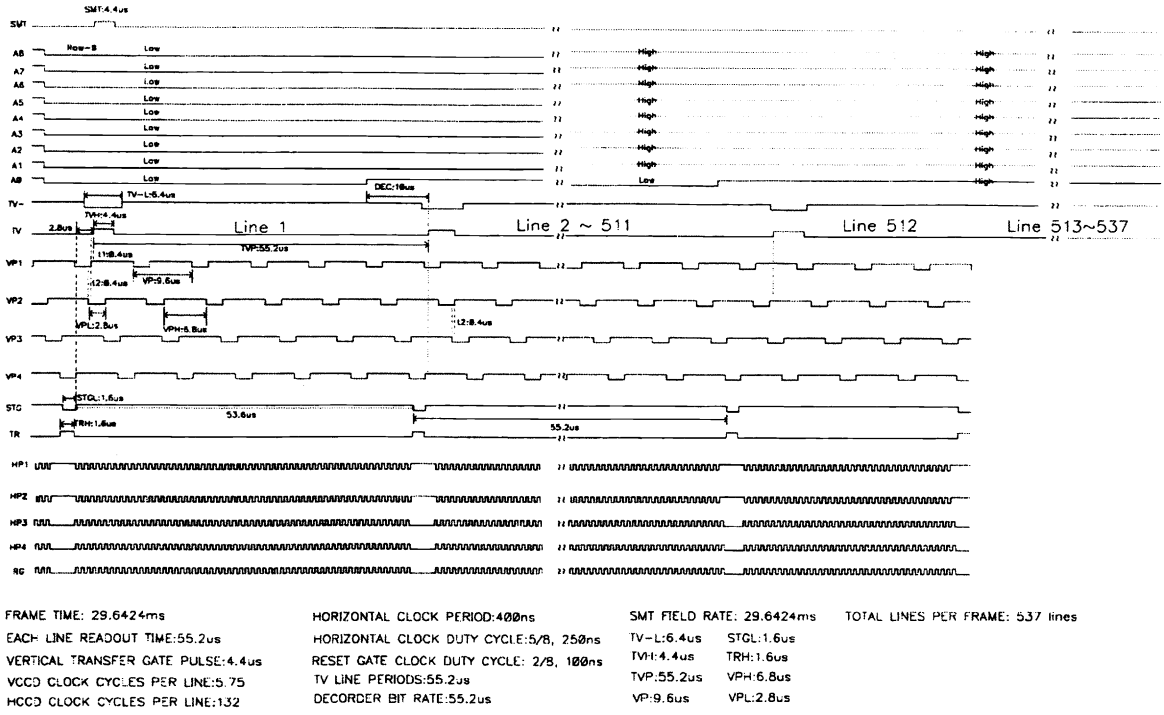

Fig. 3. The timing sequence for RLCA operation.

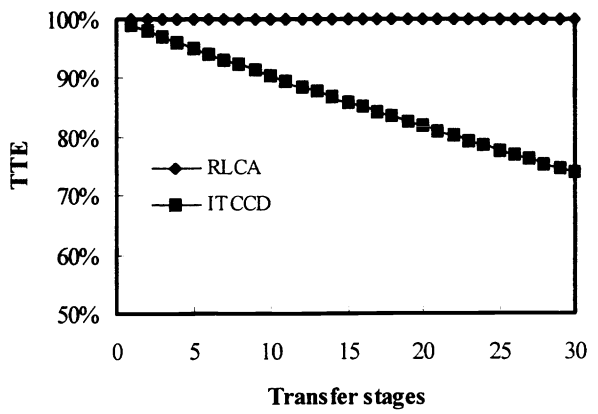

Fig. 4. The total transfer efficiency of RLCA structure compared with that of ITCCD readout.

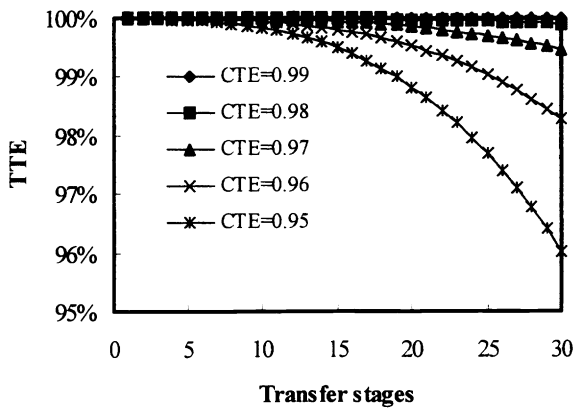

Fig. 5. The total transfer efficiency of RLCA structure for different CTE.

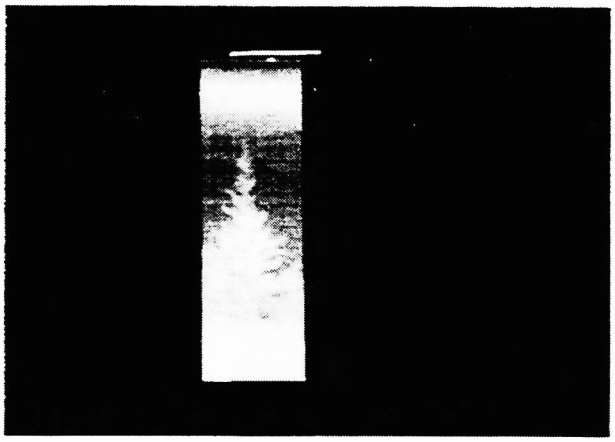

Fig. 6. The image of one video output displayed on X-Y mode monitor.

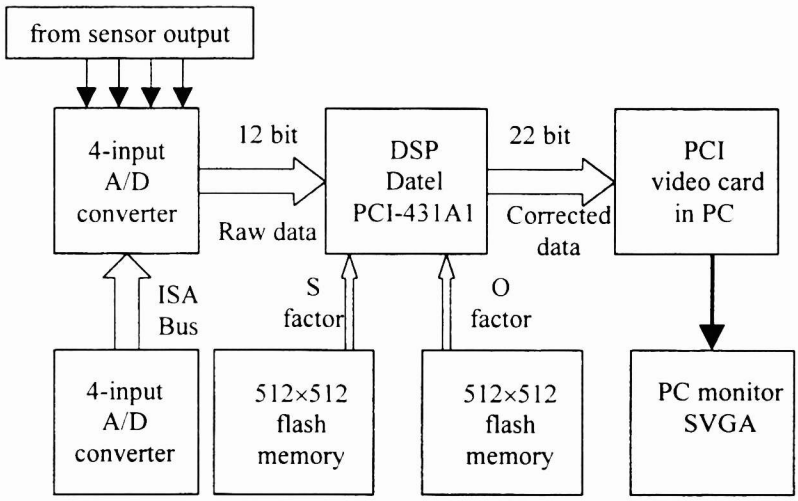

Fig. 7. The block diagram of image processing circuitry for the combination of four video outputs into one output.

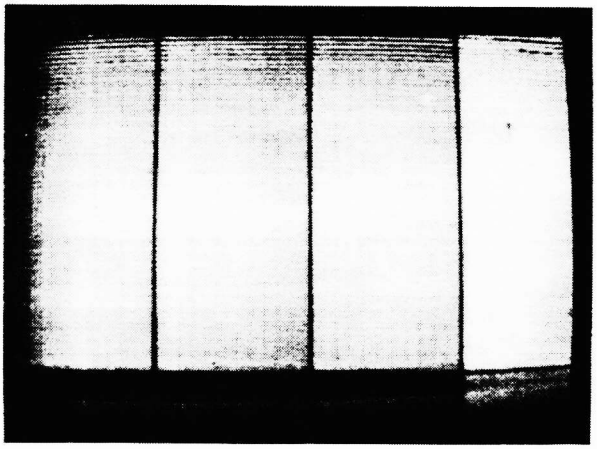

Fig. 8. The image display for a combined video signal by image processing circuitry.