Valence-Band Tunneling Enhanced Hot Carrier Degradation in Ultra-Thin Oxide nMOSFETs

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Abstract

Enhanced hot carrier degradation with stress V_g in the valence-band tunneling regime is observed. This degradation is attributed to channel hole creation by valence-band electron tunneling. The created holes provide for Auger recombination with electrons in the channel and thus increase hot electron energy. The valence-band tunneling enhanced hot carrier degradation becomes more serious as gate oxide thickness is reduced. In ultra-thin gate oxide nMOSFETs, our result shows that the valence-band tunneling enhanced degradation, as opposed to max. I_b stress induced degradation, exhibits positive dependence on substrate bias. This phenomenon may cause a severe reliability issue in positively biased substrate or floating substrate devices.

Introduction

It has been reported that Auger recombination can enhance hot electron tail and cause more serious degradation in MOSFETs [1-3]. The process for Auger recombination in various device structures and operation conditions is illustrated in Fig. 1. In Fig. 1(a), holes created by impact ionization flow to the region near the source (where electron concentration is high) in a SOI structure [4] and provide for recombination with electrons. In Fig. 1(b), a positive substrate bias is applied in a nMOSFET. As a result of substrate hole injection, the channel hole concentration and thus Auger recombination rate are enhanced [3]. In ultra-thin oxide nMOSFETs, a positive gate bias can cause valence-band electron direct tunneling to the gate and leave holes behind in the channel for Auger recombination (Fig. 1(c)). In this work, it is our intention to investigate the significance of these valence-band tunneling created holes to device reliability.

Ultra-thin oxide nMOSFETs with gate oxide thickness from 17Å to 33Å are used in this work. The devices have a gate width of 10μm. Hot carrier stress with different stress V_g is performed. Drain current degradation is measured in the triode region at V_d=0.1V and V_g=1.5V. Stress time is 500sec.

Results and Discussion

It has been shown in literature that in short channel devices hot carrier degradation at V_g=V_d stress is more serious than at max. I_b stress (V_g~0.5V_d) [5,6]. Fig. 2(a) shows the drain current degradation in two different gate-length nMOSFETs, L_g=0.20μm and L_g=0.13μm. The oxide thickness is t_{ox}=25Å. The corresponding I_b in stress is plotted in Fig. 2(b). In the 0.2μm device, the worst stress condition occurs around max. I_b while in the 0.13μm device the degradation increases monotonically with V_g. This behavior was explained in [6] because (i) the I_b-V_g curve is relatively flat in the 0.13μm device and (ii) channel hot electrons are confined more closely to the Si surface, thus leading to larger damage to the Si surface, at a larger V_g.

Notably, as stress V_g increases above 3V, a drastic rise of the degradation is observed in both devices. The subthreshold characteristics at a low V_g stress and at a high V_g stress are shown in Fig. 3. The swing degradation indicates interface trap creation by the two stresses. The stress time dependence of the drain current degradation in Fig. 4 also confirms that the degradations at a low V_g stress and at a high V_g stress are both due to interface trap creation.

To investigate the correlation between the drastic rise of the degradation and valence band tunneling, we measured I_d degradation and valence-band tunneling current in nMOSFETs with different t_{ox} (Fig. 5). The t_{ox}=33Å device has a gate length of 0.16μm and other devices have a gate length of 0.13μm. The substrate current measured at V_d=0V, which reflecting valence-band tunneling, is shown in Fig. 5(b). The following features should be noted. First, the rise of the I_d degradation in the valence-band tunneling regime is observed in all the devices except for the t_{ox}=33Å device. The valence-band tunneling current in the 33Å device is found to be negligible (result not shown in Fig. 5(b)). Secondly, the degradation at max. I_b stress decreases when t_{ox} reduces. This part is in agreement with the findings by Momose [7] that thinner oxides have better hot carrier reliability. However, an opposite trend (i.e., the degradation increases as t_{ox} reduces) is found when the devices are stressed in the valence-band tunneling regime. The process for valence-band tunneling enhanced hot carrier stress is proposed in Fig. 6. In Fig. 6(a), channel holes are created due to valence-band electron tunneling. The generated holes then provide for recombination with electrons in the channel

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and transfer the excess energy to other conduction electrons (Fig. 6(b)). The energetic electrons arising from the Auger process are subsequently accelerated by a lateral electric field near the drain (Fig. 6(c)), thus resulting in a larger hot electron tail and higher interface trap generation rate. The entire electron energy gain process therefore depends on V_g (valence band tunneling) and V_d (lateral field acceleration).

To further verify the role of valence-band tunneling created holes in the degradation, we change the substrate bias in stress (Fig. 7) to modulate the hole concentration in the channel. Fig. 8 shows the variation of I_g and I_b with substrate bias in the low V_g and high V_g stresses. For t_{ox}=20Å devices (Fig. 7(a)), the degradation in the low V_g region and in the high V_g region exhibits opposite substrate bias dependence. The simulated lateral electric field distribution and the conduction band-edge diagram in the vertical direction are plotted in Fig. 9. As V_b changes from 0V to -1V, the peak lateral channel field slightly increases (Fig. 9(a)), implying stronger lateral field heating. Moreover, the vertical field is also increased, which means the channel electrons are pushed further toward the S_i surface (Fig. 9(b)). These two factors lead to a larger gate current (Fig. 8) and increased I_d degradation in the low V_g region. In the high V_g region, we have shown valence-band tunneling plays an important role in the degradation. A negative substrate bias can help remove the channel holes to the substrate and thus reduce the hole effect. As a result, the I_d degradation becomes smaller at a negative substrate bias although the stress gate current and substrate current are larger (Fig. 8). This result actually excludes the possibility that the rise of the I_d degradation at a large V_g is primarily caused by the increase of stress I_g.

In contrast, the t_{ox}=33Å device shows negative substrate bias dependence in the entire range of stress V_g because of negligible valence-band tunneling effect. In Fig. 10, we plot the I_d degradation versus the substrate bias in stress. The stress gate bias is 1.3V (max. I_b stress) for the lower curve and 3.4V (valence-band tunneling stress) for the upper curve. The valence-band tunneling enhanced degradation, as opposed to max. I_b stress induced degradation, shows positive dependence on substrate bias and may impose a constraint in the DTMOS-like operation [8]. The degradation in a floating substrate stress condition is also indicated in the figure.

Conclusion

The significance of valence-band tunneling to hot carrier degradation in ultra-thin oxide MOSFETs has been evaluated. The valence-band tunneling enhanced degradation becomes more severe as the gate oxide thickness is reduced. Our study shows this degradation mode exhibits positive substrate bias dependence and may appear to be a new reliability issue in certain applications, such as floating substrate devices (SOI) or positively biased substrate devices (DTMOS).

Acknowledgements

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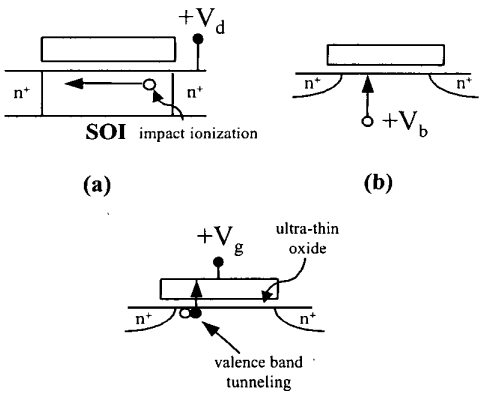
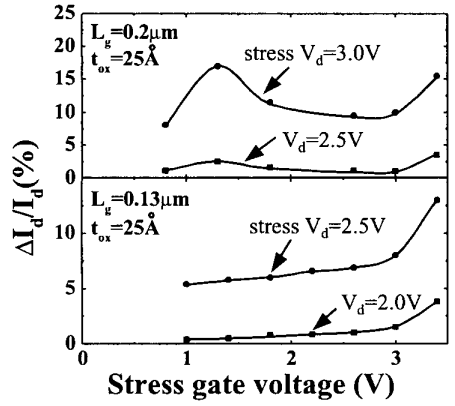
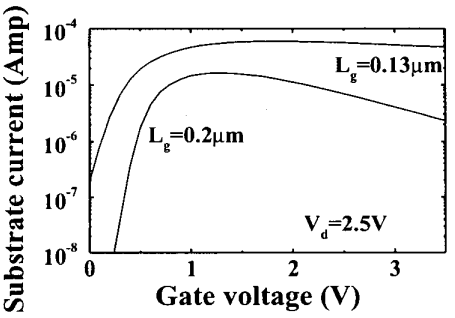


Fig.1 Auger recombination process in various nMOSFET structures and operation conditions.
(a) Impact ionization created holes flowing to the region near the source in a SOI MOSFET[4].
(b) Substrate hole injection to the channel by a positive substrate bias in DTMOS operation [3].
(c) $+V_g$ induced valance-band electron tunneling in ultra-thin oxide nMOSFETs and leaving holes in Si substrate.



(a)



(b)

Fig.2(a) I_d degradation versus stress gate bias in L_g=0.20μm and L_g=0.13μm nMOSFETs. Stress V_d is 3.0V, 2.5V and 2.0V. Stress time is 500 sec. I_d degradation is measured at V_d=0.1V and V_g=1.5V. (b) Substrate current versus gate voltage, V_d=2.5V.

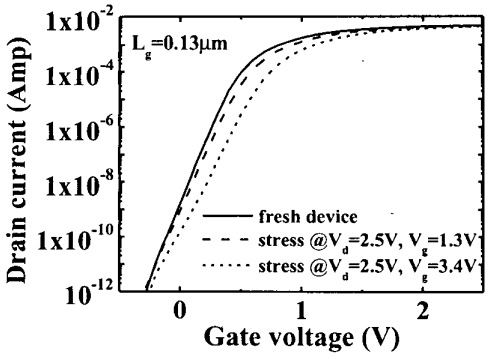


Fig.3 Measured subthreshold characteristics in a fresh device, after V_d=2.5V and V_g=1.3V stress and after V_d=2.5V and V_g=3.4V stress. Stress time is 500 sec. The swing degradation indicates that the cause of degradation is interface trap creation.

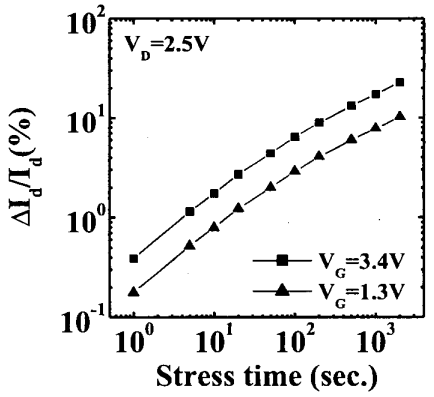


Fig.4 I_d degradation versus stress time in devices stressed at V_g=1.3Vand V_g=3.4V. Stress drain bias is 2.5V. The power factor is about 0.4. which reflects the growth rate of interface traps.

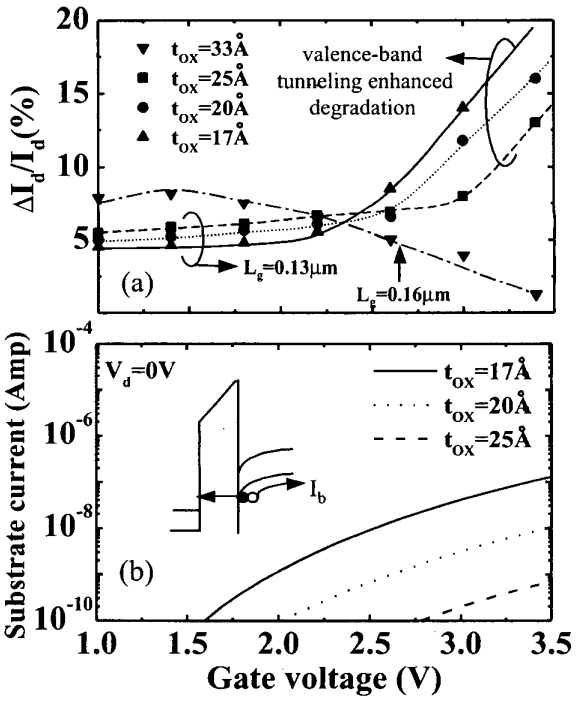


Fig.5 (a) I_d degradation versus stress gate bias in nMOSFETs with t_{ox}=17Å, 20Å, 25Å and 33Å. Stress V_d is 3.0V for the t_{ox}=33Å device and 2.5V for other devices. (b) Substrate current versus gate bias with V_d=0V. This substrate current results from valance-band electron tunneling. The valence-band tunneling current in the 33Å device is found to be negligible.

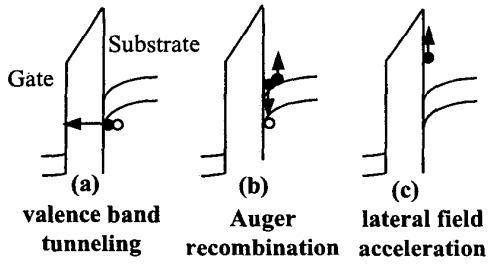


Fig.6 Illustration of valance-band tunneling enhanced hot electron process.

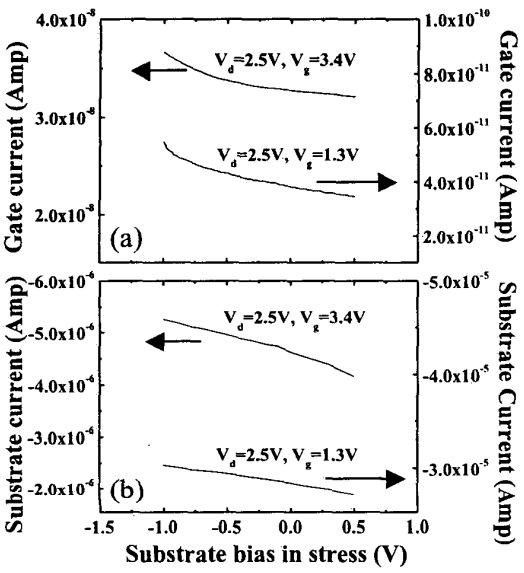


Fig.8 Dependence of gate current and substrate current on substrate bias in stress. L_g=0.13μm and t_{ox}=25Å.

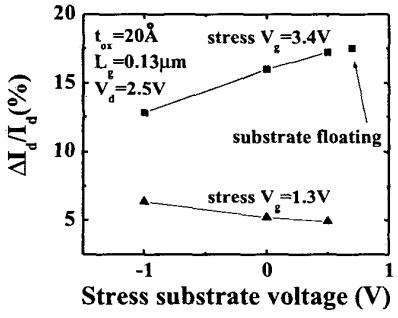


Fig.10 Substrate bias dependence of the drain current degradation at two different stress V_g, 1.3V and 3.4V. The degradation in a stress condition of V_d=2.5V, V_g=3.4V and substrate floating is indicated.

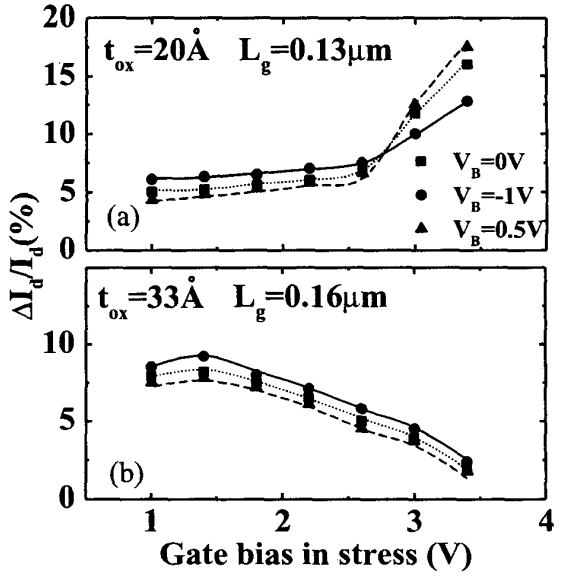
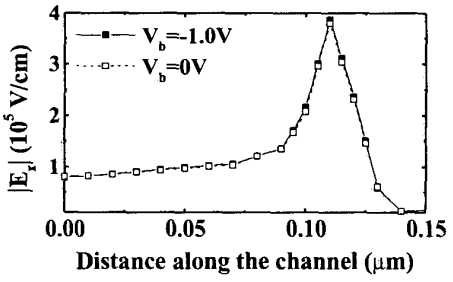
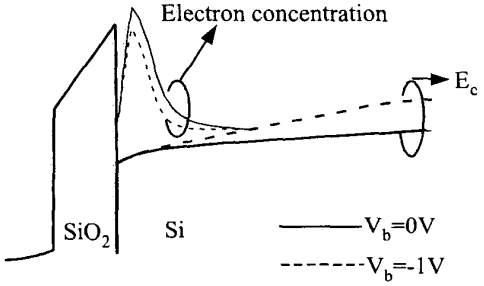


Fig.7 Drain current degradation with different substrate bias in stress, V_b=0.5V, 0V and −1V. (a) t_{ox}=20Å and stress V_d=2.5V. (b) t_{ox}=33Å and stress V_d=3.0V.



(a)



(b)

Fig.9(a) Simulated lateral field distributions along the channel. V_d=2.5V, V_g=3.4V, V_b=0V and −1V. The source junction is at x=0.0μm. (b) Simulated conduction band-edge diagram and electron concentration distribution in the vertical direction from coupled 1D Poisson equation and Schrodinger equation. The centroid of the electron distribution is closer to the Si surface at V_b=-1V.