Edge Hole Direct Tunneling in Off-State Ultrathin Gate Oxide p-Channel MOSFETs

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Abstract

This paper examines the edge direct tunneling (EDT) of hole from p^+ polysilicon to underlying p-type drain extension in off-state p-channel MOSFETs having ultrathin gate oxide thicknesses (1.2 – 2.2 nm). It is found that for thinner oxide thicknesses, hole EDT is more pronounced over the conventional GIDL and gate-to-channel tunneling, and as a result, the induced gate and drain leakage is better measured per unit gate width. A physical model accounting for heavy and light hole's subbands in the quantized accumulation polysilicon surface is built explicitly. This model consistently reproduces EDT I-V and the tunneling path size extracted falls adequately within the gate-to-drain overlap region. The ultimate oxide thickness limit due to EDT is projected as well.

Introduction

The scaled gate oxide thickness is now approaching the direct tunneling regime [1]. The gate leakage due to direct tunneling [2] was usually measured *per unit oxide area* [3],[4], and a certain criterion of 1 A/cm^2 set the ultimate limit of scalable oxide thicknesses [3],[4]. For n-channel devices operated in off state, the edge direct tunneling (EDT) [5],[6] of electron from n^+ polysilicon to underlying drain extension not only dominates the gate leakage, but also can prevail over the conventional GIDL. This paper explores straightforward the EDT of hole from p^+ polysilicon to p-type drain extension in p-channel counterpart. It is clarified that the induced gate and drain leakage indeed originates from the edge part rather than the whole gate oxide, and thus is better measured *per unit gate width*. Also presented is a physical model enabling consistently the reproduction of EDT I-V, the extraction of EDT path size, and the projection of ultimate oxide thickness.

Experiment and Characterization

Test patterns including p^+ poly-gate p-channel MOSFETs and CMOS inverters were fabricated by a 0.18-um process technology [7]. The gate oxides were grown in diluted wet oxygen ambient to three different physical thicknesses T_{ox} of 1.23, 1.85, and 2.16 nm. These values for p-channel devices were extracted by citing an electron direct tunneling I-V model [8] and were all confirmed by high resolution TEM and a C-V method accounting for polysilicon depletion and Quantum Mechanical effects, as detailed elsewhere [9]. Fig. 1 illustrates three plausible tunneling leakage paths for off-state p-channel MOSFETs and related band diagrams.

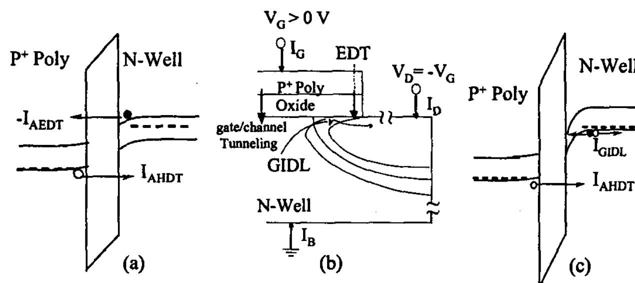
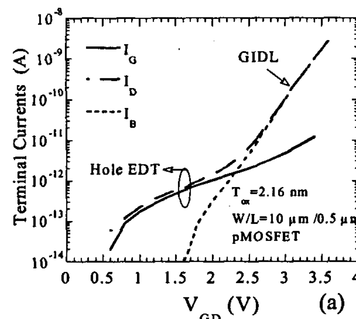


Fig. 1 (a) Band diagram located at channel region far from LDD. Accumulation hole direct tunneling current (I_{AHDT}) and electron direct tunneling (I_{AEDT}) both contribute to gate/channel tunneling. (b) Schematic cross section near gate/drain overlap region under V_G>0 V and V_D= -V_G. Three tunneling current paths are shown. (c) Band diagram located at gate/drain overlap region, showing hole EDT and GIDL.

With source open and under V_D = -V_G, the measured drain current I_D, gate current I_G, and bulk current I_B are plotted in Fig. 2 versus V_{GD} for three different oxide thicknesses. Fig. 2(a) and (b) reveal that the drain current primarily comprises the GIDL and the gate current, favoring EDT as the origin of the latter component. It is seen that a certain range of V_{GD} exists where the EDT prevails over the GIDL, and such range is expanded for decreased T_{ox}. We attribute the EDT herein via hole rather than valence electron tunneling. This can be evidenced based on the band diagram in Fig. 1 that for low voltage V_{GD} it is essentially improbable for valence electron tunneling across the oxide to the forbidden gap in polysilicon side. In Fig. 2(c) for T_{ox} = 1.23 nm, the gate-to-channel tunneling constitutes solely the bulk current making GIDL impossible to detect. Note that hole EDT dominates the gate current for all T_{ox}.



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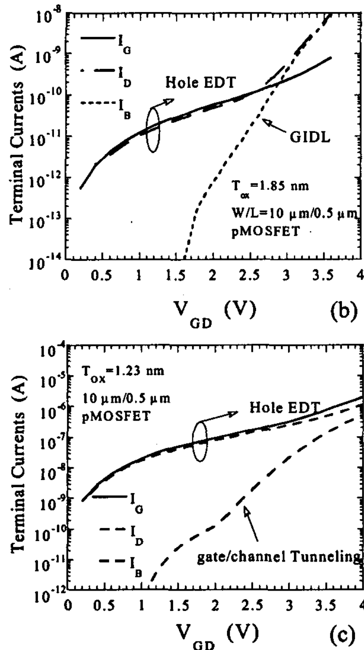
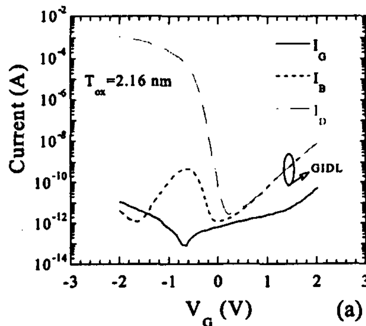


Fig.2 Measured terminal currents versus V_{GD} for three different T_{OX} (a), (b), and (c) under V_D= -V_G and source open. The aspect ratio W/L=10 μm/0.5 μm. (a) Hole EDT dominates the drain leakage I_D in 0 V<V_{GD}<2.3 V. (b) Hole EDT dominates I_D in 0 V<V_{GD}<2.6 V and GIDL constitutes drain leakage for V_{GD}>2.6 V. (c) The edge tunneling mechanism prevails over almost the drain leakage current.

With source grounded and V_D =-1.8 V, the measured terminal currents versus both polarities of V_G are plotted in Fig. 3. Obviously, the GIDL dominates the drain leakage for T_{ox} = 2.16 nm, while for thinner T_{ox} of 1.85 nm such role is replaced by hole EDT in 0 V < V_G < 0.9 V, and eventually is entirely controlled by hole EDT for T_{ox} = 1.23 nm. Fig. 3(c) shows the bulk current reversal phenomena due to two opposite sources: GIDL and gate-to-channel tunneling. Regarding on-state I-V (negative V_G) in Fig. 3, the impact of hole direct tunneling from the inverted channel in degrading drive capability is described in our recent work [9].



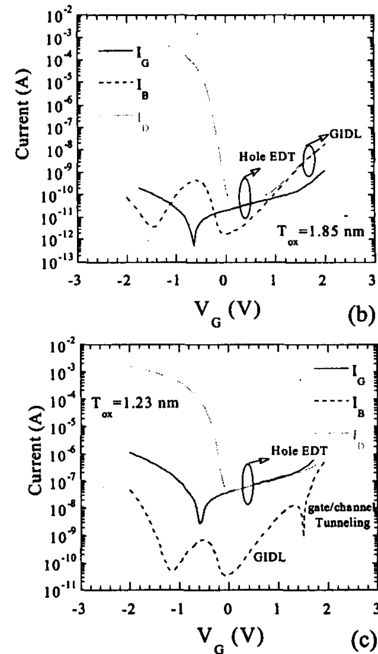
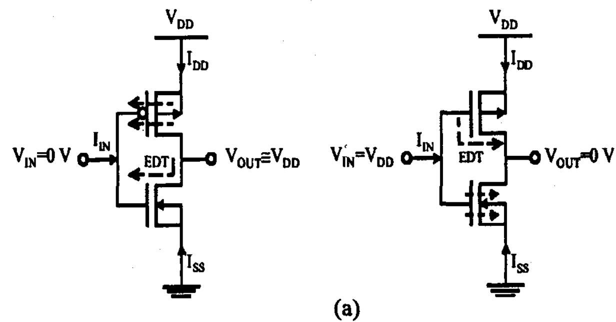


Fig. 3 Measured terminal current versus both polarities of gate voltage. The aspect ratio W/L=10 μm/0.5 μm. Source grounded and V_D=1.8 V.

We also found experimentally that the hole EDT leakage is indeed proportional to the gate width, regardless of the aspect ratio (W/L). This means that the induced gate and drain leakage is better measured per unit gate width. Fig. 4 displays the supply current and input current all versus input voltage V_{in} measured on CMOS inverter with T_{ox} = 1.23 nm for different supply voltage V_{DD}. It can be observed that (i) at high-level state V_{in} = V_{DD}, the standby current comes from the hole EDT of off-state p-channel device and the electron direct tunneling from inverted channel in turn-on n-channel one; and (ii) at low-level state V_{in} = 0, the standby current comprises the electron EDT [5],[6] of off-state n-channel and the hole direct tunneling from inverted channel in on-state p-channel [9]. *Attached in Fig. 4 is the measured ratio of each component. It is expected that as channel length continues to shrink, the role of EDT substantially increases since source/drain extension does not easily scale* [5],[11].



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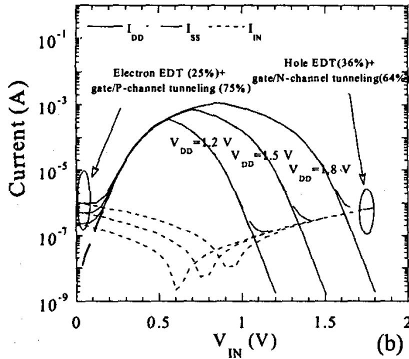


Fig. 4 (a) Measurement set-up for two standby modes and (b) measured supply currents, I_{DD} and I_{SS}, and input current, I_{IN}, versus input voltage V_{IN} from an inverter with T_{OX}=1.23 nm for different supply voltage V_{DD}. Gate leakage paths in two standby modes are shown. The gate length is 0.18 μm.

Hole EDT Modeling

By following a published analytic electron direct tunneling model [8], a hole EDT version was built:

$$I_{EDT} = A_o Q f T = L_{TP} W Q f T$$

where A_o(=L_{TP} ×W) is the effective tunneling path cross-section area; L_{TP} is the tunneling path size; Q is sheet charge of the accumulation layer; f is hole impact frequency on the p^+-poly/SiO_2 interface; and T is the modified WKB transmission probability including interface reflection correction. The oxide field E_{ox} at the gate edge is one key input parameter to the model.

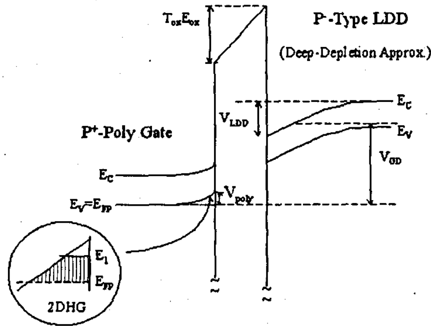


Fig. 5 Band diagram drawn along P^+-Polysilicon/Oxide/LDD. The accumulation potential bending, V_{POLY}, with 2DHG(2-Dimensional Hole Gas) Concept and the silicon surface potential, V_{LDD}, with the deep depletion approximation are adopted in the procedure of E_{OX} extraction.

Applying the first subband approximation to the accumulated p^+ poly gate and the deep depletion approximation to the underlying LDD region as shown in Fig. 5, we can get a simplified form to facilitate the extraction of E_{ox} as shown below:

Triangular - Potential Approximation

$$E_{H,1} = \frac{(3\pi \hbar q m_{H,\perp})^{2/3}}{2m_{H,\perp}} (\frac{\varepsilon_{ox} E_{ox}}{\varepsilon_{si}})^{2/3} \ , \ E_{L,1} = \frac{(3\pi \hbar q m_{L,\perp})^{2/3}}{2m_{L,\perp}} (\frac{\varepsilon_{ox} E_{ox}}{\varepsilon_{si}})^{2/3} \ ,$$

$$g_{2D,L} = \frac{m_{L,\parallel}}{\pi \hbar^2} \ , \ g_{2D,H} = \frac{m_{H,\parallel}}{\pi \hbar^2}$$

First - Subband Approximation

$$\varepsilon_{ox} E_{ox} = [g_{2D,H}(E_F - E_{H,1}) + g_{2D,L}(E_F - E_{L,1})] q \ ,$$

$$E_F = \frac{\varepsilon_{ox}}{q(g_{2D,H} + g_{2D,L})} E_{ox} + \frac{g_{2D,H} E_{H,1} + g_{2D,L} E_{L,1}}{g_{2D,H} + g_{2D,L}}$$

$$V_p \approx \frac{E_F}{q} = \frac{\varepsilon_{ox}}{q^2 (g_{2D,H} + g_{2D,L})} E_{ox} + \frac{g_{2D,H} E_{H,1} + g_{2D,L} E_{L,1}}{q (g_{2D,H} + g_{2D,L})} \ ,$$

Deep - Depletion Approximation

$$V_{LDD} = \frac{\varepsilon_{ox}^2 E_{ox}^2}{2 q \varepsilon_{Si} N_{LDD}}$$

$$V_{GD} - V_{FB} (\approx 0) = V_{ox} + V_{LDD} + V_{POLY}$$

$$= T_{ox} E_{ox} + \frac{\varepsilon_{ox}^2 E_{ox}^2}{2 q \varepsilon_{Si} N_{LDD}} + \frac{\varepsilon_{ox}}{q^2 (g_{2D,H} + g_{2D,L})} E_{ox} + \frac{g_{2D,H} E_{H,1} + g_{2D,L} E_{L,1}}{q (g_{2D,H} + g_{2D,L})}$$

$$= a_1 E_{ox} + a_2 E_{ox}^2 + a_3 E_{ox}^{2/3}$$

$$a_1 = T_{ox} + \frac{\varepsilon_{ox}}{q^2 (g_{2D,H} + g_{2D,L})} , a_2 = \frac{\varepsilon_{ox}^2}{2 q \varepsilon_{Si} N_{LDD}}$$

$$a_3 = \frac{1}{q (g_{2D,H} + g_{2D,L})} [g_{2D,H} \frac{(3\pi \hbar q m_{H,\perp})^{2/3}}{2m_{H,\perp}} (\frac{\varepsilon_{ox}}{\varepsilon_{si}})^{2/3} + g_{2D,L} \frac{(3\pi \hbar q m_{L,\perp})^{2/3}}{2m_{L,\perp}} (\frac{\varepsilon_{ox}}{\varepsilon_{si}})^{2/3}]$$

Note that the index H means heavy hole and L means light hole. g_{2D} represents two dimensional density of state and E_1 means the ground energy of triangle-like potential. For <100> poly grain orientation, $m_{H,\perp}$=0.29 m_o, $m_{H,\parallel}$=0.433 m_o; $m_{L,\perp}$=0.20 m_o, $m_{L,\parallel}$=0.169 m_o as all cited in [10].

Once E_{ox} was quantified, an excellent reproduction was achieved with LDD dopant N_{LDD}=8x10^18 1/cm^3 and effective mass m_{oxh} =0.38 m_o for both heavy and light hole resulting from parabolic dispersion relation in tunneling oxide, as depicted in Fig. 6. The tunneling path size extracted was 6 nm wide (=L_{TP}) from the gate edge (since N_{LDD} quite matches the highly-doped one). This is reasonable since the drain extension beneath the gate is about 8 nm.

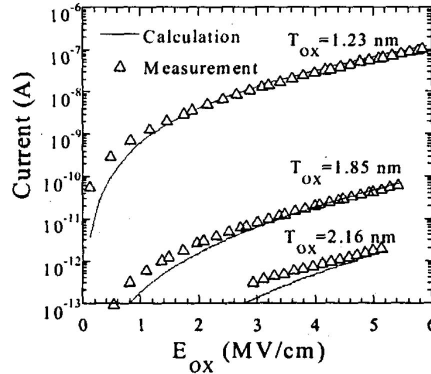


Fig. 6 Comparison of the calculated and experimental hole EDT current versus E_{OX}. The extracted effective EDT range is 6 nm wide from the gate edge. W=10 μm.

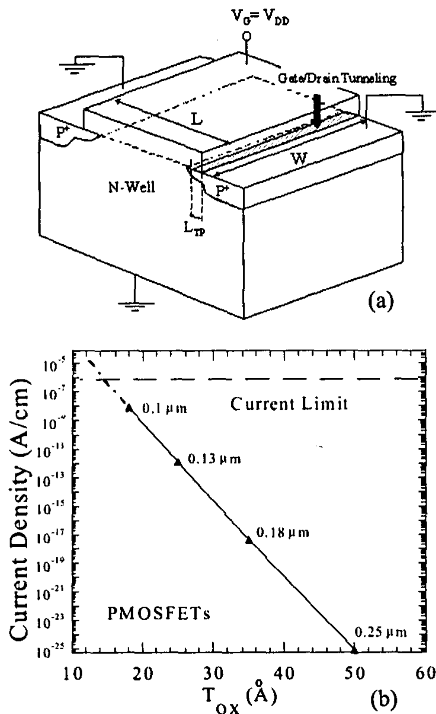
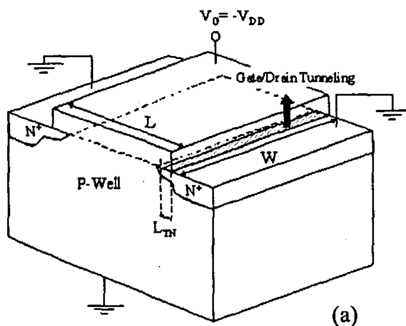


Fig. 7 (a) Showing the location of the edge hole direct tunneling. (b) The calculated hole direct tunneling per gate width versus scaling generation oxide thickness in PMOSFETs.

Table. 1 Showing the scaling parameters from [1].

Feature Size (μm)	V_{DD} (V)	T_{OX} (nm)
0.25	2.5	5.0
0.18	1.8	3.5
0.13	1.5	2.5
0.10	1.2	1.8

It is recognized [5],[11] that drain extension may be considered a non-scalable factor, implying a constant L_{TP} of 6 nm in the scaling direction.



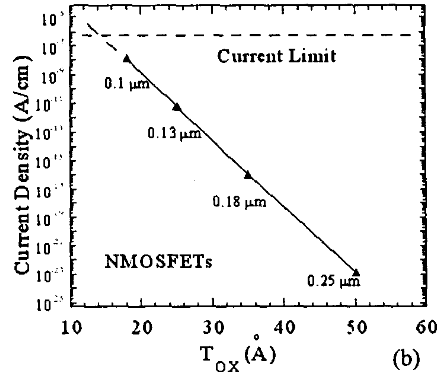


Fig. 8 (a) Showing the location of the edge electron direct tunneling in NMOSFETs. (b) The calculated electron direct tunneling per gate width versus scaling generation oxide thickness. Effective tunneling path is 6.25 nm wide from the gate edge [6].

With this in mind, the conventional criterion of 1 A/cm^2 can be transferred to 0.6 μA/cm. Using the roadmap parameters [1], the hole EDT current is calculated versus scaling generation oxide thickness as shown in Fig. 7. In Fig. 7 the new criterion due to hole EDT sets the ultimate oxide thickness of around 1.42 nm. Similarly, the electron EDT current for off-state n-channel device is calculated [6] versus scaling generation oxide thickness as shown in Fig. 8 for reference. The tunneling path size extracted was 6.25 nm wide from the gate edge [6].

Conclusion

The edge direct tunneling (EDT) of hole from p$^+$ polysilicon to underlying p-type drain extension has shown its tremendous impact on the drain leakage and gate leakage. A physical model has been built and has reproduced consistently experimental EDT I-V characteristics. The tunneling area extracted has been found to fall within the gate-to-drain overlap region. The ultimate oxide thickness due to hole EDT has also been projected based on the model.

Acknowledgment

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References

[1] International Technology Roadmap for Semiconductors, 1999 Edition.
[2] H. S. Momose et al., *IEEE Trans. Electron Devices*, vol. 43, p.1233, 1996.
[3] S. H. Lo et al., *IEEE Electron Device Lett.*, vol. 18, p.209, 1997.
[4] G. Timp et al., *IEDM Tech. Dig.*, p. 615, 1998.
[5] N. Yang et al., *IEDM Tech. Dig.*, p. 453, 1999.
[6] K. N. Yang et al., *SSDM*, 2000 (accepted).
[7] C. H. Diaz et al., *Dig. Symp. VLSI Technol.*, p. 11, 1999.
[8] L. F. Register et al., *Appl. Phys. Lett.*, vol. 74, p. 457, 1999.
[9] K. N. Yang et al., *IEEE Trans. Electron Devices*, 2000 (accepted).
[10] S. Takagi et al., *IEEE Trans. Electron Devices*, vol. 46, p.1446, 1999.
[11] S. Thompson et al., *Dig. Symp. VLSI Technol.*, p.132, 1998.