Real-time Process Control to Prevent CD Variation Induced by Post Exposure Delay

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ABSTRACT

One of the major problems for DUV resists is linewidth change owing to Post Exposure Delay (PED). Linewidth is mainly induced by acid diffusion during exposure and baking. Based on the mechanism of the neutralization of organic base and photogenerated acid, a model had been generated in our previous study to describe the linewidth variation for different PED times. The derived equation can calculate the minimum elapse time, which will cause linewidth variation to exceed the specification of a specific CD. This work concludes that the smaller CD received a higher percentage of CD variation under PED for an isolated line pattern. Therefore, the minimum acceptable time for the smallest CD can be obtained based on ± 10% of the nominal CD.

When a track alarm occurs and wafer processing stops, wafers between exposure and post exposure bake (PEB) will suffer a CD variation due to PED. The start and end time of each processing wafer is traced herein, and the time interval between one end time and the following start time is calculated via an automatic control system. If the time interval exceeds the value set herein, an automatic control system will hold this lot and send an error message to the engineer. Based on the in-line configuration of stepper and track, seven wafers must be reworked when PED occurs. By employing the model and automatic control system established herein, linewidth variation induced by PED can be prevented.

Keywords: Real-time process control, Post Exposure Delay (PED), CD DUV

1. INTRODUCTION

Chemically amplified resists suffer inherent problems with process stability. The time between exposure and post exposure bake (PEB) has proved to be the most critical parameter for linewidth variation. The linewidth change is mainly induced by acid diffusion during post exposure delay (PED). Significant effort has been devoted to understanding the role of each component of resist formation on lithographic performance, aiming to enhance process stability and resist performance.[1-10] Thus, the diffusion behavior of photogenerated acid has been widely investigated for both high and low activation energy (*Ea*) resist systems.[6-15] Base additives can reduce the linewidth slimming of low *Ea* systems such as acetal-based resists by reducing the acid diffusion.[5, 14]

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Furthermore, additional base components can not only quench photogenerated acid, but can also suppress the acid diffusion reaction within the resist film.[6]

Our previous study examined how an organic base additive influences the acid concentration and lithographic performance in a t-BOC protected type chemically amplified positive DUV resist.[16] The resists included a t-BOC protected polystyrene base resin (substitution ratio approximately 25%) and an onium salt as a photoacid generator. A resist system composed of a chemically amplified positive resist and an organic base, such as NMP, not only prevents formation of a 'T-top', but also suppresses the acid diffusion reaction within the resist film.[6] The linewidth broadens immediately after exposure and then became a constant value rather than continuously expanding. A model was established to represent the linewidth variation behavior based on the organic base neutralization method. An equation was also derived to clarify the linewidth broadening behavior during PED for various pattern sizes.

To obtain a high yield product suitable for mass production, maintaining a stable critical dimension (CD) is one of the key parameters. This work proposes a new idea to prevent the CD variation induced by PED. Based on the previously established model and equation, the different linewidth variations for various PED times are easily obtained. The maximum number of wafers affected by PED can be obtained by analyzing in-line stepper and track configuration. By employing automated control, every batch report generated after the batch is completed is analyzed. Through automated control, any abnormal lots will be 'held'. Engineers can easily deal with the abnormal lot by checking the "hold reason" generated by automation control. This automation control can prevent CD variation caused by Post Exposure Delay.

2. STRATEGY FOR MAINTAINING RELIABLE CD

2.1 Background

The behavior of the linewidth variation caused by PED was examined in our previous investigation.[16] The linewidth broadens immediately after exposure, and becomes a constant value following a long term PED. The following equation can accurately describes the linewidth:

$$CD(t) = CD(0) + S[1 - \exp(-t/\tau)], \qquad (1)$$

The linewidth $CD(t)$ is at its minimum when no PED exists. The linewidth increases with the PED time, and reaches its maximum, $CD(0)+S$, when the PED time approaches infinity. Figure 1 presents the behavior of the linewidth variation of a 0.25 μm line-and-space pattern. The resist cross-section profile was verified to confirm that no "T-top" was formed during PED. To ensure the linewidth remains constant, the linewidth was measured up to twenty-four hours. No clear CD change was observed during the PED, a result also displayed in Fig. 1.

The fitting curve in Fig. 1 is generated based on Eq.(1). Evidently, the simulation result can accurately describe the CD variation during PED. Employing the fitting technique, the value of S and τ can be obtained. The S in Eq.(1) represents the maximum linewidth variation, $CD(\infty) - CD(0)$, for a specific linewidth. Our previous investigation found that the time constant τ remained almost constant (τ around 9 to 10 minutes) for different sizes of dense and isolated patterns. Therefore, the maximum linewidth variation, S, is the only factor influencing the behavior of linewidth change during PED. Figure 2 shows the values of S for dense and isolated patterns. These values are obtained from the fitting results of different resist patterns. Providing the values of S are known, Eq. (1) can accurately predict the behavior of the linewidth variation.

2.2 Strategy

The behavior of linewidth broadening for any linewidth can be predicted when the value S of the linewidth is available. Normally, the acceptable CD variation is ±10% of the target linewidth. If we assume the energy control, image tilt, field curvature, focus drift, and other processes caused errors that account for ±5% of the CD variation, the maximum allowable CD change induced by PED is the remaining 5% of the target linewidth. Using Eq.(1), the maximum allowable PED can be calculated for various patterns. The following is an example for 0.2 μm line-and-space dense patterns. The value of $S_{0.2,dense}$ is 12 nm while the time constant τ is 10 minutes. Hence, the CD variation can be described by:

$$CD(t) = 0.2 + 0.012[1 - \exp(-t_0 / 10)]. \quad (2)$$

Based on the +/-5% CD variation, the maximum allowable time can be obtained by:

$$0.2 \times 5\% = 0.012 \times [1 - \exp(-t_0 / 10)]. \quad (3)$$

$$\exp(-\frac{t_0}{10}) = 1 - \frac{0.2 \times 5\%}{0.012} = 1 - \frac{0.01}{0.012}. \quad (4)$$

$$t_0 = -10 \ln(0.167) = 17.9. \quad (5)$$

Similarly, the maximum allowed PED time for various pattern sizes can be obtained for both dense and isolated patterns. Figures 3(a) and 3(b) display these results. From the previous results, the maximum allowable PED time can be determined based on the most critical linewidth, for example a 0.2 μm isolated line.

After analyzing the maximum allowable PED time, the machine configuration must be examined to determine how many wafers need to be reworked when the track is unexpectedly stopped. Figure 4 displays an in-line configuration of stepper and track. When the process is running an in-line mode, wafers start (and end) at the input (and output) of the wafer track. After coating and baking, wafers are sent directed to the exposure chuck of the stepper through the interface systems of the track and stepper. If an alarm causes the wafer to stop processing, the PED time for those wafers, which are exposed but baked changes. From the previous analysis, it is known that the changed PED will cause linewidth variation. Our previous work had found that the linewidth is not affected by any delay following the PEB process. Therefore, the maximum number of wafers that can be affected by PED can be obtained from the plot of Fig. 4, and this number is seven.

A new approach for preventing PED induced linewidth variation is proposed herein. After completing a batch, the batch report is generated, including extensive information concerning the processed wafers, including processing time, alignment signal strength, leveling conditions, and so on. Figure 5 displays a portion of the batch report. The figure lists the start and end time of each wafer. For this batch, the average wafer process time, which depends on the exposure energy, shot number, image number, and so on, is approximately 1 minute. Meanwhile, the average transfer time, which is the time interval between the start time of a particular wafer and the end time of the previous wafer, is around 9 seconds. If the track has sufficient coaters, developers and hot/cool plates, the stepper is the bottleneck of this process line. Hence, the time interval will become almost constant. From the explanation in section 2.1, the maximum allowable PED time can be determined for a

specific technology (for example, the maximum allowable PED time for a 0.2 μm dense pattern is about 18 minutes). Meanwhile, using the automatic control, the batch report can be obtained for each processing lot. By subtracting the time interval from 9 seconds (which is the transfer time), whether a delay exists during processing can be determined for each wafer. Through the calculation of the automatic control, the user setting a maximum allowable PED time can identify the abnormal wafer. The automatic system can then decide to either hold this lot or hold both the current lot and the previous lot, because the maximum number of affected wafers is seven. Therefore, the automatic system can identify the abnormal wafers, and can generate a reason for holding, such as "PED error, wafer no. 10" or "PED error by next lot (wafer no.3)". This approach allows the engineers to easily deal with any abnormal wafers based on the reason s for holding the abnormal lots.

3. EXPERIMENT

The effect of an additional base component, N-methyl pyrrolidone (NMP), was investigated in tert-butoxycarbonyl (t-BOC) protected chemically amplified positive deep ultraviolet (DUV) resist. The resists included a t-BOC protected polystyrene base resin (substitution ratio approximately 25%) and an onium salt as photoacid generators. The resist samples were coated on hexamethyl disilazane (HMDS) vapor primed silicon substrates. The positive DUV resist was spun-coated to 0.6 μm thickness and pre-baked at 110°C for ninety seconds. All patterns were exposed by a KrF excimer laser scanner with a 0.63 NA lens, and the PEB was performed at 110°C for ninety seconds. Meanwhile, the resist films were developed in a 2.38-wt% tetramethylammonium hydroxide (TMAH) based developer for sixty seconds. A Hitachi S-9200 scanning electron microscope (SEM) was used to measure the resist pattern line widths. Finally, the ammonia concentration was controlled under 8 ppb by mol in the air and under 0.8 ppb by mol inside the track to prevent T-top formation.

4. RESULTS AND DISCUSSION

Figure 6 displays an example of the statistical process control (SPC) CD chart, which is obtained from the production line. The measured CD is a DRAM product dense pattern, with a target of 0.25 μm. Based on the criterion of ±10% CD, the upper and lower limits are 0.275 μm and 0.225 μm, respectively. Meanwhile, the nominal energy is set as 20 mJ/cm^2 to maintain the CD mean value of this pattern close to the target. Normally, only one wafer per lot is measured to maintain the throughput of the SEM. Additionally, the specific wafer slot is pre-determined to measure the CD by the automatic control. In this example, wafer slot 25, which is the first processed wafer in this lot, is measured to represent the linewidth of the lot. During the exposure of lot "T05", a track alarm halted the track movement, and stopped the sending and/or receiving of wafers from the stepper. At that moment, the stepper was exposing the third wafer of this lot. Although the track problem was solved after 15 minutes, the PED effect had already affected the CD and broadened the measured pattern to 0.281 μm. Evidently, increasing the exposure energy can reduce the linewidth owing to light diffraction. Based on the measured CD, the on-duty engineer wrongly concluded that the CD drift might be caused by variation of the deposited film. Therefore, this lot was reworked, and the exposure energy was changed from 20 mJ/cm^2 to 22 mJ/cm^2. After removing the resist film, this lot was processed and measured again. Because of the increasing energy, the CD became 0.22 μm and was still out of specification. Based on the first and second results, the energy 21 mJ/cm^2 was given for the third time process. Unfortunately, this lot encountered a track alarm, and broadened the linewidth. Because the exposure energy is 1 mJ/cm^2 higher than the nominal energy, the average CD is 0.272 μm, which was within the specification. Normally, five or nine measurements, distributed among different exposure shots, are required to collect sufficient shot-to-shot CD information. Although the third time average CD is still smaller than the upper limit, some measurement results were out of spec. Based on the trial-and-error

process of lot "T05", the PED problem was discovered from the batch report. By knowing the root cause of CD variation, this lot was reworked and given a nominal energy for the fourth run. Eventually, the average CD reached 0.257 μm, close to the target line displayed in Fig. 6.

After the event of lot "T05", a new means of monitoring the running process was proposed, using automatic control. Based on the generated batch report of each process lot, the influence of PED on linewidth variation can be prevented, because the abnormal wafer will be sent to be reworked before it is measured by SEM. Simultaneously, those wafers that will not be measured by SEM can still be identified by the automatic control to prevent yield loss caused by CD broadening.

5. CONCLUSION

The model established previously can accurately predict the linewidth broadening cause by PED time. By setting the tolerated CD variation, such as 5% or 10% of target CD, the maximum allowable PED can be determined based on different technological requirements. Through automatic control, any PED occurrence can be detected and quantified based on the batch report. Meanwhile, each abnormal wafer caused by PED can be sent for reworking before measuring by SEM to obtain a reliable SPC chart. Additionally, wafers that will not be measured by SEM can still be detected to prevent a yield loss. Therefore, the automatic system can perform real time process control to prevent PED induced CD variation.

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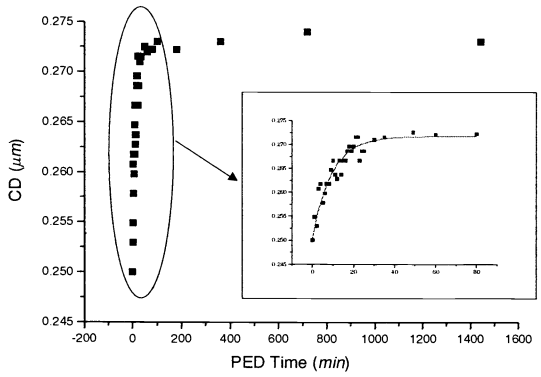

Fig. 1 CD variation for 0.25 μm line-and-space patterns.

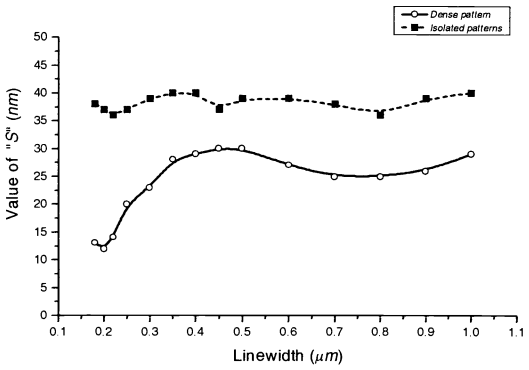

Fig. 2 Maximum linewidth variation S of dense and isolated patterns.

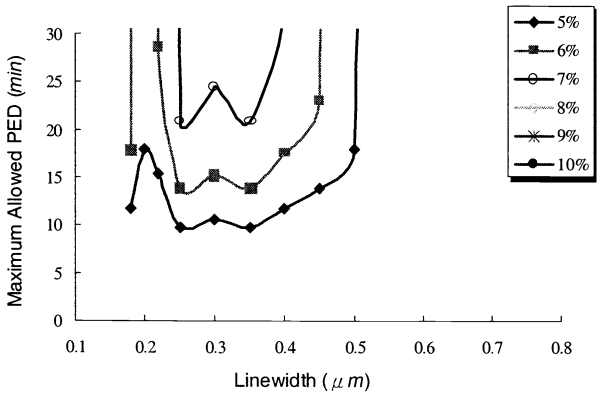

Fig. 3(a)

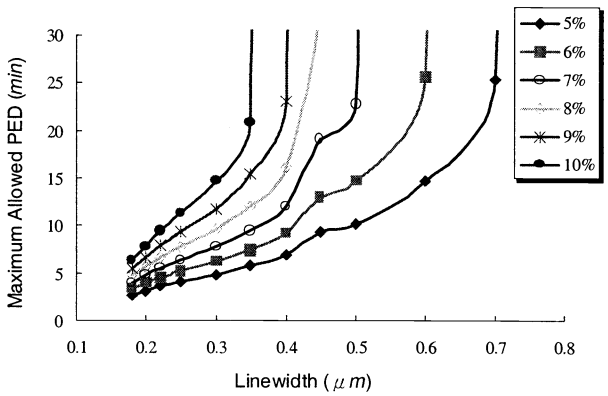

Fig. 3(b)

Fig. 3 Maximum allowable PED time for different percentage of CD variation
(a) dense patterns (b) isolated pattern

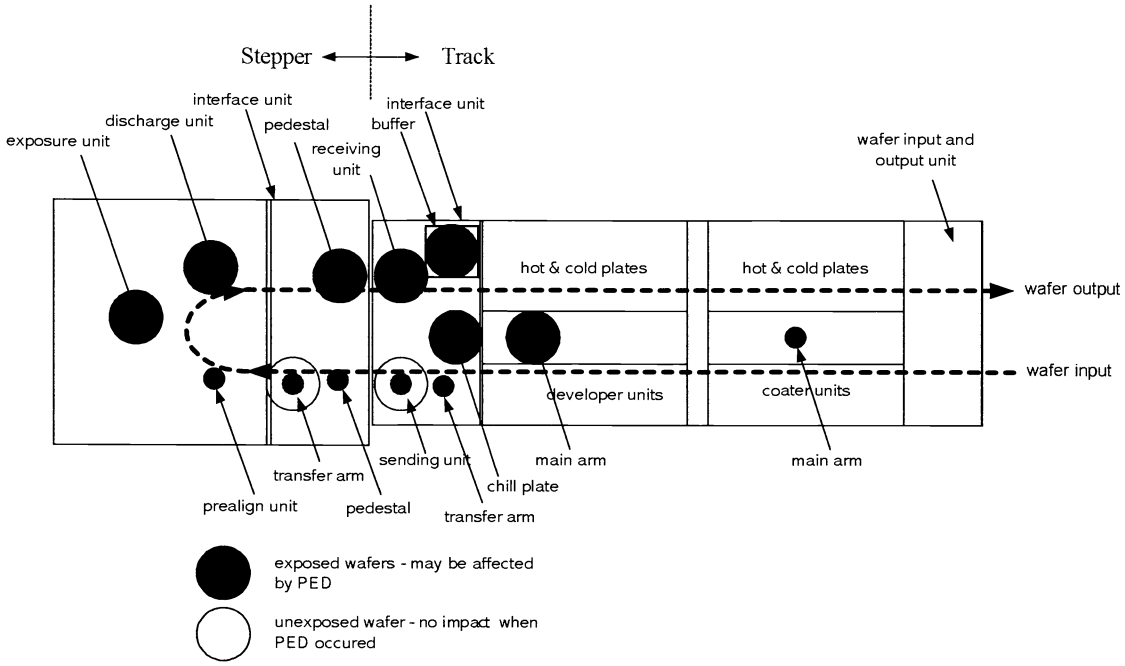

Fig. 4 In-line configuration of stepper and track

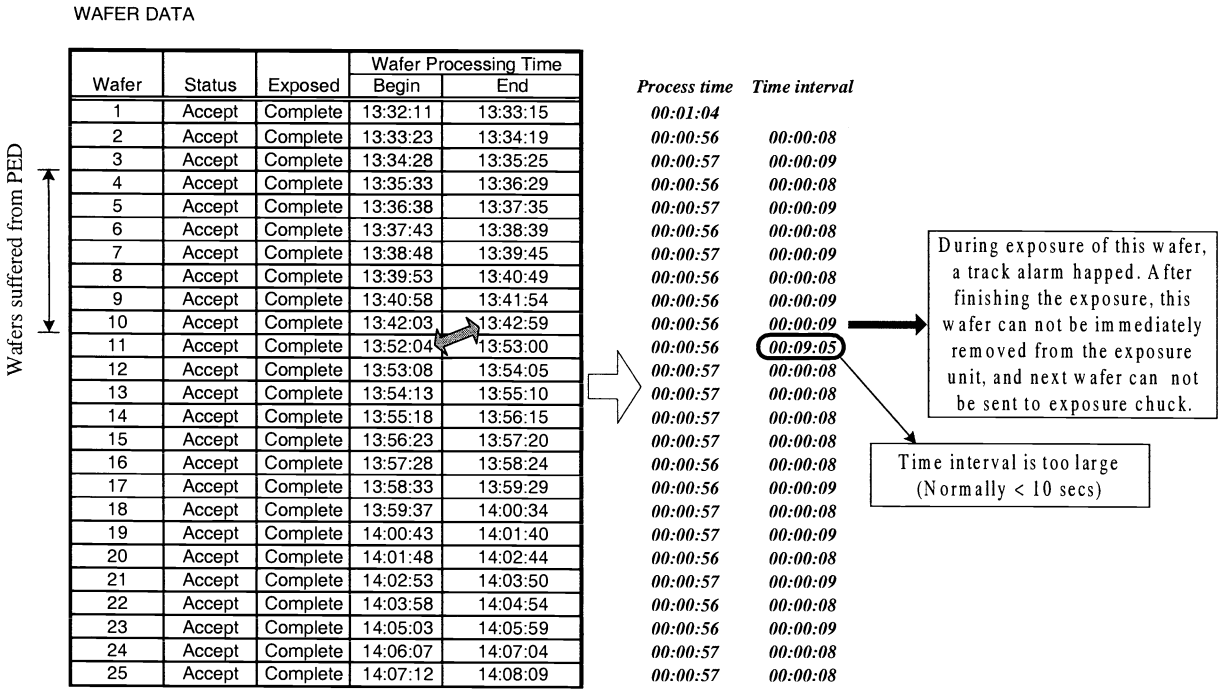

Fig. 5 Portion of the batch report

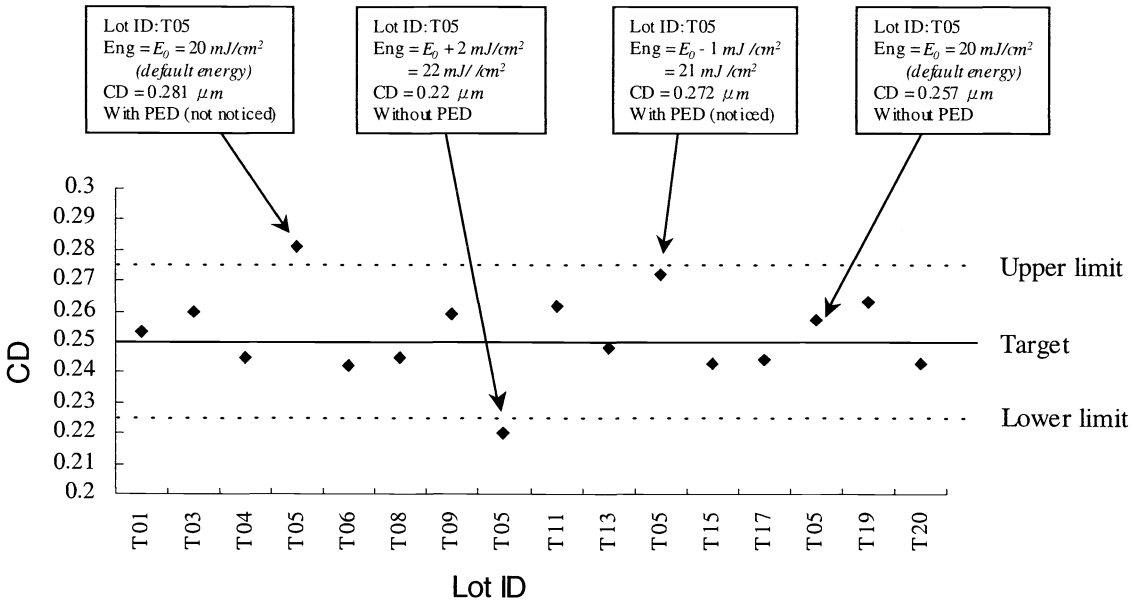

Fig. 6 CD SPC chart which is affected by PED