Plasma Process Induced Damage in Sputtered TiN Metal Gate Capacitors with Ultra-Thin Nitrided Oxide

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ABSTRACT

A comprehensive study on plasma process induced damage (P2ID) in sputtered TiN metal-gated devices with 4nm N_2O-nitrided oxide was performed. It is observed that the post-deposition RTA temperature affects both the flat-band voltage (Vfb) and interface state density (Dit). The TiN metal-gated devices also show a 8 Å reduction in the effective oxide thickness, due to physical damage caused by sputtering and/or oxide consumption during the post annealing step. Finally, degradation in gate oxide integrity caused by severe charging damage during the additional plasma processes in the TiN metal gate process flow is also observed. The P2ID leads to significant degradation in charge-to-breakdown and gate leakage current increase, even for the genuinely robust nitrided oxide used in this study. Finally, N_2 plasma post-treatment is found to be effective in suppressing the gate leakage current.

INTRODUCTION

As CMOS technology scales toward sub-0.1 μm regime, the poly gate depletion effect, caused by insufficient dopant activation near the poly/SiO_2 interface, becomes increasingly non-tolerable. Due to the voltage drop across the poly depletion layer, an effectively lower surface electric field causes a significant inversion capacitance degradation, which in turn reduces the device driving capability [1]. This undesirable effect becomes even more severe for advanced devices accompanied by lower thermal budget. To overcome this problem, the replacement of conventional poly-Si gate by refractory metals, such as TiN or WN, has recently been proposed [2]~[5]. By employing the metal gate, the gate depletion problem can theoretically be completely eliminated.

However, the use of metal gate itself could create many new issues such as process compatibility, metal penetration, threshold voltage variation and adjustment, etc. In this work, a comprehensive study on the plasma process induced damage in sputtered TiN metal gate capacitors with 4nm N_2O-nitrided oxide was performed. It is observed that the effective oxide thickness extracted from C-V measurement could be reduced by as much as 8 Å for the metal gate splits, which is probably due to sputter damage and/or oxide reaction with metal during high temperature annealing. Moreover, it is also observed that charging damage due to the additional plasma processes in metal gate process flow could severely degrade the resultant oxide integrity. A post-metal plasma treatment is studied to suppress the gate leakage current.

EXPERIMENTAL

MOS capacitors with sputtered TiN gate electrode were fabricated on p-type Si wafers. Capacitors with the conventional n^+ poly-Si gate were also processed to serve as the control. The key process flow and the experimental splits are illustrated in Fig. 1. Briefly, a 4nm-thick nitrided oxide was thermally grown in a dry N_2O/N_2 furnace ambient at 900 ℃, followed by the deposition of gate materials. A 200nm-thick TiN film deposited by the reactive ion sputtering with Ar and N_2 gas mixture was used for the metal-gate devices, while the control split received the conventional n^+ poly-Si gate. This was followed by gate patterning and definition. For the split with TiN gate, the TiN layer was etched in a Cl_2-based helicon-type plasma etcher, followed by photoresist stripping in a down-stream O_2 plasma asher. After gate definition, the metal-gate devices were further split to receive rapid thermal annealing (RTA) at three temperatures (i.e., 500 ℃, 600 ℃, 700 ℃) for 30 sec. While the poly-gate control devices received a standard RTA at 1050 ℃ for 30 sec. Afterwards, a 550 nm-thick interlayer dielectric was deposited by LPTEOS and PETEOS for poly-gate and metal-gate devices, respectively. Contact holes and metal pads with various antenna area ratios (AAR) were subsequently formed. Finally, a forming gas annealing at 400 ℃ was performed. Some of the TiN-gated devices received an additional plasma post-treatment in N_2, NO_2, or NH_3.

RESULTS AND DISCUSSION

I. Basic characteristics of devices with TiN metal gate

Figure 2 shows the quasi-static C-V characteristics of TiN metal gate and n^+ poly gate devices. While the metal gate device is immune to gate depletion effect, the poly gate device suffers a 6 % capacitance reduction in inversion region. Additionally, TiN-gated capacitor also shows a higher accumulation capacitance, which corresponds to a 8 Å reduction in the effective oxide thickness, compared to the poly-Si gate counterpart. The oxide thinning effect can be attributed to sputter damage [2] and/or oxide reaction with metal during high temperature annealing. Flat-band voltage (Vfb) of TiN-gated capacitor is different from that of the poly gate capacitor, primarily due to the work-function difference. Vfb is also found to be dependent on post-deposition

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RTA temperature, as shown in Fig. 3. Vfb becomes more negative as RTA temperature increases and the spread becomes larger at higher temperatures. In addition, the mid-gap interface state density (Dit) is also larger (close to 10^{12} cm^{-2}) for devices annealed at 600 and 700 ℃. Such phenomenon is believed to be related to the change in TiN texture and material properties. Figure 4 shows the XRD spectra of TiN films after RTA treatment. For the 700 ℃-annealed sample, co-existence of TiN(111) and TiN(200) is indeed observed. The texture change could lead to flat-band voltage shift and a wider spread, consistent with previous report [5,6]. Sheet resistance (Rsh) of TiN also varies with RTA temperature, as listed in Table I. Rsh decreases as RTA temperature increases, which is ascribed to the grain size increase with temperature, consistent with the AFM observation (data not shown). However, surface roughness is also found to increase with RTA temperature. We have also performed SIMS analysis, and the results (data not shown) indicate that higher RTA temperature leads to more Ti penetration, which could degrade the gate oxide integrity. Stress release during annealing is also a possible reason for the observed Dit increase.

II. Plasma Damage in devices with TiN metal-gate

Due to the incompatibility of metal gate with conventional processing, metal gate devices may receive additional plasma processing steps, compared to the conventional poly gate devices. As illustrated in Fig.1, in addition to the sputter deposition, TiN-gated capacitors received two extra plasma ashing steps (i.e., one after gate definition and the other after contact hole etching) in the down-stream O_2 asher, and an additional plasma deposition step (i.e., PETEOS). As a result, the cumulative plasma charging damage is expected to be more pronounced in metal gate devices. Figure 5 shows gate current versus voltage characteristics of capacitors with both TiN metal gate and the conventional poly gate. Due mainly to the oxide thinning effect, TiN-gated capacitor exhibits more severe leakage characteristics than the poly gate counterpart. It is worthy to note here that we have also fabricated TiN-gated capacitors with pure O_2 gate oxide, and these devices depict significantly worse leakage current characteristics (data not shown) than the metal-gated devices with nitrided oxide. This trend is consistent with our previous observation that the nitrided oxide is genuinely more robust to plasma damage than the pure oxide [7]. However, gate oxide reliability is also found to be degraded for TiN-gated devices even with nitrided oxide, as shown in Fig. 6. Significant charge-to-breakdown (Qbd) degradation is observed for TiN-gated devices, compared to the poly gate controls. This can be attributed to the sputter damage as well as the mechanical stress caused by thermal coefficient difference between TiN layer and the oxide. Such stress can be minimized by process optimization such as reduced TiN thickness, lower RTA temperature, and reduced temperature ramping rate, etc.

Plasma-induced charging damage was analyzed by Qbd and gate leakage current (Ig) measurements on devices with various antenna area ratios (AAR). As shown in Fig. 7, Qbd as a function of cell position for devices with various AAR indicates that severe charging damage occurs at the wafer center, consistent with our previous results on capacitors with conventional poly gate [7]. Moreover, a much more severe damage is observed for TiN-gated devices, since essentially all the devices with AAR of 10 K are broken down already, with the exception of those few which are located at the wafer edge. Fig. 8 further confirms that severe Qbd degradation is induced in TiN-gated devices even with a small AAR. Similar results are also observed for Ig measured at -2 V, as shown in Fig. 9 and Fig. 10. Large gate leakage current is observed for antenna devices located at the wafer center, despite the fact that our previous experience has shown that N_2O-nitrided oxide similar to that used in this study should be genuinely robust to gate leakage current degradation caused by plasma charging [7]. This finding strongly suggests that plasma charging damage will be a major reliability concern for metal gate devices, and a tighter antenna circuit design rule may be necessary for devices employing metal gate. More efforts need to be made to fully understand and minimize the charging damage encountered in metal gate devices.

III. Suppression of plasma damage by plasma annealing

Plasma passivation, which provides a low temperature (below 300 ℃) and highly effective method to anneal out trapping state, has been widely adopted for improving the device reliability in thin film transistor technology grown on glass substrate. In this study, we have also applied plasma treatment in an effort to passivate the excessive trap density of TiN-gated devices, which is almost an order of magnitude larger than that of poly gate devices, as shown previously in Fig. 3. To improve its characteristics, some of the TiN-gated capacitors were further subjected to an additional plasma post-treatment in NH_3, N_2O or N_2 at 250 ℃ for 40 min. This plasma post-treatment was performed after forming gas annealing. Gate leakage current characteristics are depicted in Fig. 11. It can be seen that significant gate leakage current reduction is achieved for devices that received N_2 plasma post-treatment. The leakage current spread is also improved after plasma treatment. However, for devices that received NH_3 plasma treatment, gate current increase is observed. The mechanism responsible for this unexpected degradation is still not clear at this stage, and could presumably be related to the excessive amount of hydrogen incorporation. On the other hand, N_2 plasma treatment is expected to incorporate nitrogen into the gate dielectric. The formation of strong Si-N bonds in place of strained Si-O bonds and weak Si-H bonds enhance the interface hardness, resulting in the suppression of low-level gate current which is dominated by excessive trap-assisted tunneling. Hence, N_2 plasma post-treatment

appears to be an effective method to suppress the gate leakage current for devices employing sputtered TiN metal gate.

CONCLUSION

A comprehensive study on plasma process induced damage in sputtered TiN metal gate devices with 4nm N_2O-nitrided oxide was reported for the first time. An effective oxide thickness reduction by as much as 8 Å was found on the metal-gated devices, due probably to physical damage caused by sputtering and/or oxide reaction with TiN. Moreover, severe charging damage due to additional plasma processing required for metal gate process integration also results in significant charge-to-breakdown degradation and gate leakage increase for the devices with sputtered TiN metal gate, despite the use of the nitrided oxide known to be genuinely robust to plasma charging damage. Finally, an N_2 plasma post-treatment is proposed to effectively suppress the gate leakage current in TiN-gated devices.

ACKNOWLEDGMENT

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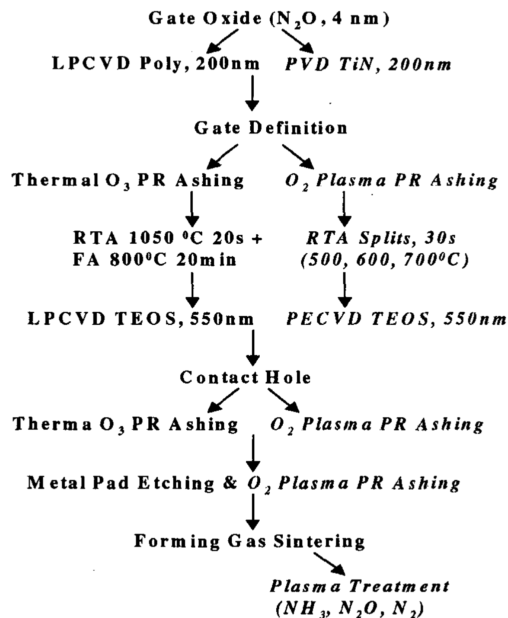

Fig. 1 Key process flow of TiN- and poly-gated devices.

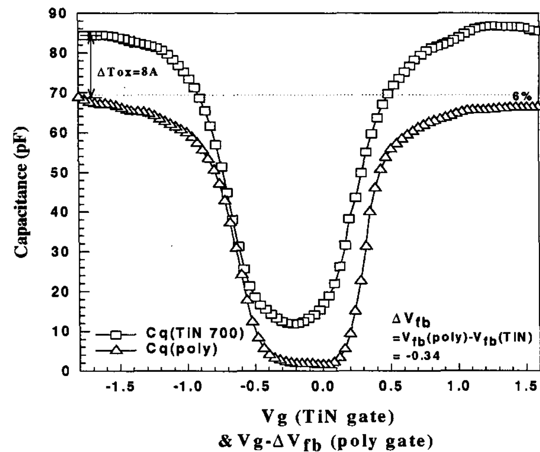

Fig. 2 C-V curves of TiN- and poly-gated devices.

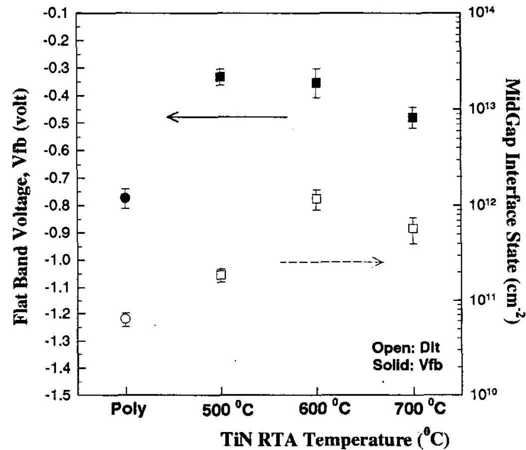

Fig. 3 Flat-band voltages and midgap interface states for TiN-gated devices as a function of RTA temperature.

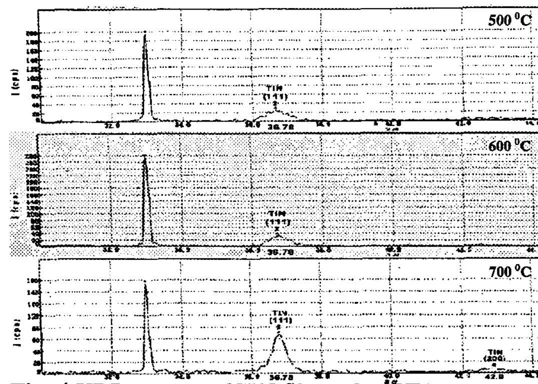

Fig. 4 XRD spectra of TiN films after RTA treatment.

Table I Sheet resistance and surface roughness from AFM of TiN under various RTA temperatures.

	RTA 500 °C	RTA 600 °C	RTA 700 °C
Rsh (Ω/□)	7.4± 0.2	6.5± 0.7	5.9± 0.1
Roughness (nm)	0.295	0.689	0.86

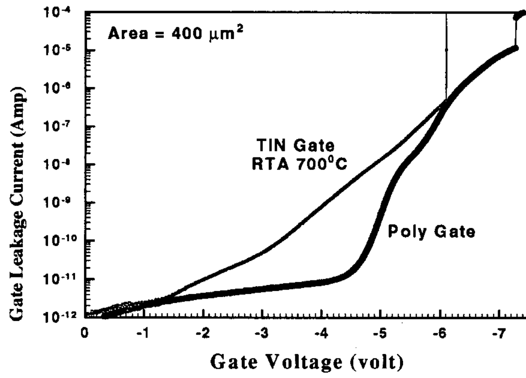

Fig. 5 Gate current characteristics of TiN- and poly-gated devices.

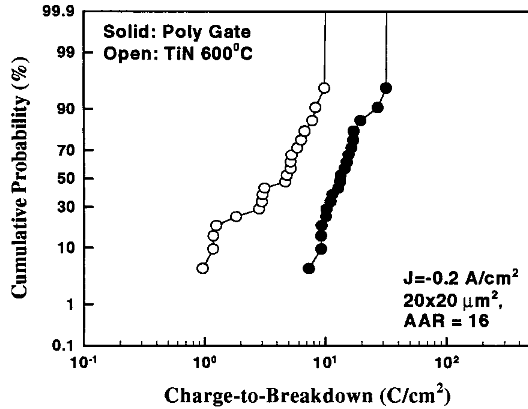

Fig. 6 Cumulative failure of constant current Qbd tests for TiN- and poly-gated devices under gate injection polarity.

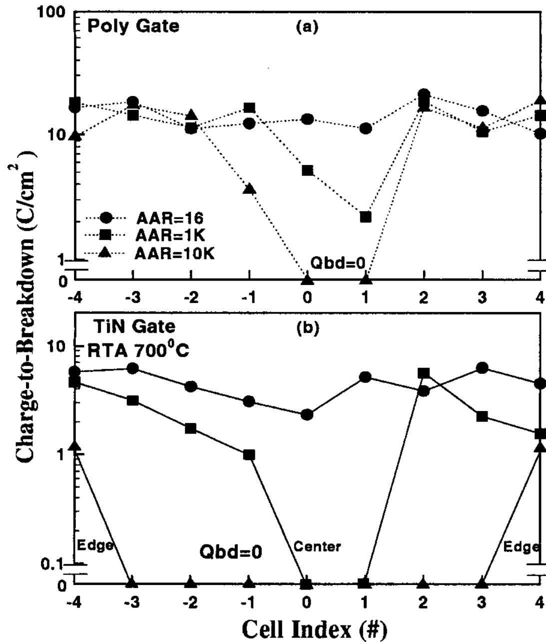

Fig. 7 Qbd characteristics of (a)poly- and (b)TiN-gated antenna devices as a function of cell position from center.

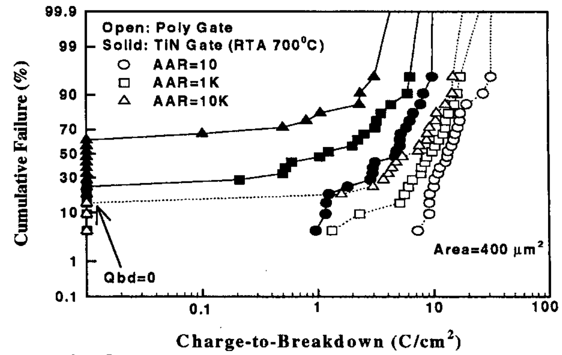

Fig. 8 Cumulative failure of Qbd tests for poly- and TiN-gated devices with various AAR.

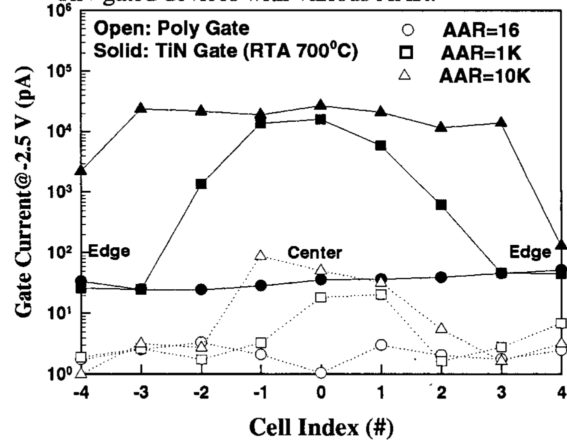

Fig. 9 Ig of poly- and TiN-gated devices with various AAR as a function of cell position.

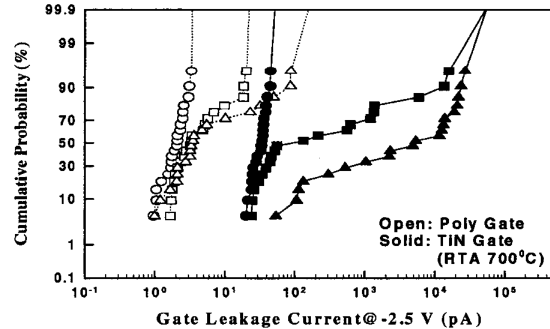

Fig. 10 Cumulative probability of Ig for poly- and TiN-gated devices with various AAR.

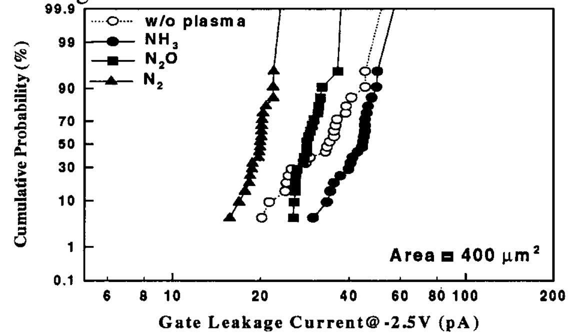

Fig. 11 Ig characteristics after plasma treatments.