Auger Recombination Enhanced Hot Carrier Degradation in nMOSFETs with Positive Substrate Bias

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Abstract

Enhanced hot carrier degradation is observed in DTMOS-like operation mode. This phenomenon is attributed to Auger recombination assisted hot electron process. Measured hot electron gate current and light emission spectrum in nMOSFETs provide evidence that the high-energy tail of channel electrons is increased by the application of a positive substrate bias. As opposed to conventional hot carrier degradation, the Auger enhanced degradation exhibits positive temperature dependence and is more significant at low drain bias.

Introduction

In certain analog and digital circuits, positive substrate bias is applied in nMOSFETs to achieve better performance. For example, improved transistor matching properties and lower flicker noise in analog MOSFETs [1,2] and higher I_{on}/I_{off} ratio in DTMOS [3,4] were reported. The applied substrate bias is sometimes as large as 0.7V [5] or even above [6,7]. The reliability issue of MOSFETs in such bias condition is rarely studied. In this paper, we will report enhanced hot carrier degradation in DTMOS-like operation. The observed degradation cannot be simply explained by conventional channel hot electron theory. Instead, an Auger recombination assisted hot electron energy gain process is proposed. In our model (Fig. 1), holes are injected from positively biased substrate to the channel, which provide for recombination with electrons in the inversion region and give the excess energy to other electrons. The energetic electrons arising from Auger process are then accelerated by channel electric field, thus resulting in a larger hot electron tail than in the standard MOSFET operation condition.

Device Characterization

A four-terminal nMOSFET is used in this work. The device has a gate length of 0.25μm, a gate oxide thickness about 50Å and a gate width of 100μm. Maximum I_b stress around V_g=0.5V_d is performed in DTMOS-like mode (V_b>0) and in the standard mode (V_b=0). Drain current in the triode region is measured to monitor degradation. Temperature and drain bias dependence of the Auger enhanced degradation is characterized.

Results and Discussion

(a) Auger effect enhanced hot electron tail

Hot electron gate current in the standard mode and in DTMOS mode is shown in Fig. 2. The gate current first decreases and then increases with V_b. Hot electron luminescence and emission spectrum are measured to analyze the hot electron distribution (Fig. 3). The light intensity is normalized to the drain current to compensate for the different carrier flux in the channel. Similarly, the emission spectrum shows a turn-around feature as V_b increases from 0V to 0.8V. The reduction of I_g/I_d and I_L/I_d at V_b=0.5V is due to a smaller lateral electric field. At V_b=0.8V, although the lateral field continues to decrease, the Auger recombination rate increases considerably, thus leading to larger I_g/I_d and I_L/I_d. Fig. 4 shows the simulation result of Auger recombination rate and electric field in the channel. Note that hole injection is restricted to the low field region near the source. To further demonstrate the Auger effect on device reliability, the linear drain current degradation at different V_b is measured (Fig. 5). The drain current degradation is increased by an order of magnitude when V_b is from 0V to 0.8V.

(b) Temperature accelerated degradation

The temperature effect on the Auger enhanced degradation is investigated. We compare the temperature dependence of hot electron gate current in the standard mode and in DTMOS mode (Fig. 6). The gate current at V_b=0V has negative temperature dependence due to increased phonon scattering at a higher temperature. This result is consistent with conventional hot electron theory. However, the gate current in DTMOS mode shows reversed I_g-temperature dependence. The reason is that hole injection and Auger recombination rate are enhanced at an elevated temperature. To our knowledge, this is the first time to observe positive temperature dependence of hot electron gate current.

The temperature effect on drain current degradation is shown in Fig. 7. Temperature accelerated degradation is noticed in DTMOS mode. The degradation is enhanced by eight times from T=25C to T=125C. This point is particularly important to device reliability since today's high performance components are required to operate in such temperature range. The substrate bias dependence of drain current degradation is shown in Fig. 8. The measured result shows opposite temperature dependence in the low V_b region and in the high V_b region. The critical V_b for the onset of the Auger enhanced degradation becomes smaller as temperature increases.

(c) Drain bias dependence of degradation

The dependence of the Auger enhanced drain current degradation on stress drain bias is evaluated (Fig. 9). At a relatively large drain bias, the dominant electron energy gain mechanism is field heating. The degradation in DTMOS mode and in the standard mode is therefore about the same. As drain bias reduces, electrons by field heating solely do not have sufficient energy for interface trap creation. The combined Auger recombination and channel field heating process can increase hot electron energy above the threshold for trap creation. Consequently, the Auger enhanced degradation appears to be more significant at low drain voltage in Fig. 9.

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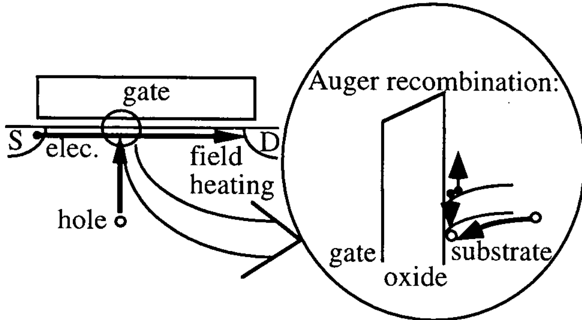

Fig.1. Illustration of Auger recombination assisted hot electron energy gain process in a nMOSFET.

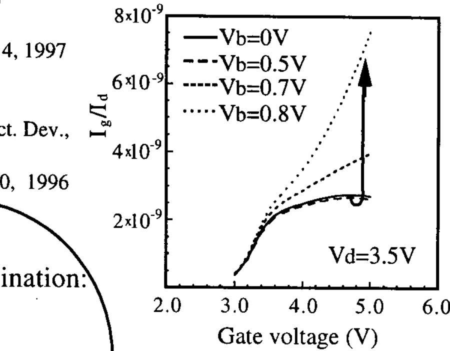

Fig.2. Normalized gate current versus gate voltage with different substrate biases.

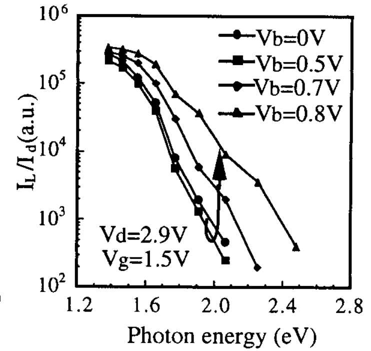

Fig.3. Hot electron light emission spectrum in a nMOSFET with different substrate biases. I_L is the light intensity.

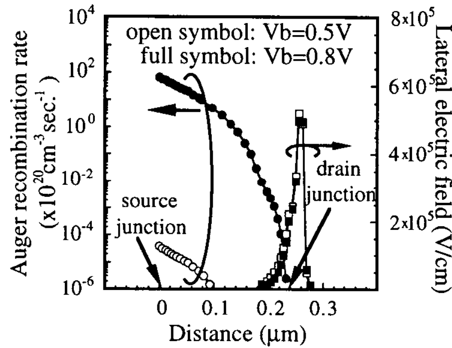

Fig.4. Simulated Auger recombination rate and lateral electric field along the channel. Vd=2.9V and Vg=1.5V.

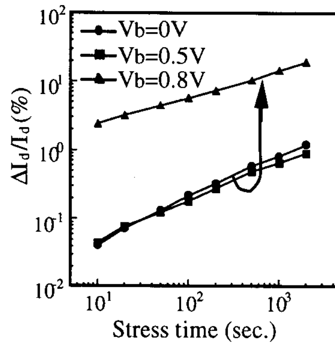

Fig.5. Linear drain current degradation as a function of stress time. Drain current is measured at Vg=2.0V and Vd=0.1V. Stress drain bias is 2.9V and gate bias is 1.5V.

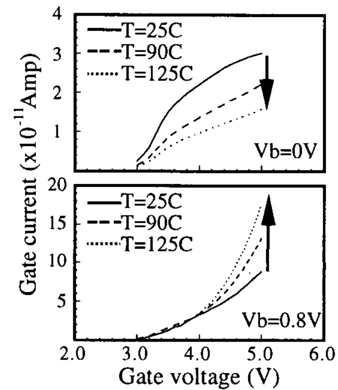

Fig.6. Temperature dependence of gate current at Vb=0V and 0.8V. The drain bias is 3.5V.

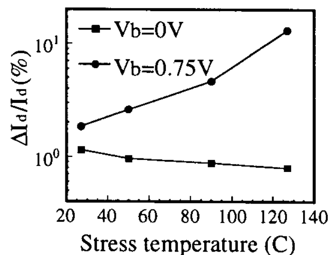

Fig.7. Temperature dependence of linear drain current degradation. Vd=2.9V and Vg=1.5V. The stress time is 2000 sec.

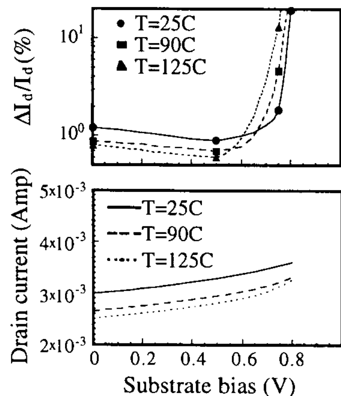

Fig.8. Substrate bias dependence of linear drain current degradation at different stress temperatures. Vd=2.9V and Vg=1.5V. The stress time is 2000 sec. The stress drain current is shown in the lower plot.

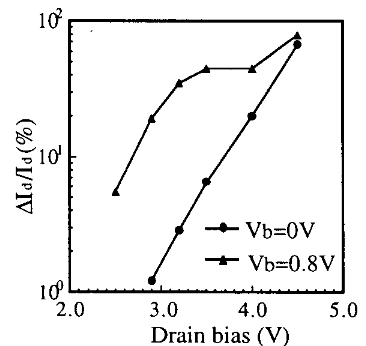

Fig.9. Linear drain current degradation as a function of stress drain bias. The stress time is 2000 sec. T=25C.