Development of Low-temperature Wafer Level Vacuum Packaging for Microsensors

Wei-Feng Huang[a], Jin-Shown Shie[a], Chengkuo Lee*[,b], Shih Chin Gong[b], Cheng-Jien Peng[c]
a. Institute of Electro-Optical Eng., National Chiao Tung University,
1001, Ta Hsueh Rd., Hsinchu, **Taiwan**
b. Metrodyne Microsystem Corp., 1F, No.12, Prosperity Rd. II,
Science-Based Industrial Park, Hsinchu, **Taiwan**
c. MRL, Industrial Technology Research Institute, Hsinchu, **Taiwan**

ABSTRACT

Wafer level packaging received lots of attention in microsystems recently. Because it shows the potential to reduce the packaging cost, while the yield of devices after dicing and packaging can be increased. However, there is a limitation of commercialized wafer bonding technology, i.e., the high process temperature, such as 1000°C of silicon fusion bonding, and 450°C of anodic bonding. A novel low temperature wafer bonding with process temperature lower than 160°C is proposed, it applies the In-Sn alloy to form the interface of wafer bonding. The experiment results show helium leak test of $6x10^{-9}$torr-liter/sec, and a tensile strength as high as 200kg/cm^2. Reliability test after 1500 temperature cycles between -10 to 80°C also shows no trace of degradation compared to the initial quality of the samples. This low temperature soldering process demonstrates its promising potential at the wafer level packaging in industrial production.

Keywords: Wafer Bonding, Soldering, Sealing, Package, Microsensors

1.INTRODUCTION

Silicon wafer bonding process has been developed for more than a decade. Currently commercial wafer bonder can offer 6" processes of silicon fusion bonding and anodic bonding [1]. Since it is able to form microstructures like pressure sensor, accelerometer, and packaging of microsensors [2]. In most cases the hermetic sealing and interface bonding strength are major concerned, while low-temperature processing is essential in the case of bonding a microelectronic wafer to a micromechanical wafer in order to facilitate integration and achieve increment of device density. However, the commercialized wafer bonding technology can not meet this demand well, since process temperature is relatively high, such as silicon fusion bonding of 1000 °C, and anodic bonding of 450 °C [1]. The anodic bonding can be performed at 180 °C by using high alkaline content glass [3], nevertheless, it is not a commercial available process and high alkaline content may cause degregation of IC for monolithic IC sensors. The intermediate bonding by using Au-Si eutectic bonding, i.e., adding adhesive interlayer, has been proposed as another potential way to reduce bonding temperature. It concluded a necessary process temperature of 500 °C that is higher than the Au-Si eutectic temperature of 363 °C [4]. On the other hand, an Au-Au_4Al-Si intermediate bonding at 350°C is reported for

*Correspondence: Email: vclee@infrared.com.tw; Tel: +886-3-5632161; Fax: +886-3-5632509

Part of the Conference on Design, Characterization, and Packaging for MEMS and Microelectronics
Royal Pines Resort, Queensland, Australia • October 1999
SPIE Vol. 3893 • 0277-786X/99/$10.00

packaging infrared microsensor successfully [5]. The same group also use Au/Sn to Ni/Au solder bonding, and Sn/Pb to Ni/Au solder bonding for making a sealed cavity of capacitive pressure sensor, while the respective treatment temperature are 300 °C, and 250 °C for fluxless soldering in an vacuum oven with infrared light [6]. Actually all materials that provide enough bonding force to the adhesive can be used at the bonding interface. The epoxy and thermoplastic polymer have been applied to the wafer level packaging with heat treatment temperatures of 150 °C and 280 °C, respectively [7].

However, a lower bonding temperature is not only for easier integration of circuits, but also for minimizing bonding-induced stress problem after cooling. Except the above mentioned hermetic sealing, interface bonding strength, and bonding temperature, the vacuum-sealed cavity is able to gain the design of pressure sensor of a wide dynamic range with high resolution [8]. Vacuum package is known to be necessary for thermal sensors and some resonant sensors due to the merit of increasing responsivity [9,10]. In this paper we report a new low temperature wafer bonding process based on using In-Sn alloy as the intermediate layer for bonding. The feasibility of forming a vacuum-sealed cavity by In-Sn wafer bonding is also studied.

2. PROCESS DEVELOPMENT AND EXPERIMENTAL RESULTS

2.1. Basic preparation procedure of samples

In-Sn alloy has eutectic temperature near 120°C, it is frequently used as the final treatment of step soldering. The In-Sn alloy shows fair wetability to most alloy, its ductility and ability of against creep are compatible with Pb-Sn alloy. In the experiment, material of In-Sn (50/50) eutectic composition was vacuum-evaporated onto a lid wafer with film thickness of 2 to 12 μm, while another gold-coated wafer is used to imitate the sensor wafer. A 100 nm Au-Sn (80/20) thin layer was deposited subsequently on In-Sn surface in order to avoid oxidation of indium when In-Sn surface exposures in atmosphere. A pair of matching patterns was delineated on both the films of individual wafers for the purpose of diffuse bonding. The two wafers were then taken for pattern alignment with a double-side aligner. They were then held in position with a fixture and transferred into a vacuum chamber for physical bonding. They were first subjected to vacuum evacuation and pressed, then gradually heated to a preset temperature for a defined soldering duration before cooling down. The integrated (bonded) wafers were than sawed into pieces of sample for subsequent testing.

2.2. Adhesive strength evaluation

In the case of real application, the contacting surface of sensor wafer may be bare silicon or SiO_2, so we design 6 combinations of bonding interface to make optimization, as shown in Table 1. The Au 2μm / Ti 200Å thin film has been deposited onto the base wafer B2 and B3, and lid wafer L2. Then InSn 12μm and AuSn 100 nm films have been subsequently deposited onto the lid wafer L1 and L2. All of the depositions were done at the $3x10^{-6}$ torr by thermal coating. The specimens were diced into 8x8 mm^2 samples for later on bonding experiment. A pair of samples were put inside a vacuum chamber, and the soldering condition is 160 °C, $5x10^{-5}$ torr, with an axial loading of 3 kg/cm^2 for 1.5 hours.

Lid Wafer / Base Wafer	Si//InSn//AuSn	Si//Au//InSn//AuSn
Si (with native oxide)	Failed	52 kg/cm^2
Si/SiO_2//Au	Failed	150 kg/cm^2
Si//Au	82 kg/cm^2	207 kg/cm^2

Table. 1 Interface strength for various pairs of substrates

Pulling test via a force perpendicular to the substrate can derive the interface bonding strength. As shown in Table 1, L1/B1 and L1/B2 pairs have failed, while the L1/B3, L2/B1 and L2/B2 show fairly interface strength. It points out the adhesion between Si//InSn is comparatively weak. Additionally the SiO_2//Ti//Au interface is weaker than Si//Ti//Au interface. Pair of L2/B3 shows the best result of interface strength 207 kg/cm^2. We characterized the fracture surface of separated, broken, samples of L2/B3 pair. From Fig. 1, it can be observed as a ductile fracture surface from the fracture surface morphology. There is no evidence that cracks initiated from void defects and propagated during the pulling test, then fracture of bonding interface may induced by these cracks. Additionally the fracture interface of some samples was even observed in the broken silicon substrate in stead of the soldering interface, as shown in Fig. 2. We prepared L2/B3 pair at the same condition but various temperatures as well. It is found from the experiment that a interface strength as high as 210 kg/cm^2 for the case of 170 °C heat treatment (Fig.3). The strength of 120 °C sample drops from 125 kg/cm^2 down to 50 kg/cm^2 of 100 °C sample. It means the soldering process could not proceed well at a temperature below the eutectic temperature of InSn alloy.

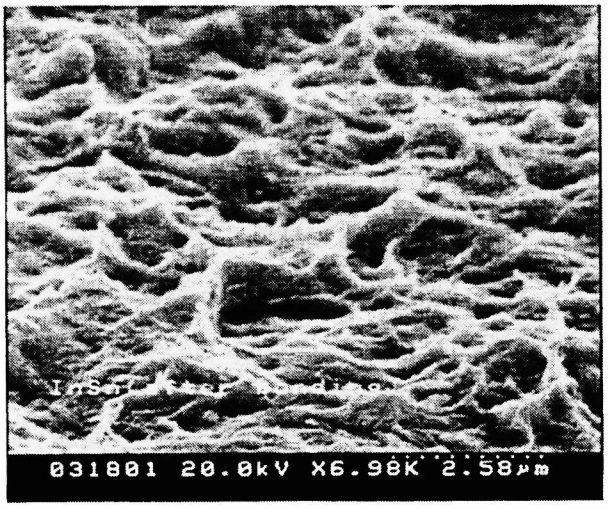

Fig.1 SEM photo of the fracture surface of bonding interface.

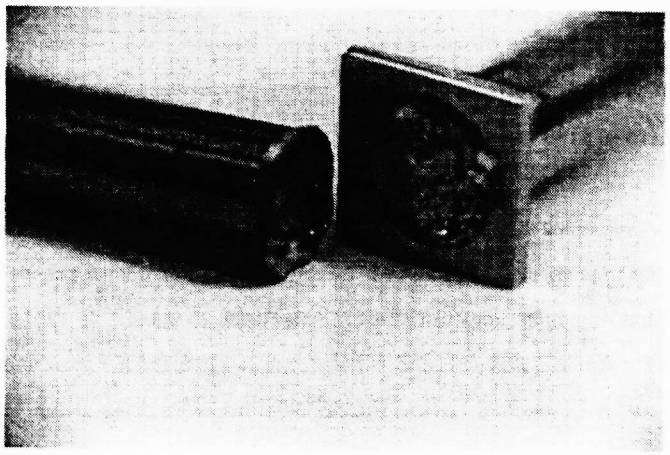

Fig.2 Photo of the fracture surface of bonded sample pair.

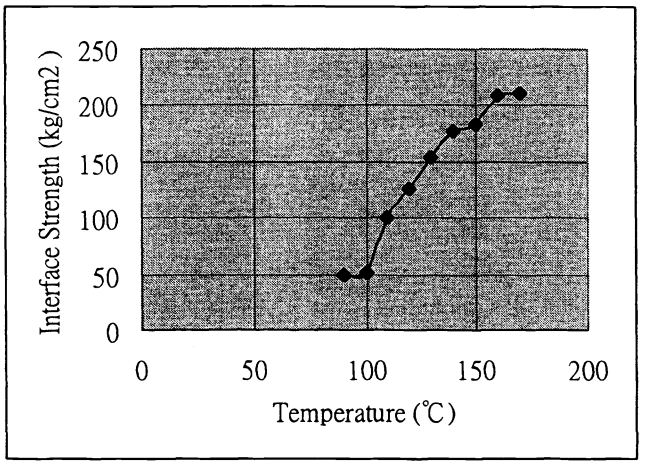

Fig.3 Interface strength of different soldering temperatures.

2.3. Sealing evaluation

After the bonding strength evaluation, helium leak rate test was used to check the quality of interface. The anisotropic Si wet etching was applied to make a through wafer hole of one B3 sample, another plain L2 sample is prepared. They were bonded together at the same condition as previous bonding experiment but with various temperatures. We use the silver paste to fix the sample on an adapter, which is connected with pumping tube of leak rate tester. Then helium gas is sprayed onto the bonding interface.

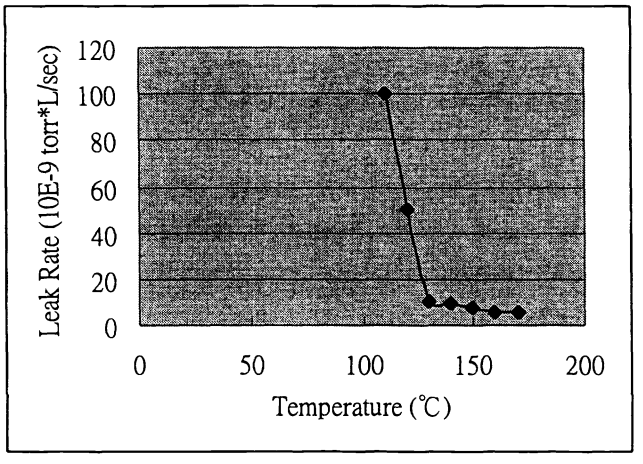

Fig.4 Helium leak test data of different soldering temperatures.

From Fig. 4, we find the leak rate decrease quickly when the bonding temperature increase, and a helium leak as low as $6x10^{-9}$ torr-liter/sec can be obtained for temperature higher than 150°C. This value is superior than that reported by others [11]. A fair value is obtained for 130 °C, while the leak rate becomes higher than $1x10^{-7}$ torr-liter/sec for bonding temperature less than 110 °C. Interface inspection by scanning acoustic microscope (SAM) shows that the bonding interface is pore-free for the L2/B3 bonded samples (Fig.5). This SAM has the resolution about 100 μm, some small reflective steps will occur in Fig. 5, if there are some cracks or pores.

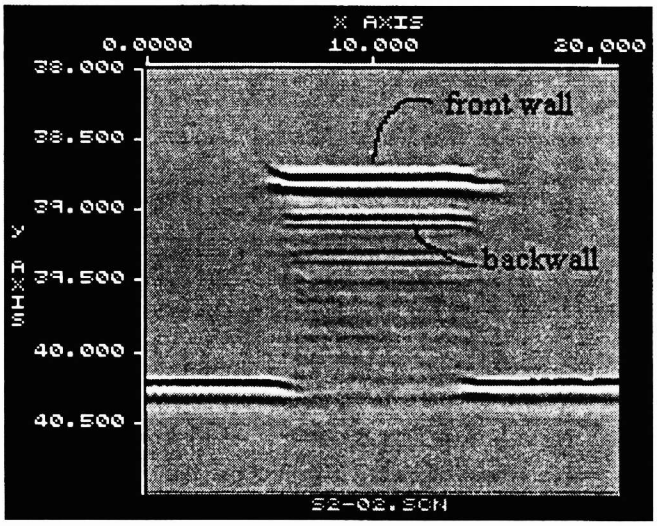

Fig.5 Interface inspection of the bonding quality by Scanning Acoustic Microscope.

2.4. Materials characterization

Fig. 6 shows the surface morphology of the as-deposited InSn film, the roughness of 2 ~ 4 μm can be observed. We also find lid wafers with thickness of InSn less than 6 μm were hard to be bonded in the bonding experiment. This fact reflects that a minimum solder film thickness is necessary to overcome influence of surface roughness. As a result, we applied 12 μm thick InSn solder film in the bonding experiment to avoid surface roughness effect. The Auger surface spectrum and depth profile analysis were applied to characterize the oxygen element content of surface of AuSn with 100nm thickness. It showed very low oxygen content. This fact help us to believe that the AuSn thin film acts as a passivation layer to prevent oxidization of beneath InSn film, since the indium is a strong reduction precursor.

The raw materials for preparing InSn solder film have been characterized by X-ray diffraction analysis. The major phase of In_3Sn (β) and minor phase of $InSn_4$ (γ) can be observed in the XRD pattern of InSn (50/50) solder preform, i.e., the raw materials. On the other hand, the XRD pattern of evaporated solder film shows major γ phase and minor β phase. Checking eutectic point of In-Sn phase diagram, eutectic composition of InSn (51/49) at 120 °C can be observed. However, in the case of

InSn (50/50), the melting point becomes around 125 °C [12]. In the soldering process of bonding experiment, some grains of β-Sn (high temperature phase with melting point of 232 °C) will nucleate and grow from the $InSn_4$ matrix, while some $InSn_4$ and In_3Sn will start melting. Good melting state should be reached above 125 °C, but some remaining β-Sn particles inside melted solder need time and higher temperature to consume themselves and transfer into liquid through solid/liquid interface diffusion. This can explain only the samples treated above 130 °C show good leak rate test results in Fig. 4. We also know indium is a material showing cold welding behavior. It means some In rich area may start melting at a temperature a little bit below 125 °C when a force loading applied on to samples. This is the reason for L2/B3 samples still exhibit 50 kg/cm^2 bonding strength, even this value is poor.

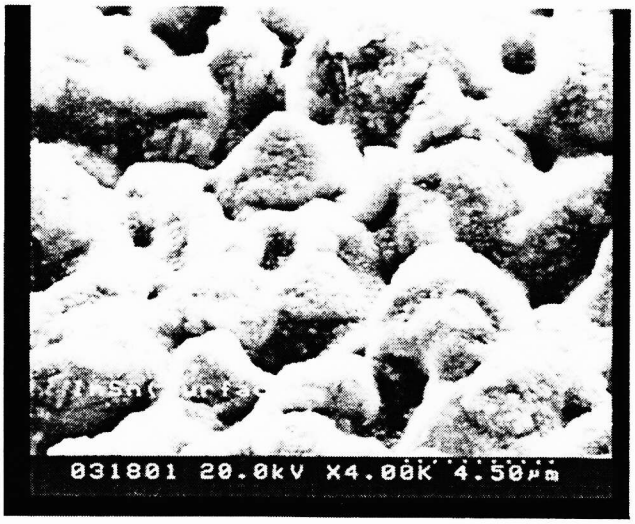

Fig.6 SEM photo of the surface morphology of as-deposited InSn solder film.

2.5. Characterization on vacuum degree and reliability

In order to identify the pressure inside the packaged cavity of L2/B3 samples, the wet etched B3 wafer with 15 μm thick diaphragm was bonded with L2 wafer at 160 °C. Then the bonded wafer were diced into 8x8 mm^2 pieces. Because the inside pressure is lower than the atmosphere, a concavity of B3 surface can be observed by human eyes, and measured with 4 μm depth in the center. We built a FEM model to analyze and simulate the relationship between displacement of center point and inside pressure. Displacement will become saturated when inside pressure is less than 0.01 torr from Table 2. The measured displacement is about 4.1 μm ± 0.1μm for various samples. As a result, we believe the inside pressure should be lower than 50 torr. Packaging a microbolometer inside the cavity for directly measuring the vacuum degree may be a good method for more precise evaluation. Since microbolometer has been applied as a micro-pirani gauge for measuring the vacuum down to 0.001 torr [13]. Moreover, a vacuum-sealed capacitance type pressure sensor has been reported as an alternative way for measurement [14].

P_{inside} (torr)	760	400	100	30	20	10	0.01	0.001
Displacement (μm)	0	2.06	3.72	4.1	4.15	4.2	4.26	4.26

Table. 2 The simulated displacement of center point for concave diaphragm versus inside pressure.

The temperature cycles of 10 minutes duration at -10 and 80°C with two minutes switch time were used to characterize L2/B3 samples. Cycles of 100, 200, 400, 800, and 1500 have been done, and samples after 1500 thermal cycling still show bonding strength of 200 kg/cm^2, leak rate of 6x10^{-9} torr-liter/sec, and measured center displacement of about 4 μm. It exhibits no trace of degradation compared to the initial quality of the bonded samples.

3. CONCLUSIONS

A novel low temperature wafer bonding with process temperature lower than 160°C is proposed, it applies the In-Sn alloy to form the interface of wafer bonding. The experiment results show helium leak test of 6x10^{-9}torr-liter/sec, and a tensile strength of bonding interface as high as 200kg/cm^2. Reliability test after 1500 temperature cycles between -10 to 80°C also shows no trace of degradation compared to the initial quality of the samples. It is concluded that the In-Sn (50/50) eutectic solder is an ideal low-temperature interlayer of bonding process for vacuum-sealed package application of microsensors.

ACKNOWLEDGMENTS

This study is supported by Chinese Petroleum Corp. under the MOEA Small Business R&D Supporting Program with contract of "0288013" in the title of "R&D project of CSP for MEMS components".

REFERENCES

[1] A. R. Mirza, A. A. Ayon, Silicon Wafer Bonding: Key to MEMS High-Volume Manufacturing, *Sensors,* Vol. 15, No. 12, pp. 24-33, 1998.
[2] M. A. Schmidt, Wafer-to-Wafer Bonding for Microstructure Formation, *Proc. of the IEEE,* Vol. 86, No. 8, pp. 1575-1585, 1998.
[3] Shuichi Shoji, Hiroto Kikuchi, Hirotaka Torigoe, Low-temperature Anodic Bonding Using Lithium Aluminosilicate—Quartz Glass Ceramic, Sensors & Actuators A, Vol. 64, pp. 95-100, 1998.
[4] R. F. Wolffenbuttel, Low-temperature Intermediate Au-Si Wafer Bonding; Eutectic or Silicide Bond, Sensors & Actuators A, Vol. 62, pp.680-686, 1997.
[5] M. Waelti, N. Schneeberger, O. Paul, and H. Baltes, Low-temperture Packaging of CMOS Infrared Microsystems by Si-Al-Au Bonding,, *Proc. Electrochem. Soc.,* Paris, Vol. 97-36, pp. 147-154, 1998.
[6] B. Rogge, D. Moser, H. Oppermann, O. Paul, and H. Baltes, Solder-bonded Micromachined Capacitive Pressure Sensors, *Proc. of the SPIE,* Vol. 3514, pp. 307-315, 1998.
[7] G. Klink and B. Hillerich, Wafer Bonding with an Adhesive Coating, *Proc. of the SPIE,* Vol. 3514, pp. 50-61, 1998.
[8] A. V. Chavan, et. al, A Batch-processed Vacuum-sealed Capacitive Pressure Sensor, Transsducers'97, Chicago, USA, pp.1449-1452, June 16-19, 1997.
[9] J.-S. Shie, Y.-M. Chen, M. Ou-Yang, and B. C. S. Chou, Characterization and Modeling of Metal-Film Microbolometer, J. MEMS, Vol. 5, No. 4, pp. 183-189, 1996.

[10] L. Lin, K. M. McNair, R. T. Howe, and A. P. Pisano, Vacuum-encapsulated lateral microsensors, Transducers'93, Yokohama, Japan, pp.270-273, June 7-10, 1993.
[11] H. Reichl, Packaging and Interconnection of Sensors, Sensors & Actuators A, Vol. 25-27, pp. 63-71, 1991.
[12] C. E. T. White and H. Okamoto, Phase Diagrams of Indium Alloys and Their Engineering applications, ASM International, May 1992.
[13] J.-S. Shie, Bruce C. S. Chou, and Y.-M. Chen, High Performance Pirani Vacuum gauge, J. Vac. Sci. Technol., A, Vol. 13, No. 6, pp. 2972-2979, 1995.
[14] M. Esashi, S. Sugiyama, K. Ikeda, Y. Wang, and H. Miyashita, Vacuum-sealed Silicon Micromachined Pressure Sensors, *Proc. of the IEEE,* Vol. 86, No. 8, pp. 1627-1639, 1998.