A CMOS Transistor-Only 8-b 4.5-Ms/s Pipelined Analog-to-Digital Converter Using Fully-Differential Current-Mode Circuit Techniques

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Abstract— **Fully-differential current-mode circuit techniques are developed for the design of a pipelined current-mode analog-to-digital converter (IADC) in the standard CMOS digital processes. In the proposed IADC, the 1-b-per-stage architecture based on the reference nonrestoring algorithm is adopted. Thus large component ratios can be avoided and the linearity errors caused by device mismatches can be minimized. As one of the key subcircuits in the IADC, an offset-canceled high speed differential current comparator (CCMP) is proposed and analyzed. In the CCMP, the subtractions of offsets are performed in the current domain without floating capacitors. Moreover, the other key subcircuit, the current sample-and-hold amplifier (CSHA), is also developed to realize the pipeline architecture. An experimental chip for the proposed IADC has been fabricated in 0.8-μm n-well CMOS technology. Using a single 5-V power supply, the fabricated IADC can be operated at 4.5-Ms/s conversion rate with a signal-to-noise-and-distortion-ratio (SNDR) of 51 dB (effective 8.2-b) for the input signal at 453 kHz. For 8-b resolution, the fabricated IADC can be operated at 4.5-Ms/s conversion rate with both differential nonlinearity (DNL) and integral nonlinearity (INL) below +/− 0.6 LSB. The power consumption and the active chip area are 16 mW/b and 0.73 mm^2/b, respectively.**

I. Introduction

DUE TO THE rapid advancement of the CMOS digital technologies, an increasing number of functions in signal processing systems are implemented in the digital domain to reduce the cost and increase the reliability. However, the signals in the real world are inherently analog and thus analog-to-digital (A/D) conversions are needed to interface the digital circuits to the real world. The dominance of the digital circuits in a single-chip system brings out the strong desire to realize the A/D converters in the standard digital processes. Ideally, digital process compatible A/D converters must be realized without relying on closely matched or high performance resistors or capacitors [1]–[4].

For high-speed applications, flash A/D converters generally achieve the highest conversion rate. However, for more than 8-b resolution, flash converters suffer from the exponential growth of die area and power dissipation. Moreover, due to the large nonlinear input capacitance, dedicated external circuits are needed to achieve the required resolution at high input frequencies [5]–[9]. To solve these problems, CMOS pipelined A/D converters which achieve 8 to 10 b resolution at high conversion rate have been proposed [7]–[9]. However, these converters utilize the switch-capacitor (SC) techniques to implement the interstage gain required in the pipelined structure and thus additional process steps must be added to realize the linear capacitors used in the SC circuits.

Recently, current-mode techniques in which the signals are processed in the current domain have been proposed to design digital process compatible filters [11]–[15] and A/D converters [1]–[4]. Current-mode circuits offer the potential advantages such as inherent low voltage swing and no need of linear capacitors which make current-mode signal processing an attractive alternative to conventional voltage-mode approaches.

Nairn and Salama [1] have successfully demonstrated a digital process compatible IADC with 10-b accuracy and 25 kHz conversion rate by the active dynamic-matching current-copier techniques based on the cyclic architecture. The IADC proposed by Daubert *et al.* [3] uses the current-copier integrator to develop a transistor-only sigma-delta modulator with 12-b linearity and 3.4 kHz input signal bandwidth. An 8-b IADC with a higher conversion rate of 500 ks/s is also developed in [2] by the active current mirror techniques. However, this converter requires the external off-chip sample/hold (S/H) circuits for high frequency inputs.

In this work, new current-mode circuit techniques are developed to realize an 8-b, 4.5 Ms/s pipelined IADC in a CMOS digital process. The interstage gains needed in the pipelined structure are realized by the sizing ratios of the transistors instead of linear capacitors so that the IADC can be fabricated by the standard digital process. The IADC structure is also arranged to avoid the use of large component ratios so that the linearity errors caused by the device mismatch can be minimized. In contrast to the single-ended configurations used in [1], [2], and [4] the proposed IADC are implemented by fully-differential circuits. Fully differential configurations can offer better design flexibility, 6-dB increase in the dynamic range and a higher immunity against clock feedthrough noises [13]. Additionally, since the IADC is expected to be integrated in a digitally-dominated chip, it must be operated in the presence of large power line noises caused by the digital

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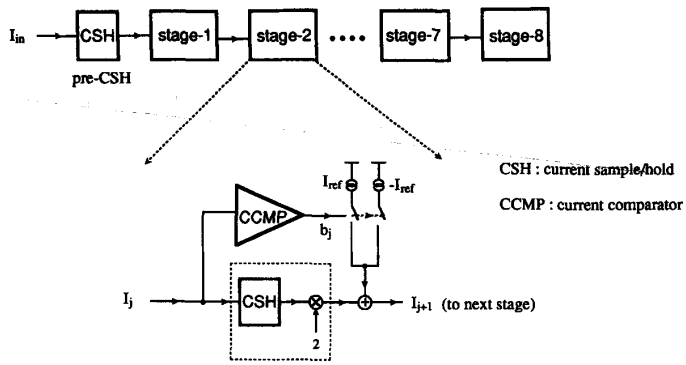

Fig. 1. The schematic diagram of the proposed 8-b IADC.

circuits, especially when the clock rate is high. Therefore, fully-differential circuit implementations are vital to obtain high signal-to-noise-ratio (SNR) and power-supply rejection ratio (PSRR) at high operating frequencies.

In Section II, the A/D conversion algorithm and architecture are described. In Section III, the designs of the offset-canceled current comparator (CCMP) and the current reference generation scheme are presented. In Section IV, the current sample/hold amplifier (CSHA) design is described. The experimental results including the dynamic testing of the IADC using an on-chip V–I converting circuit are presented in Section V. Finally, a conclusion is given in Section VI.

II. Architecture and Algorithm

The schematic diagram of the proposed IADC based on the reference nonrestoring A/D conversion algorithm [10] is shown in Fig. 1. The 8-b IADC consists of a pre-current-sample/hold (pre-CSH) circuit and 8 identical 1-b pipelined stages with the output of the previous stage connected to the input of the next stage. Each stage contains a current sample/hold circuit (CSH), an interstage current amplifier of gain 2, a current comparator (CCMP), and current references I_{ref} and $-I_{\text{ref}}$. In each pipelined stage, the polarity of the input current I_j is determined by the current comparator first. If the input is positive, the corresponding bit is ONE and the residual current for the next stage is $(2I_{\text{j}} - I_{\text{ref}})$. If negative, the bit is ZERO and the residual current is $(2I_{\text{j}} + I_{\text{ref}})$. The residual current I_{j+1} is then sent to the next stage to determine the next bit. Therefore, the sampled input current can be pipelined to the cascaded stages to determine its digital codes sequentially. In practical implementation, the functions of amplification-by-2 and sample/hold are realized simultaneously by a current sample/hold amplifier (CSHA). In contrast to the reference restoring algorithm used in [1] and [2], the extra reference restoring operation can be eliminated by using the nonrestoring algorithm which leads to higher operating speed and less circuit complexity. Note that if the single-ended configuration is used, two well-matched current references I_{ref} and $-I_{\text{ref}}$ are required for the nonrestoring algorithm. However, the matching requirement for these two reference currents is eliminated if fully-differential configurations are used because signal inversion can be performed by cross-connection of the differential signal pairs.

TABLE I
The Operations of the CSHA and CCMP of the Three Neighboring Stages Under the Two Different Clock Timing Phases

phase / stage		ϕ_1	ϕ_2
N+1	CSHA	H	S/A
	CCMP	AZ	CP
N	CSHA	S/A	H
	CCMP	CP	AZ
N-1	CSHA	H	S/A
	CCMP	AZ	CP

H : hold, S/A : sample/amplification
AZ : auto-zero, CP : comparison

The converter is clocked by two nonoverlapped clocks so that each conversion requires only two clock phases. To get a high conversion rate, the clocking strategy must be chosen according to the circuit characteristics of CSHA and CCMP such that they can work concurrently. The operations of three neighboring stages during the two clock timing phases are illustrated in Table I. In each stage, the sampling/amplification operation of the CSHA and the comparison of the CCMP are performed simultaneously in the first clock phase. In the second clock phase, the CSHA is switched to the hold mode with its output sampled by the next stage and the CCMP is switched to auto-zero mode for offset-cancellation with its digital output latched to control the current steering switches for current references. Since the sampling operation of the CSHA and the comparison operation of the CCMP are performed in the same clock phase, a pre-CSH circuit with two unity-gain outputs must be placed in front of the first pipelined stage as shown in Fig. 1.

III. Current Comparator Design

The basic function of the CCMP is to provide sufficient amplification for the small difference between two input current levels and generate the corresponding digital voltage

level. The CCMP is thus effectively a current-to-voltage (I–V) comparator. In the IADC architecture shown in Fig. 1, the offset of the CCMP in the pipelined stages would result in the linearity errors for the IADC except that in the first stage. Consequently, in addition to provide a sufficient gain for a small input signal, the offset of the CCMP must also be smaller than 1/2 LSB. Many high performance voltage comparators (VCMP) have been analyzed and developed in the past [20], [21]. However, differential current comparators with offset cancellation and high operating speed suitable for the IADC design have not been reported to date [26].

A. Offset Cancellation by Auto-Zero Techniques

A sense amplifier is a fast VCMP because its amplification is achieved by means of regeneration. However, its large offset voltage caused by device mismatches limit its resolution to about 5-b [20]. Therefore, in the VCMP design, the sense amplifier is preceded by some amplifier stages. The offset errors of these gain stages can be greatly reduced using the auto-zero (offset-cancellation) technique [19]–[22] and thus higher resolution can be obtained.

For a high-gain amplifier, when the input and the initial conditions are of opposite polarity, the response time of the amplifier to reach a threshold point is degraded by the nonzero exponential decay of the initial condition. Since the initial condition can be reset to zero through the auto-zero operation, the auto-zero technique also helps to reduce the response time of the amplifier stages. Additionally, the auto-zero technique also offers the advantage of self-biasing which reduces the bias sensitivity to process variations and eliminates the need for additional bias circuits.

B. Fully-Differential I–V Converter with Offset Cancellation

Consider the design of a high speed, offset-canceled I–V CCMP for the pipelined IADC. Generally, the input currents must be converted into voltages through an I–V converting circuit. The I–V conversion could be performed by the direct use of resistors or its equivalents. For example, the CCMP in [3] uses a MOS transistor operated in the triode-region as a resistor to perform the I–V conversion. When a resistor R is used directly to perform the I–V conversion, the response time becomes strongly dependent on the output characteristics of the input signal sources. If the capacitance load imposed by the input source is large, the response time is significantly increased. In addition, the effective I–V conversion transresistance is given by $(R//R_s)$ where R_s is the output resistance of the input signal source. If R_s is on the same order as R or is smaller than R, the effective transresistance is degraded which also leads to the increase of the response time. Therefore, the direct use of resistors imposes some severe limitations on the output characteristics of the input signal sources. In the case of the IADC design, the input source is the CSHA. The situation is further complicated if fully-differential configurations are used. The common-mode input currents cannot be rejected and they might drive the following gain stages out of their operating ranges if the I–V conversion resistor R is large.

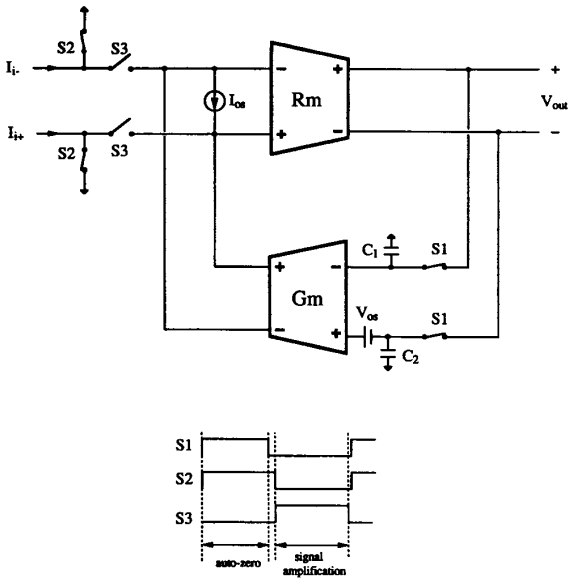

Fig. 2. The schematic diagram of the offset-canceled I–V converter.

To overcome the above limitations, a novel differential I–V converter with offset cancellation is proposed to perform the I–V conversion instead of the direct use of resistors. Fig. 2 shows the block diagram of the offset-canceled I–V converter where R_m is the transresistance amplifier for the I–V conversion and G_m is the transconductance amplifier for the offset cancellation. The clock waveforms are also shown in Fig. 2. In operations, the auto-zero cycle begins at the instance when the switch S1 is turned on. The input currents are bypassed to a fixed bias voltage by turning on S2 while turning off S3 and thus the external input current to the R_m amplifier is zero. The G_m amplifier senses the output voltage V_{out} of the R_m amplifier and converts it into currents. The currents are fed back to the inputs of the R_m amplifier. As a result, the offset current I_{os} of the R_m amplifier and the offset voltage V_{os} of the G_m amplifier can be obtained at the output V_{out} of the R_m amplifier. The output voltage is given by

$$V_{\text{out}} = \left(\frac{R_m}{1 + R_m G_m}\right) I_{\text{os}} + \left(\frac{R_m G_m}{1 + R_m G_m}\right) V_{\text{os}}. \quad (1)$$

After the circuit has settled down to the required accuracy, the auto-zero cycle is ended by turning off S1. Due to the charges stored on the capacitors C_1 and C_2, the output currents of the G_m amplifier containing the offset information can still be sent to the inputs of the R_m amplifier. Therefore, if $R_m G_m \gg 1$, the effective offset at the inputs of the R_m amplifier can be expressed as

$$I_{\text{os,eff}} = \left(\frac{1}{R_m G_m}\right) I_{\text{os}} + \left(\frac{1}{R_m}\right) V_{\text{os}} + G_m \left(\frac{Q_{\text{inj}}}{C}\right) \quad (2)$$

where I_{os} and V_{os} are the offset errors of the R_m and G_m

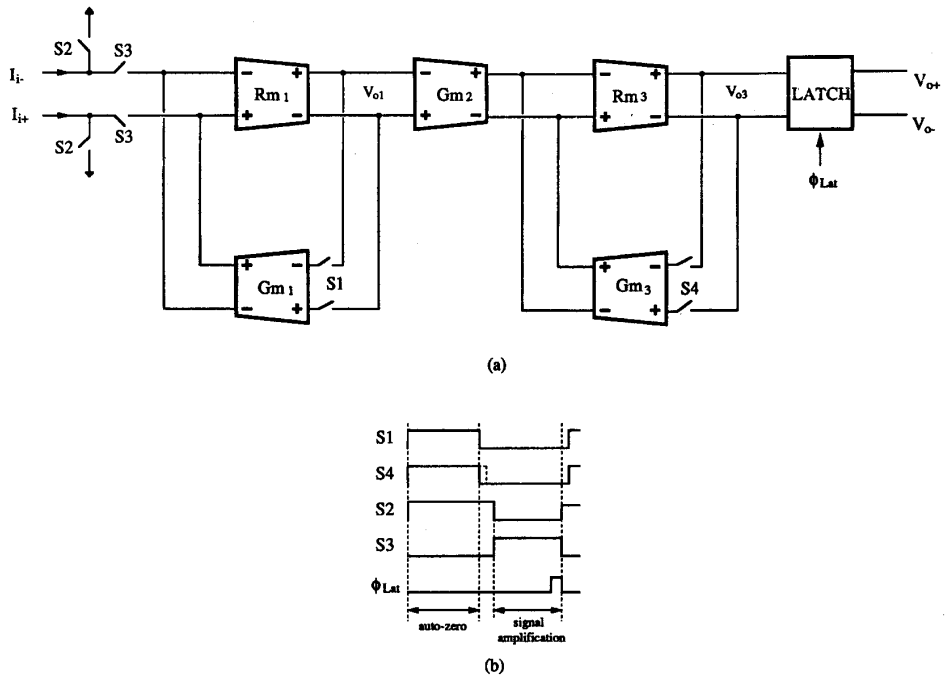

Fig. 3. (a) The schematic diagram and (b) the clock waveforms of the proposed CCMP.

amplifiers, respectively. The third term arises from the charges Q_{inj} injected from the turn-off transients of S1 and C is the nominal capacitance for C_1 and C_2. It can be seen from (2) that the offset current I_{os} of the R_m amplifier is attenuated by the auto-zero loop gain R_mG_m. Moreover, the contribution of the offset voltage V_{os} of the G_m amplifier to $I_{\text{os,eff}}$ is divided by the gain factor R_m when referred to the inputs of the I–V converter. Therefore, as compared to the case without the G_m amplifier added to perform the auto-zero operation, the effective offset of the I–V converter can be significantly reduced if R_m is sufficiently large. The optimum values for G_m is $\sqrt{CI_{\text{os}}/(Q_{\text{inj}}R_m)}$ which gives the optimum offset as

$$I_{\text{os,opt}} = 2\sqrt{\left(\frac{1}{R_m}\right)\left(\frac{Q_{\text{inj}}}{C}\right)I_{\text{os}}} + \left(\frac{1}{R_m}\right)V_{\text{os}}. \quad (3)$$

After switch S1 has been turned off, the I–V converter can be switched to the signal-amplification cycle by turning off S2 and turning on S3 to steer the input currents to the R_m amplifier. During the signal-amplification cycle, the current input nodes and the voltage output nodes are buffered by the R_m amplifier. Therefore, the dependence of the response time on the output resistance and capacitance of the input signal source can be minimized.

C. Offset-Canceled CCMP

Based on the similar operating principle of the offset-canceled I–V converter, the block diagram of the proposed CCMP is constructed and shown in Fig. 3(a). The clock waveforms are also shown in Fig. 3(b). The CCMP consists of two offset-canceled I–V converters R_{m1}-G_{m1} and R_{m3}-G_{m3} and one interstage transconductance amplifier G_{m2}. Since a single stage I–V converter cannot sufficiently amplify the 1/2 LSB input current to override the offset of the regenerative latch within the time allowed, more gain stages are used. The transconductance amplifier G_{m2} acts as a gain stage as well as an interface between the two transresistance amplifiers R_{m1} and R_{m3}.

In operation, firstly, the CCMP is switched to the auto-zero cycle by turning on the switches S1 and S4. Meanwhile, the input currents are bypassed to a fixed bias voltage by turning on S2 while switching off S3. The offset-cancellation cycle is ended by switching off the feedback switches S1 and S4. The input currents can then be steered to the inputs of the CCMP for signal amplification by turning off S2 and turning on S3. In this signal-amplification cycle, the input currents are amplified by the three cascaded gain stages R_{m1}, G_{m2}, and R_{m3}. Once the output V_{o3} reaches the threshold point of the latch, the dynamic latch is enabled by raising ϕ_{Lat} to high to further amplify the signal to the full logic levels through regeneration.

If $R_{m1}G_{m1} \gg$ and $R_{m3}G_{m3} \gg 1$, it can be shown that the effective offset at the inputs of the CCMP is

$$I_{\text{os,eff}} \approx \frac{I_{\text{os1}}}{R_{m1}G_{m1}R_{m3}G_{m3}} + \frac{V_{\text{os1}} + V_{\text{os2}}}{R_{m1}R_{m3}G_{m3}} + \frac{I_{\text{os3}}}{R_{m1}G_{m2}R_{m3}G_{m3}} + \frac{V_{\text{os3}}}{R_{m1}G_{m2}R_{m3}} + \left(\frac{Q_{\text{inj,1}}}{C_1}\right)G_{m1} + \left(\frac{Q_{\text{inj,2}}}{C_3}\right)\left(\frac{G_{m3}}{R_{m1}G_{m2}}\right) \quad (4)$$

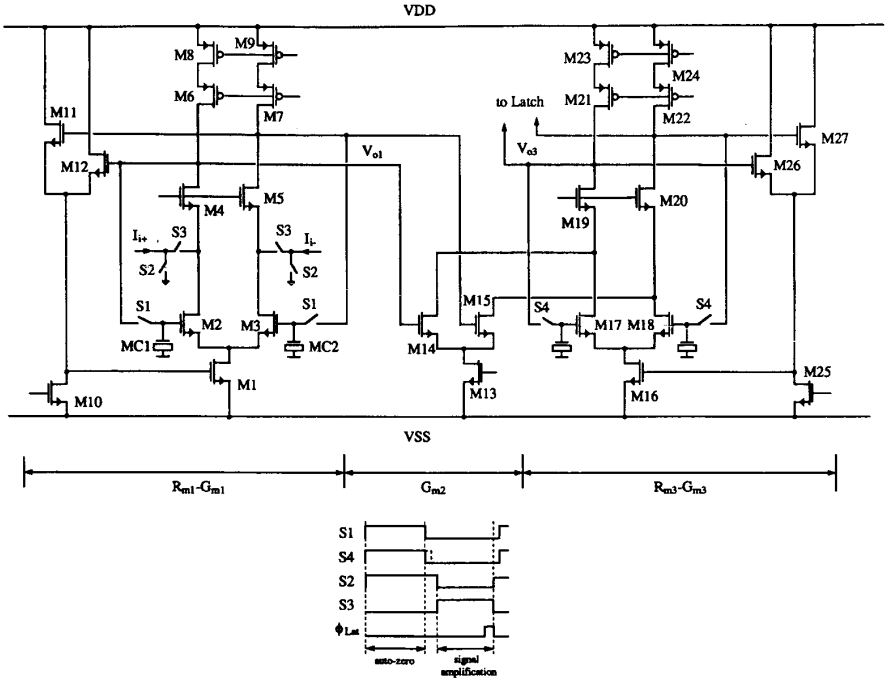

Fig. 4. The circuit diagram of the CCMP (the latch is not shown).

where I_{os1}, V_{os1}, V_{os2}, I_{os3}, and V_{os3} are the offsets of the amplifiers R_{m1}, G_{m1}, G_{m2}, R_{m3}, and G_{m3}, respectively, and $Q_{inj,1}$ and $Q_{inj,2}$ are the charges injected from the turn-off transients of the switches S1 and S4, respectively. It can be seen from (4) that the offset current I_{os1} of the R_{m1} amplifier is attenuated by the product of the two auto-zero loop gains $R_{m1}G_{m1}$ and $R_{m3}G_{m3}$. The offset current I_{os3} of the R_{m3} amplifier is attenuated by the second auto-zero loop gain $R_{m3}G_{m3}$ as well as the preceding gain stages R_{m1} and G_{m2}. The contributions of the offset voltages V_{os1} and V_{os2} of the G_{m1} and G_{m2} amplifiers to $I_{os,eff}$ are reduced by the preceding R_{m1} stage as well as the second auto-zero loop gain $R_{m3}G_{m3}$. The contribution of the offset voltage V_{os3} of the G_{m3} amplifier to $I_{os,eff}$ is reduced by the three preceding gain stages R_{m1}, G_{m2}, and R_{m3}. Therefore, with the feedback G_m amplifiers added to perform the auto-zero operations, the effective offset of the CCMP can be significantly reduced as compared to the case without the feedback G_m amplifier. The errors caused by the charge injection $Q_{inj,1}$ can be further reduced by delaying the turn-off of S4 with respect to that of S1.

Note that the offset errors of the second gain stage can be attenuated by the first gain stage even without the associated auto-zero circuitry. However, as described in part A of this section, besides the reduction of offset errors, the auto-zero operation also offers the advantages of operating speed improvement and bias stability. Moreover, the auto-zero operation can be achieved without significantly increasing the circuit complexity. Therefore, the auto-zero circuitry is added to the second gain stage in the CCMP design.

The detailed circuit diagram of the CCMP is shown in Fig. 4. The transistors M1–M12 constitute the R_{m1}-G_{m1} offset-canceled I–V converter. The cascode constant current sources formed by M6–M9 offer not only the bias currents but also the required transresistance. The transistors M4 and M5 are used as input current conveying devices as well as casccode devices to increase the output resistance and reduce the Miller-effect. The feedback transconductance amplifier G_{m1} is constructed by the transistors M1–M3. To absorb the common-mode input currents, the transistors M10–M12 are used to form the common-mode feedback (CMFB). The offsets of this stage are stored on the gate nodes of M2 and M3. The two NMOS capacitors MC1 and MC2 are added to ensure the good settling behavior during the offset-cancellation cycle. These two capacitors also help to reduce the clock feedthrough noise caused by S1 and the capacitance coupling noises in the signal-amplification cycle. In this I–V converting circuit, the current input nodes (the source nodes of M4 and M5) and the voltage output nodes (the drain nodes of M4 and M5) are buffered by the transistors M4 and M5. In the IADC design, the current input nodes are connected to the outputs of the CSHA and the drains of the current reference transistors. Consequently, the capacitance loads at the current input nodes are much larger than those at the drain nodes of M4 and M5. Therefore, as compared to the resistor-based I–V conversion circuit, a shorter response time for the I–V conversion can be obtained because the major voltage swing occurs at the nodes with smaller capacitive loads.

The buffering provided by M4 and M5 also allows the use of high transresistance while keeping low input resistance.

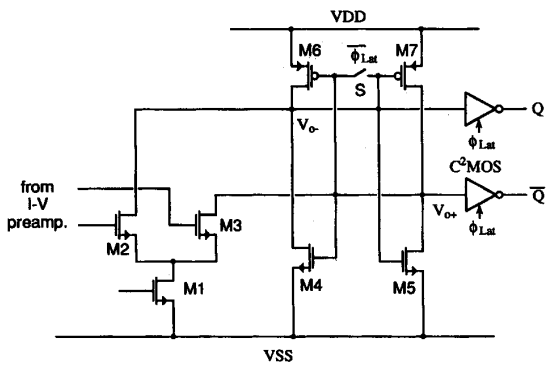

Fig. 5. The regenerative latch used in the CCMP.

The transresistance of the R_{m1}-G_{m1} stage is on the order of $(g_m r_d)r_d$ whereas the input resistance is r_d, where g_m and r_d are the nominal transconductance and output resistance of MOS transistors, respectively. Since the CSHA uses the cascode structure (as discussed in Section IV) whose output resistance is $(g_m r_d)r_d$, the output currents of the CSHA can be sent directly to the inputs of the CCMP without significant attenuation.

Similarly, the transistors M16–M27 form the offset-canceled I–V conversion stage R_{m3}-G_{m3}. The transconductance amplifier G_{m2} is constructed by the transistors M13–M15. The output currents of G_{m2} are sent directly to the inputs of R_{m3}.

The regenerative latch used in the CCMP is shown in Fig. 5. The transistors M1–M3 convert the amplified signals coming from the outputs of the I–V preamplifier to imbalance the latch formed by the cross-connected inverters M4–M7. The two C^2MOS inverters [29] clocked by ϕ_{Lat} are added to latch the digital outputs after the regeneration. When the input signals are being amplified by the I–V preamplifier described above, the switch S is turned on to equalize the two output nodes V_{o+} and V_{o-}. Once the output voltage difference from the I–V preamplifier is sufficiently large to override the offset of the regenerative latch, the switch S is turned off to enable the regeneration. The regeneration can amplify a 30 mV input imbalance to the full logic level in less then 5 ns. After V_{o+} and V_{o-} have been pulled up/down to the full logic swing, the clock ϕ_{Lat} can be pulled down to low. The digital outputs are thus latched by the two C^2MOS inveters.

HSPICE simulation results show that the auto-zero cycle time of the CCMP is less than 35 ns and the signal-amplification cycle time for a 0.1 μA input is less than 70 ns. The power consumption of the CCMP is about 5.5 mW which is one of the dominant power consuming blocks in the IADC.

D. Current Reference Generation

To generate the current references steered by the digital outputs of the CCMP in each pipeline stage, the master-slave current generation scheme [16], [23] is employed to reduce the errors caused by the device mismatches, power/ground line resistance, and power/ground line noises. Note that the matching of the current references in the first three pipeline stages are the most critical. The matching of the current references in the remaining pipelined stages are less critical because of the interstage gain.

IV. Current Sample/Hold Amplifier Design

To develop the CSHA used in the IADC, the following requirements must be considered. Firstly, single-stage structure is desired to have a short settling time and wide bandwidth. As shown in Table I, to perform each A/D conversion within two clock phases, the sampling operation of the CSHA and the comparison of the CCMP must be carried out in the same clock phase. Therefore, the CSHA must offer two outputs to drive the CSHA and CCMP of the next stage simultaneously. The gains of both outputs must ideally equal to two for the amplification of the residual currents. Although additional errors might be generated due to the mismatches between the two outputs of the CSHA, the mismatch errors can be minimized by using long channel (6 μm) devices and precision layout strategies [14]. To eliminate the requirement that the input characteristics of the CCMP and CSHA must be well matched, the output resistance of the CSHA must be high enough to reduce the loading effect. Thus the CSHA and CCMP can be designed more independently to optimize their performance.

Secondly, the charge holding nodes in the CSHA during the hold mode should be suitably isolated from the outputs to reduce the coupling errors caused by the parasitic C_{gd} capacitance [17], [25]. If the charge holding nodes are not isolated from the output nodes, the voltage difference at the output nodes when switching from the sample mode to the hold mode results in errors through the parasitic C_{gd} capacitance of MOS transistors into the holding currents which are to be sampled by the next stage CSHA.

Some high-performance fully-differential CSHA circuits for switched-current (SI) filter applications have been reported [11], [13], [15]. However, there are some difficulties in applying these CSHA circuits to meet the above requirements simultaneously. The CSHA circuit depicted in Fig. 6 [27], [28] can satisfy the aforementioned requirements without imposing stringent matching requirements on the input characteristics of CCMP and CSHA. To sample the input current, the switch S is turned on and S_d is turned off. If zero common-mode component presents at the inputs I_{i+} and I_{i-}, the voltage at the common source node of P1 and P2 which is connected to the gate nodes of P3 and P4 ideally remains at the quiescent value. The currents of P3 and P4 thus only offer the dc bias currents J at this time. If nonzero common-mode component i_{cm} presents at the inputs, it can be detected at the common source node of P1 and P2 which can adjust the currents of P3 and P4 to be $(J - i_{\text{cm}})$. Consequently, the common-mode component i_{cm} can thus be taken away from the inputs by the upper PMOS branches consisting of (P3, P5) on the left and (P4, P6) on the right. The differential part of the input currents are detected at the gate-drain shorted nodes of N1 and N2 which can adjust the currents of N3 and N4 to be $(J + i_d)$ and $(J - i_d)$, respectively.

In the output branches, the gate of P7 (P8) is connected to the fixed bias V_{cm} which is designed to have the current of P7

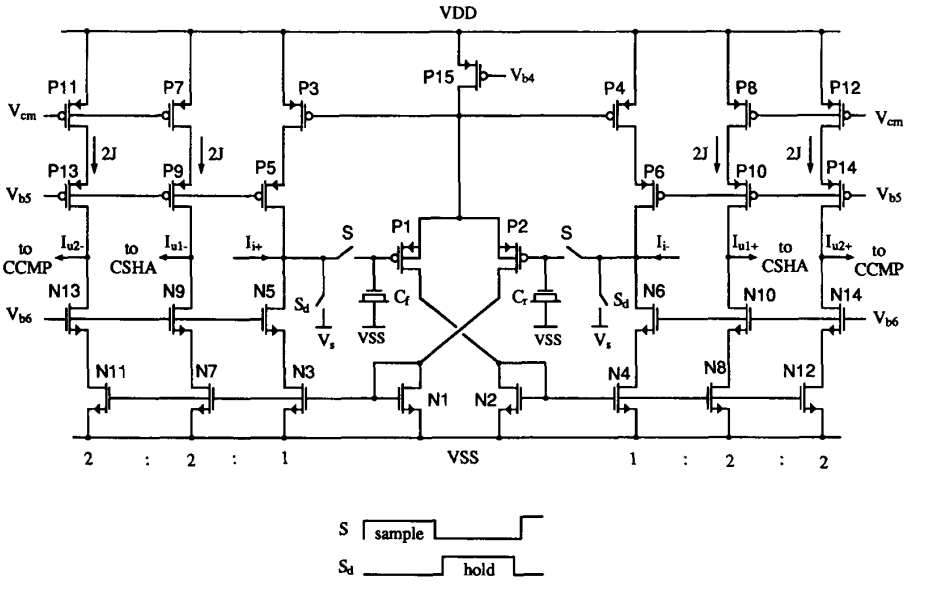

Fig. 6. The fully differential CSHA used in the proposed IADC.

(P8) equal to the bias current $2J$ with the current gain of 2. Note that J is the bias current for the input branches provided by P3 (P4) when zero common-mode component presents at the inputs. As a result, the common-mode part of the inputs no longer presents at the outputs because it is not mirrored to the outputs. Since the gates of N7 (N8) and N3 (N4) are connected together, the differential part $i_d(-i_d)$ is inverted and mirrored to the output $I_{u1-}(I_{u1+})$. The circuit is then switched to the hold mode by turning off the switch S. By the charges stored at the gate node of P1 (P2), the output currents is therefore held. Note that the switch S_d is turned on after the turn-off of S to bypass the input currents to a fixed voltage V_s in the hold mode.

The output resistance of the CSHA is large due to the cascode structure. The circuit also provides a better isolation for the charge holding nodes from the output nodes. This also makes the design of the CCMP more easily because it is not necessary to lower down the CCMP input impedance using the feedback techniques. The required differential current gains of 2 can be obtained by scaling the device sizes in the output branches as shown in Fig. 6. Besides the outputs I_{u1+} and I_{u1-} to drive the CSHA of the next stage, the outputs required to drive the next stage CCMP are also obtained by simply adding the additional output current mirrors (N11–N14 and P11–P14). Since the current gains are determined by the sizing ratios of neighboring transistors, precision layout strategies must be used for these mirror transistors to reduce the mismatch errors. In the layout of the CSHA circuit, each of the nominally unity-sized transistors (e.g., N3 or P3) shown in Fig. 6 is actually broken into 4 smaller-sized transistors to reduce the errors caused by the systematic edge effects [12], [19]. In addition, these unity transistors are arranged to form the common-centroidal configuration so that the linear process gradient errors can be reduced [12], [19]. Moreover, although the 0.8-μm CMOS process is used, the channel length of the current-mirror transistors in the CSHA is designed to be 6 μm to reduce the mismatch errors. The use of long-channel current-mirror devices leads to lower conversion rate and the increase of chip area. The bandwidth of the CSHA can be further improved by using transistors with shorter channel length but at the cost of reduced matching accuracy. Therefore, the trade-off between the operating speed, chip area, power consumption, and matching accuracy is required.

Owing to the fully-differential configuration, the common-mode clock feedthrough errors can be canceled. However, the differential part of the clock feedthrough errors are not canceled. Therefore, half-sized dummy devices are added to the sampling switches to lower down the differential-mode clock feedthrough errors.

The settling behavior during the sample mode can be analyzed by the equivalent small-signal half circuit. It can be shown that if the following expression is satisfied, a phase margin of 60° can be obtained,

$$\frac{C_i}{C_L} \approx 1.5\left(\frac{g_{m,P1}}{g_{m,N1}}\right)\left(\frac{g_{m,N3}}{g_{m,N1}}\right) \tag{5}$$

where C_i and C_L are the capacitances at the gate nodes of P1 (P2) and N1 (N2), respectively, and $g_{m,P1}, g_{m,N3}$, and $g_{m,N1}$ are the transconductances of the transistors P1 (P2), N3 (N4), and N1 (N2), respectively. In this design, $(g_{m,P1}/g_{m,N1}) \approx 1$ and $(g_{m,N3}/g_{m,N1}) \approx 1$, thus (5) can be simplified as $C_i \approx 1.5C_L$. Therefore, the CSHA can be stabilized without significantly reducing the bandwidth. The capacitors C_f and C_r formed by NMOS devices as shown in Fig. 6 are added to get a good settling behavior. Note that the addition of these two capacitors also helps to reduce the clock feedthrough errors and thermal noises. Simulation results show

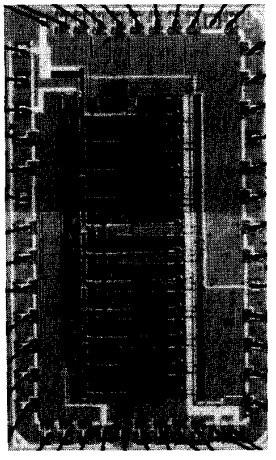

Fig. 7. The photograph of the test chip.

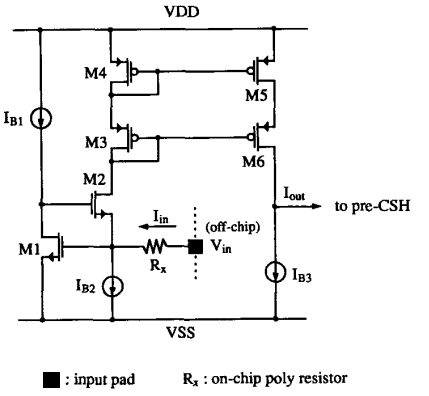

Fig. 8. The on-chip V–I conversion interface circuit to convert the external voltage signals into internal current signals.

that the 0.1% settling time for the CSHA to make a 260 μA step transition is 100 ns when operated in the sample mode. The CSHA circuit with power consumption of 6.3 mW is also one of the major power consuming blocks of the IADC.

V. Experimental Results

The proposed IADC was fabricated in a 0.8-μm double-poly double-metal N-well CMOS process. Though the process offers the double-poly linear capacitor, it was not used in this test chip. Thus, the IADC is equivalently fabricated by a digital process. The photograph of the experimental chip is shown in Fig. 7. For the testing purpose, the chip was laid out to contain 10 pipelined stages (10 output bits) so that the performance limits of the developed circuits can be measured. The chip also contains the digital shift registers, output buffers, input clock buffers, and the input V–I converting circuits. Due to the pipelined configuration, an adequate number of digital shift registers must be added to each pipeline stage so that the digital outputs can be time-aligned for each analog input sample. The fabricated IADC requires two external nonoverlap clocks. The other clock waveforms are on-chip generated from the two nonoverlap external clocks.

A. Input V–I Conversion Interface

Because the available instruments for the input signal sources are mostly in the voltage domain, the V–I conversion interface is required to test the chip. In this test chip, an on-chip linear V–I conversion circuit using current conveying techniques is employed to alleviate this limitation. The circuit diagram of the V–I conversion interface is shown in Fig. 8. The circuit consists of an on-chip poly resistors R_x and a current conveyor [17] to convey the current flowing through R_x to the output. The transistors M2–M6 and the bias currents I_{B2}-I_{B3} form the current conveyor. The transistor M_2 acts as the current conveying device. The transistor M_1 and the active load I_{B1} form an inverting voltage amplifier to lower down the input resistance of the conveyor by the negative feedback. The transistors M3–M6 form the cascode current mirrors so that the current flowing through M_2 is mirrored to the output while with a high output resistance. HSPICE simulation results show that the −3 dB bandwidth of the V–I converting circuit is 20 MHz which is much higher than that of the fabricated IADC. Therefore, the bandwidth of the V–I converting circuit has negligible effect on the measurement of the bandwidth of the IADC.

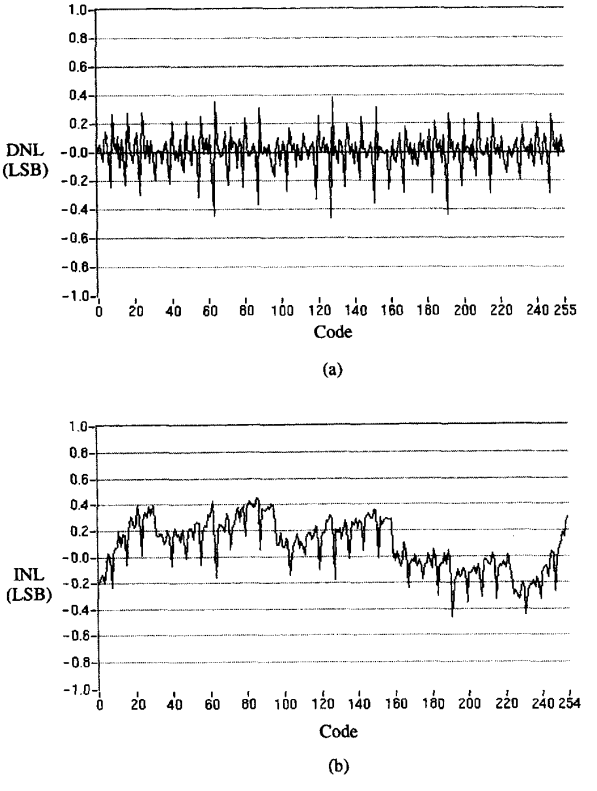

Fig. 9. The measured (a) DNL and (b) INL for 8-b resolution at 3.8 Ms/s conversion rate.

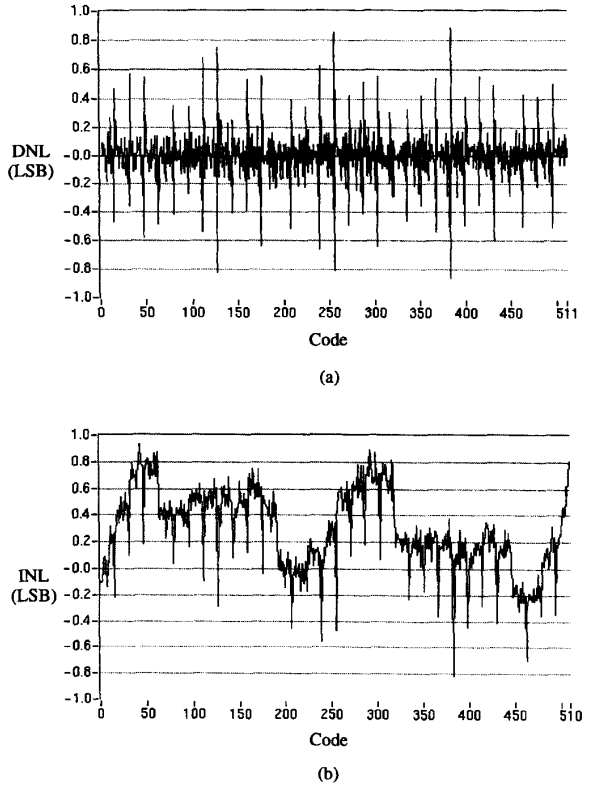

Fig. 10. The measured (a) DNL and (b) INL for 9-b resolution at 3.6 Ms/s conversion rate.

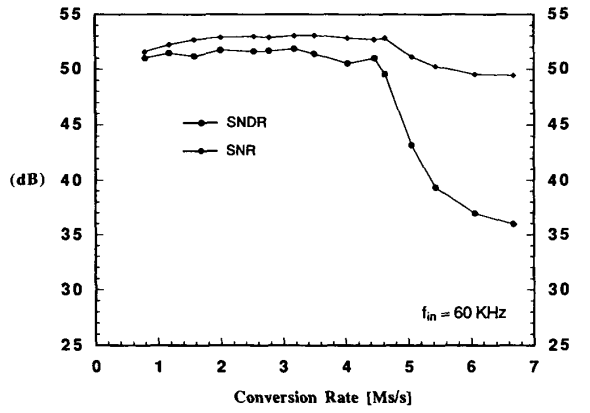

Fig. 11. The measured SNR and SNDR versus the conversion rate of the fabricated IADC for 60 kHz analog input.

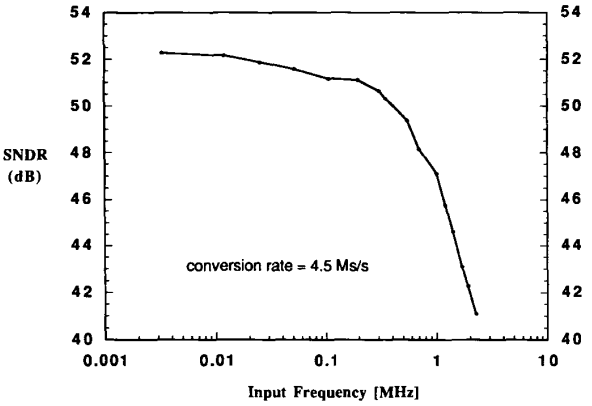

Fig. 12. The measured SNDR versus the analog input frequency of the fabricated IADC at 4.5 Ms/s conversion rate.

B. Linearity Test

The sine-wave-based histogram algorithm is used to measure the linearity of the converter. Fig. 9 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) plot for 8-b resolution (with 8 output bits) when the fabricated IADC is operated at 3.8 Ms/s conversion rate. The DNL and the INL for all codes are less than $+/-0.5$ LSB. When the conversion rate is increased to 4.5 Ms/s, the worst DNL becomes $+/-0.6$ LSB at the major carry and the two submajor carries. The DNL for all other codes is still within $+/-0.4$ LSB. The INL is still within $+/-0.6$ LSB for all codes. Fig. 10 shows the DNL and INL plots for 9-b resolution (with 9 output bits) at 3.6 Ms/s conversion rate. The INL for all codes is within $+/-0.9$ LSB. Since the DNL never goes down to -1 LSB, there are no missing codes. The DNL for most codes are within $+/-0.6$ LSB and the worst cases of DNL are -0.85 LSB and 0.9 LSB.

C. Dynamic Test by FFT

Signal-to-noise-ratio (SNR), signal-to-noise-and-distortion (SNDR), and total-harmonic-distortion (THD) are measured by taking the fast Fourier transform (FFT) on 4096 samples from the output codes (with 9 output bits) of the IADC. The measured SNR and SNDR versus conversion rate are plotted in Fig. 11 where the analog input frequency is kept constant at 60 kHz. It can be seen that the measured SNDR is kept at about 52 dB (effective 8.3 b) when the conversion frequency is below 4.5 Ms/s and starts to decrease rapidly as the conversion rate is increased beyond 4.5 Ms/s. However, the SNR is still above 49 dB when the conversion rate is at 6.7 Ms/s. The degradation of SNDR at the higher conversion rate is mainly caused by the increase in the THD. The high SNR at high conversion rate is achieved by the fully-differential circuit configurations.

Fig. 12 shows the measured SNDR versus the analog input frequency for a full-scaled sinusoidal input digitized at 4.5 Ms/s. It can be seen that the SNDR at low frequency is 52 dB. Then it begins to decrease at about 500 kHz and becomes 42 dB at 2 MHz. The degradation of SNDR at high input frequencies is due to the bandwidth limitation of the CSHA. Two plots of the measured SNDR versus the analog input level for two input signal frequencies, 10 kHz and 100 kHz, at 4.5 Ms/s conversion rate are shown in Fig. 13. For the 10-kHz input, the peak SNDR is about 52 dB. The plot of the 100-kHz input is very similar to that of the 10-kHz input without significant degradation except that the peak SNDR is reduced to about 51 dB. Fig. 14 shows the measured FFT

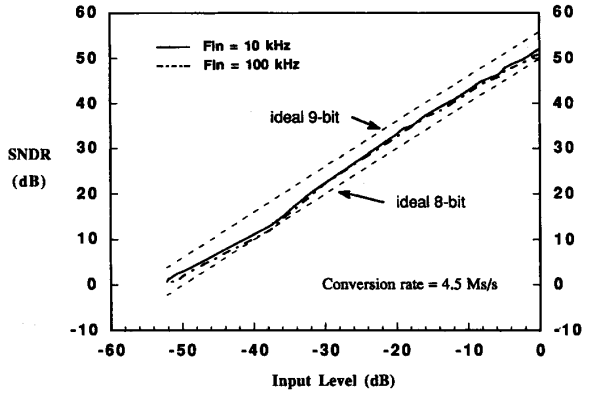

Fig. 13. The measured SNDR versus analog input levels of the fabricated IADC at 4.5 Ms/s conversion rate.

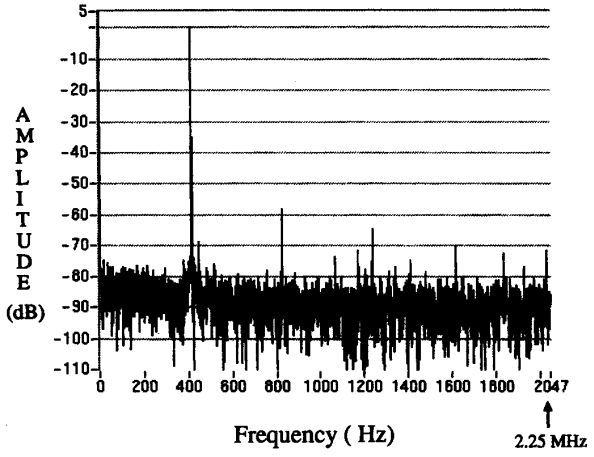

Fig. 14. The measured FFT spectrum of the fabricated IADC for a 453 kHz sinewave sampled at 4.5 Ms/s conversion rate.

spectrum of a 453 kHz sinusoidal input with the fabricated IADC operated at 4.5 Ms/s conversion rate. The SNR and THD are 51 dB and −57 dB, respectively. Theoretically, the even harmonics should be reduced significantly by the fully differential configuration. However, in the measured data, the second harmonic is still the dominant term for the THD. This is because the input V–I converting circuit is of single-ended configuration, and thus the even harmonics might be generated in the V–I conversion.

Table II gives a summary of the measured characteristics of the fabricated IADC. Owing to the pipelined architecture, the input capacitance is 6 pF which is much smaller than that of the fully-parallel A/D converters (28 pF for 8-b resolution) [24]. The chip area (excluding the I/O pads) for the 10-b layout is 7.3 mm^2 and the power consumption is 160 mW. The active area and power consumption for each bit is thus 0.73 mm^2 and 16 mW, respectively.

VI. Conclusion

New fully-differential current-mode circuits are proposed to design a pipelined IADC in the standard CMOS digital technology with more than 8-b resolution at 4.5 Ms/s conversion rate. The proposed IADC has been experimentally verified by a test chip fabricated by 0.8-μm CMOS technology. The achievable accuracy is limited by the clock feedthrough errors and the mismatches of MOS transistors. The operating speed is limited by the bandwidth of the CSHA circuit.

TABLE II
Measured IADC Characteristics

Technology	0.8-um CMOS
SNDR (f_{ck} = 4.5 Ms/s)	51 dB (f_{in} = 200 KHz)
	47 dB (f_{in} = 1 MHz)
DNL	-0.5 LSB ~ 0.5 LSB (8-b, f_{ck} = 3.8 Ms/s)
	-0.6 LSB ~ 0.6 LSB (8-b, f_{ck} = 4.5 Ms/s)
	-0.9 LSB ~ 0.9 LSB (9-b, f_{ck} = 3.6 Ms/s)
INL	-0.5 LSB ~ 0.5 LSB (8-b, f_{ck} = 3.8 Ms/s)
	-0.6 LSB ~ 0.6 LSB (8-b, f_{ck} = 4.5 Ms/s)
	-0.9 LSB ~ 0.9 LSB (9-b, f_{ck} = 3.6 Ms/s)
Input Bandwidth (-3 dB)	640 kHz (f_{ck} = 4.5 Ms/s)
Full Scale Current	260 uA
Input Capacitance	6 pF *
Power Supply	single 5 V
Active Area	0.73 mm^2/bit
Power Consumption	16 mW/bit

* simulation data

Acknowledgment

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