Universal Switched-Current Integrator Blocks for SI Filter Design

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Abstract- The switched-current (SI) circuit is a circuit technique which is able to realize analog sampled-data circuits with a standard CMOS technology. Among all the basic SI circuits, the memory cell circuit is the most primitive element. In this work, a practical SI memory cell which employs negative feedback circuitry and glitch reduction technique is first presented. Based on this basic cell, a universal SI integrator is then developed. General first and second order building blocks are subsequently developed for the cascade design of SI filters. These general building blocks can be used to generate all types of first and second order filters. To verify the accuracy of the SI circuits, test filters including a first order low-pass filter, a second order Chebyshev low-pass filter, and a fifth order Chebyshev low-pass filters have been designed and verified with HSPICE. The simulation results of the frequency response characteristics show good agreement with the theoretical results.

1. Introduction

Switched-current (SI) circuits have recently been introduced as an alternative circuit approach to switched-capacitor (SC) circuits. The most basic building block of the SI technique is the current memory cell [1] which is used to construct the integrator, differentiator, delay line, etc. The analog performance of the SI systems arises directly from the errors of its constituent memory cells. The measured responses of the corresponding SI systems often exhibit large errors. The deviations are caused by several factors such as MOSFET mismatches, switch charge injection [2,3], and channel-length modulation effect [4]. To improve the accuracy, a high-performance SI memory cell which employs active negative feedback [6] and glitch reduction technique is presented. In order to realize cascade filters, a universal SI integrator is subsequently developed to construct general first and second order SI building blocks. To verify the circuit technique, typical filter circuits have been designed and simulated. All simulated results agree closely with the theoretical responses.

2. A New Switched-Current Memory Cell

The basic element of the switched-current (SI) technique is the SI memory cell. To achieve better performance, a practical memory cell is presented as shown in Fig. 1. The grounded-gate voltage amplifier used here comprises the grounded-gate transistor M_G and two current sources each providing a bias current J. The PMOS transistor M_P with its gate biased at the voltage V_{ref} passes its drain current equal to I. During phase ϕ_2, both S_1 and S_2 are closed, the signal current i flows into the source of transistor M_G and charges the storage capacitor C. When the current in M_T reaches I+i and the current in M_G returns to J, equilibrium is established, and the voltage at the summing node A is close to a constant value $V_{in} = V_{bias} + V_{gs}$, where v_{gs} is the gate-source voltage of M_G with its drain current equal to J. During phase ϕ_1, S_3 is closed. The output current i_o flows into next cascaded connected cell, and the output voltage of the driving cell is fixed at the input node of the driven cell. Since the output node is held close to V_{in}, the memory transistor M_T sustains its current at I+i and gives an output i_o equal to -i. The grounded-gate amplifier creates a "virtual earth" at the input node [6] (and the output node while connecting to the next cascaded cell). In Fig. 2, a fully differential version of the memory cell is illiustrated. To minimize the error current generated into the storage node due to loading effect, high-performance regulated-gate cascode current sources [7] are adopted. The feedback connection to the transistors M_{CMFB1} and M_{CMFB2} provides overall common-mode stability. For glitch reduction, two additional switches S_{dx1} and S_{dx2} are employed to minimize the deviation of signals due to transient glitches. During the non-overlapped period of the clock, both S_{dx1} and S_{dx2} are turned on, and the difference of the drain currents between M_P and M_T is sinked or sourced by the constant voltage source V_{ref}. During the output phase ϕ_1, the switches remain close for a short time to stabilize the output voltage. This can effectively eliminate the unbalance of the drain currents of M_P and M_T during the non-overlapped period thus reduce the glitches at the moment of either ϕ_1 or ϕ_2 goes high.

3. A Universal Switched-Current Integrator

A universal SI integrator which performs an identical algorithm to a well known switched-capacitor universal integrator is presented [9]. This switched-current universal integrator are duals of those already used in active-RC and switched-capacitor systems. Fig. 3 shows the configuration of the SI universal integrator and the associated circuit is given in Fig. 4. Although identical circuit topology is adopted with respect to that in [9], the presented integrator uses a high-quality meomory cell and has better analog performance. The input currents weighted α_1, α_2 and α_3 are accomplished by scaling the aspect ratios (W/L) of the corresponding output transistors and the output stage has unit weight. As derived in [9], the current equation is given as

$$i_o(z) = \frac{A_1 z^{-1}}{1 - Bz^{-1}} \cdot i_1(z) - \frac{A_2}{1 - Bz^{-1}} \cdot i_2(z) - \frac{A_3(1 - z^{-1})}{1 - Bz^{-1}} \cdot i_3(z) \quad (1)$$

where $A_1 = \alpha_1/(1 + \alpha_4)$, $A_2 = \alpha_2/(1 + \alpha_4)$, $A_3 = \alpha_3/(1 + \alpha_4)$, and $B = 1/(1 + \alpha_4)$.

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4. General First and Second Order Building Blocks

A. General First-order Building Blocks

The general continuous-time first-order transfer function is given by

$$H(s) = \frac{a_1 s + a_0}{s + \omega_0} \quad (2)$$

The numerator coefficients, a_0 and a_1, determine the type of filter (e.g., low-pass, high pass, and all-pass). Using the bilinear transformation ($s = (2/T)(1 - z^{-1})/(1 + z^{-1})$) in Eq. (2) gives the z-domain transfer function:

$$H(z) = \left(\frac{2a_1 + a_0T}{2 + \omega_0T}\right) \frac{1 - \left(\frac{2a_1 - a_0T}{2a_1 + a_0T}\right)z^{-1}}{1 - \left(\frac{2 - \omega_0T}{2 + \omega_0T}\right)z^{-1}}$$

$$= K \cdot \frac{1 - \alpha z^{-1}}{1 - \beta z^{-1}} \quad (3)$$

where $K = (2a_1+a_0T)/(2\omega_0T)$, $\alpha = (2a_1-a_0T)/(2a_1+a_0T)$, and $\beta = (2-\omega_0T)/(2+\omega_0T)$. Consider the universal SI integrator in Fig. 3. If $2a_1 - a_0T \geq 0$, $\alpha \geq 0$, by setting $i_1 = i_2 = -i$, and $i_3 = 0$, the z-domain transfer function becomes,

$$H(z) = \frac{i_o(z)}{i(z)} = \frac{A_2 - A_1 z^{-1}}{1 - Bz^{-1}}. \quad (4)$$

Comparison between Eqs. (3) and (4) yields

$$A_1 = \frac{\alpha_1}{1 + \alpha_4} = \alpha K,\ A_2 = \frac{\alpha_2}{1 + \alpha_4} = K, \text{and } B = \frac{1}{1 + \alpha_4} = \beta \quad (5)$$

If $2a_1 - a_0T < 0$, $\alpha < 0$, by setting $i_1 = -i_2 = i$, and $i_3 = 0$, the z-domain transfer function becomes,

$$H(z) = \frac{i_o(z)}{i(z)} = \frac{A_2 + A_1 z^{-1}}{1 - Bz^{-1}} \quad (6)$$

where $A_1 = -\alpha K$, A_2 and B are as defined in Eq. (6). The z-domain transfer functions of Eqs. (4) and (6) thus correspond to those of the general first-order building blocks. Figure 5 shows the general first-order section configuration made of the universal SI circuit.

B. General Second-order Building Blocks

The general biquadratic transfer function is given by

$$H(z) = \frac{i_o(z)}{i(z)} = \frac{(a_5 + a_6) + (a_1a_3 - a_5 - 2a_6)z^{-1} + a_6z^{-2}}{(1 + a_4) + (a_2a_3 - a_4 - 2)z^{-1} + 1} \quad (7)$$

with the building block given in Fig. 6. Also, the coefficients associated with every types of filters are summarized in Table 1.

C. Performance Verification

To verify the operation of the proposed first-order and second-order blocks, a first-order low pass filter and a second order 0.5-dB ripple Chebyshev low-pass filter are relaized respectively. For the first-order LP filter with DC gain=1, 3dB frequency f_0= 1MHz, its magnitude response is plotted in Fig. 7.

For the second-order LP filter, the specifications of the simulated SI filter are given in the sampled-data domain: the ripple bandwidth f_p = 500 kHz and the sampling frequency f_{clk} = 5 MHz. Figure 8 shows the theoretical magnitude response and the simulation result with HSPICE. It can be seen that the simulated response agrees closely with the theoretical one for both cases.

5. Case Study: A Cascade Design Example

To show a design example, a fifth-order 1 dB-ripple Cheby- shev low-pass filter is realized by cascading two biquadratic and one first-order sections. The specification of this test filter are given in the sampled-data domain: the ripple frequency f_p = 500 kHz and the sampling frequency f_{clk} = 5 MHz. Following the precedure described in Section 4, the weights of the constituent sections can be determined. Theoretical and simulated magnitude responses of the filter is plotted in Fig. 9. It can be seen that the simulation result of the frequency response characteristics is in close agreement with the theoretical result.

In conclusion, a high-performance SI memory cell circuit has first been presented. This memory cell circuit utilizes active negative feedback to improve transmission accuracy. Fully differential structures with common-mode feedback are used to reduce charge injection errors. Furthermore, additional glitch reduction switches are employed to improve transient behavior. Based on the proposed cell circuit, a universal SI integrator has been generated which performs an identical algorithm to a well known SC general integrator. General first and second order building blocks which correspond to the bilinear s-z transformation of the general continuous-time first and second order section have been developed from the universal SI integrator. These building blocks are used for designing cascade SI filters. To verify the circuit technique, test filters including a first order low-pass filter, a second order Chebyshev low-pass filter, and a fifth-order Chebyshev low-pass filters have been realized and simulated with HSPICE. The simulation results of the frequency response characteristics show pretty good agreement with the theoretical results.

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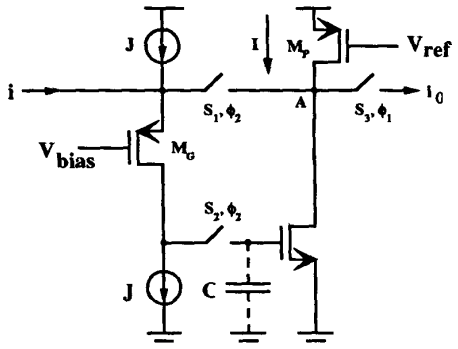
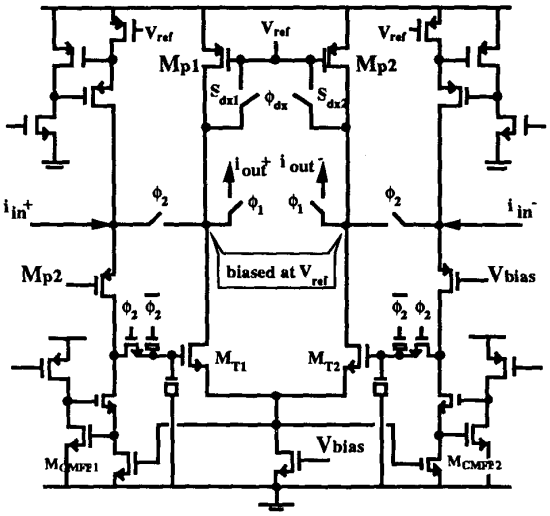
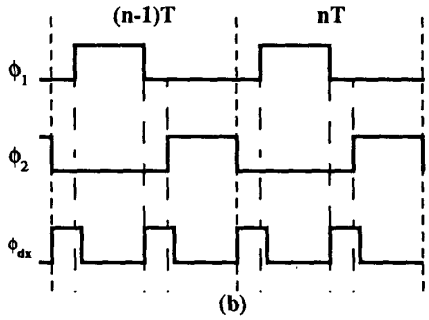


Fig. 1 A practical memory cell



(a)



(b)

Fig. 2 (a) A fully-differential memory cell.
(b) The associated control signals.

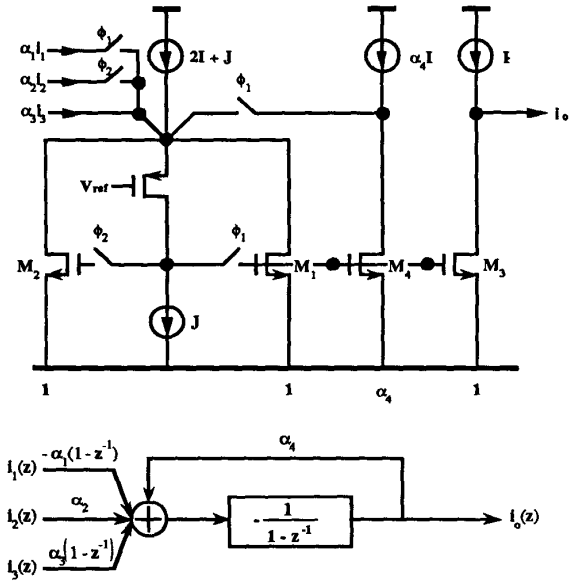


Fig. 3 Configuration of the SI universal integrator.

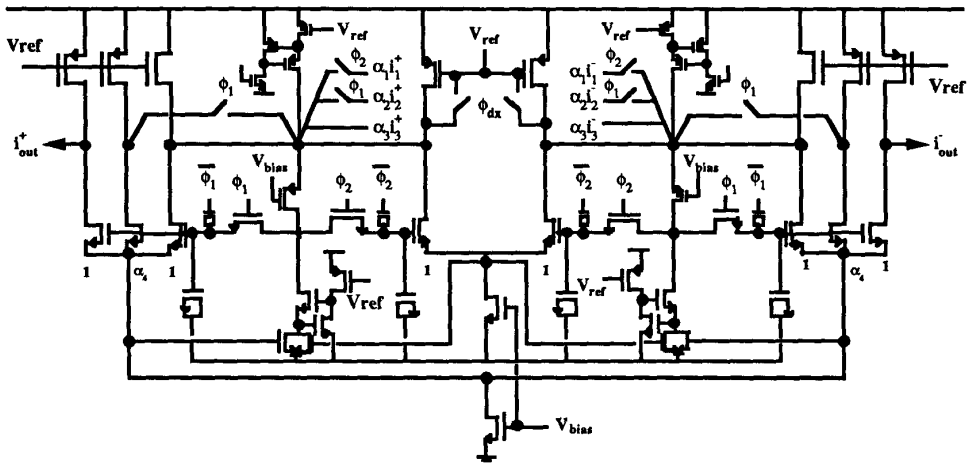


Fig.4 A fully-differential circuit of Fig.3.

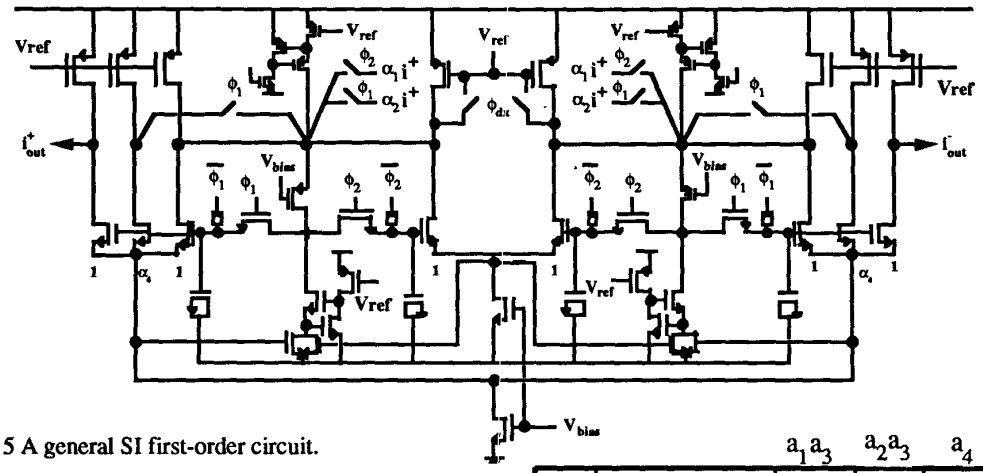


Fig. 5 A general SI first-order circuit.

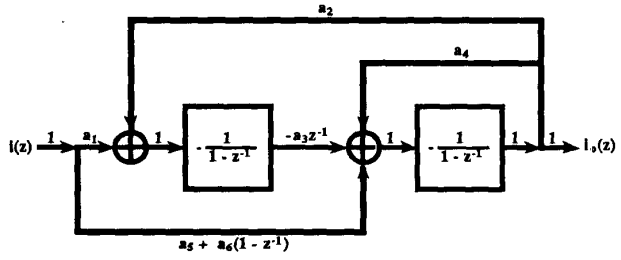


Fig. 6 A general second-order building block.

		a_1a_3	a_2a_3	a_4	a_5	a_6
Low-Pass	$H(s) = -\frac{k_0\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	$\frac{4k_0\omega_0^2T^2}{D}$	$\frac{4\omega_0^2T^2}{D}$	$\frac{4\omega_0T}{QD}$	0	$\frac{k_0\omega_0^2T^2}{D}$
High-Pass	$H(s) = -\frac{k_0s^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	0	$\frac{4\omega_0^2T^2}{D}$	$\frac{4\omega_0T}{QD}$	0	$\frac{4k_0}{D}$
Band-Pass	$H(s) = -\frac{k_0\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	0	$\frac{4\omega_0^2T^2}{D}$	$\frac{4\omega_0T}{QD}$	$\frac{4k_0\omega_0T}{QD}$	$\frac{-2k_0\omega_0T}{QD}$
Band-Reject	$H(s) = -\frac{k_0(s^2 + \omega_0^2)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	$\frac{4k_0\omega_0^2T^2}{D}$	$\frac{4\omega_0^2T^2}{D}$	$\frac{4\omega_0T}{QD}$	0	$\frac{4k_0 + k_0\omega_0^2T^2}{D}$
All-Pass	$H(s) = -k_0\frac{s^2 - \frac{\omega_0}{Q}s + \omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$	$\frac{4k_0\omega_0^2T^2}{D}$	$\frac{4\omega_0^2T^2}{D}$	$\frac{4\omega_0T}{QD}$	$\frac{-4k_0\omega_0T}{QD}$	$\frac{(4k_0 + 2k_0\omega_0T/Q + k_0\omega_0^2T^2)/D}$

$D = \omega_0^2T^2 - \frac{2\omega_0T}{Q_0} + 4$

Table 1 Coefficients for various types of filters based on the second-order block in Fig. 6.

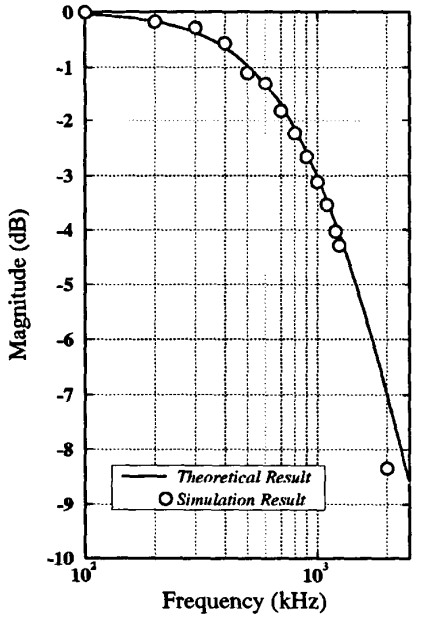


Fig. 7 Magnitude response of a first-order low pass filter.

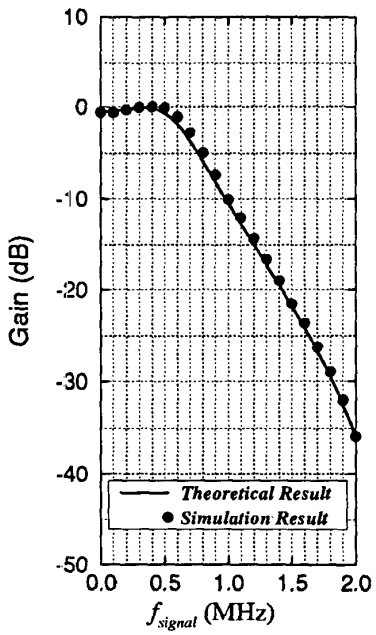


Fig. 8 Magnitude response of a second-order Chebyshev low pass filter.

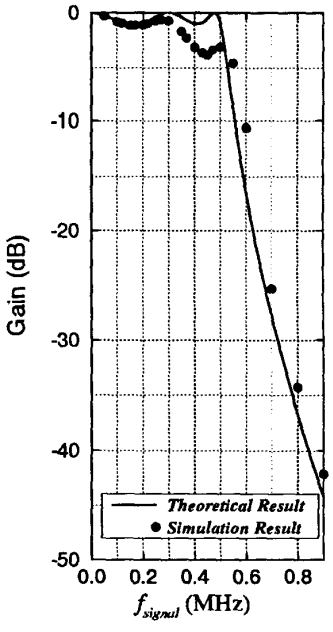


Fig. 9 Magnitude response of a fifth-order Chebyshev low pass filter.