Weak Inversion Charge Injection in Analog MOS Switches

Ming-Jer Chen, Yen-Bin Gu, Terry Wu, Po-Chin Hsu, and Tsung-Hann Liu

Abstract— **The on-chip test circuit for examining the charge injection in analog MOS switches has been described in detail, and has been fabricated and characterized. Mixed-mode circuit and device simulations have been performed, creating excellent agreements not only with the experimental waveforms but also with the measured switch-induced error voltage. Further investigation of the experimental and simulated results has separated the charge injection into three distinct components: i) the channel charges in strong inversion; ii) the channel charges in weak inversion; and iii) the charges coupled through the gate-to-diffusion overlap capacitance. Important observations concerning the weak inversion charge injection have been drawn from the waveform of the current through the switched capacitor. In this work the channel charges in weak inversion have exhibited a 20% contribution to the switch-induced error voltage on a switched capacitor.**

I. Introduction

THE MOS transistor analog switch is one of the major building blocks for the switched-capacitor circuits [1]. One of the fundamental factors limiting the accuracy of the switched-capacitor circuits is the charge injection occurring when the MOS transistor turns off [2]. An understanding of the charge injection phenomenon in analog MOS switches as well as its control is very important for the switched-capacitor circuits. Several compensation techniques such as dummy transistor [2] and Miller hold capacitance [3] have been developed for suppression of the charge injection. Analysis and modeling of charge injection due to channel charges in strong inversion and feedthrough charges via gate-to-diffusion overlap capacitance have also been extensively studied [4]–[8]. Very recently, a new charge injection component due to channel charges in weak inversion has been observed [9].

In this paper we will report detailed investigation of the charge injection due to channel charges in weak inversion not only from the experimental analog MOS switch but also from the mixed-mode circuit and device simulation. The experimental test circuit will be completely described. A comparison of the experimental and simulated results will be given. We will demonstrate how to draw important observations concerning the weak inversion charge injection from the waveform of the current through the switched capacitor. The impact of channel charges in weak inversion on the switch-induced error voltage will also be addressed.

Manuscript received July 15, 1994; revised November 7, 1994. This work was supported by the National Science Council under Contract NSC 83-0404-E-009-087.

M.-J. Chen and Y.-B. Gu are with the Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsin-Chu 300, Taiwan, Republic of China.

T. Wu, P.-C. Hsu, and T.-H. Liu are with the Mixed-Mode Integrated Circuits Department, Electronics Research & Service Organization/ITRI, Hsin-Chu 300, Taiwan, Republic of China.

IEEE Log Number 9410177.

II. Experiment versus Simulation

A. Test Circuit

The on-chip test circuit, fabricated by a 1.2 μm double-metal double-polysilicon twin-well CMOS process, consists of an n-channel MOS transistor with gate width to length ratio of 25 μm/5 μm, a holding capacitance of 1.0 pF, and a unity-gain operational amplifier. The circuit is schematically shown in detail in Fig. 1, where the photograph of the test chip is also given. In our work the unity-gain operational amplifier, which is a key subblock determining the ability of measuring the charge injection, follows that cited in [3]. SPICE simulations have exhibited that with the device sizes in unit of μm/μm as labeled in Fig. 1 for the unity-gain operational amplifier, the test circuit has a linear transfer characteristic, i.e., $V_{\text{out}} = V'_{\text{out}}$ only for input voltage V_{in} ranging from 1 to 2.5 V, in agreement with that reported experimentally in [3]. Our measurement results have judged that outside of this range the precise measurement is impossible to achieve. Therefore, under the condition of V_{in} ranging from 1 to 2.5 V, not only the designed unity-gain operational amplifier can be utilized as a buffer, but also the voltage waveform on the holding capacitor can be represented by that at the output of the test circuit.

The test circuit has been mounted on a plastic 24-pin package, which has been inserted into the printed-circuit board specially designed for suppression of oscillation and noise interference. The measurement equipments and conditions are: i) Keithley 236 source-monitor unit to offer the dc input voltage V_{in}; ii) HP 8115 A pulse generator to offer the gate voltage waveform $V_G(t)$ with high-level $V_H = 5$ V and low-level $V_L = 0$ V, with pulse width of 100 μs, and with fall time ranging from 50 ns to 5 μs; and iii) Tektronix 11402 A storage digitizing oscilloscope for observing and recording the waveforms at the gate and the output. Tektronix 11402 A also provides the capability of creating the waveform of the current $I_D(t)$ through the holding capacitance by differentiating the output voltage waveform with respect to time and multiplying it by the $C_H(= 1.0$ pF) value.

B. Mixed-Mode Simulation

The mixed-mode circuit and device simulations by utilizing the program MEDICI [10] have been performed on the MOS switch in Fig. 1 with $C_H = 1.0$ pF. The MOS transistor structure with the same gate width to length ratio of 25 μm/5 μm has been created from the process parameters available from the foundry: the gate oxide thickness is about 250 Å; the gate-to-diffusion overlap capacitance is 7.76 fF; and the junction depth and surface doping concentration of the p-well are about 3.0 μm and 6.0×10^{16} cm^{-3}, respectively. In such simulations, both the Kirchhoff equations and the two-

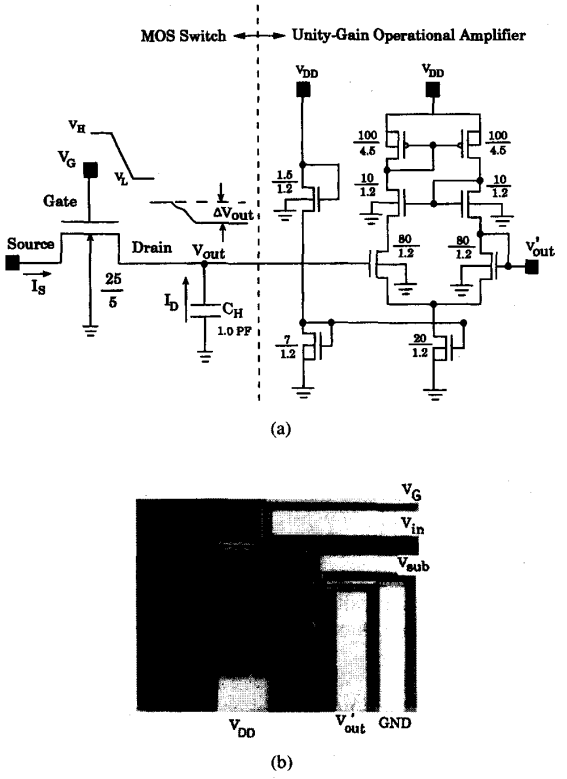


Fig. 1. (a) The detailed description of the test circuit for measuring the charge injection; and (b) the photograph of the test chip. $V_{\text{sub}} = 0$ V. ΔV_{out} is the error voltage and C_H is the holding capacitance.

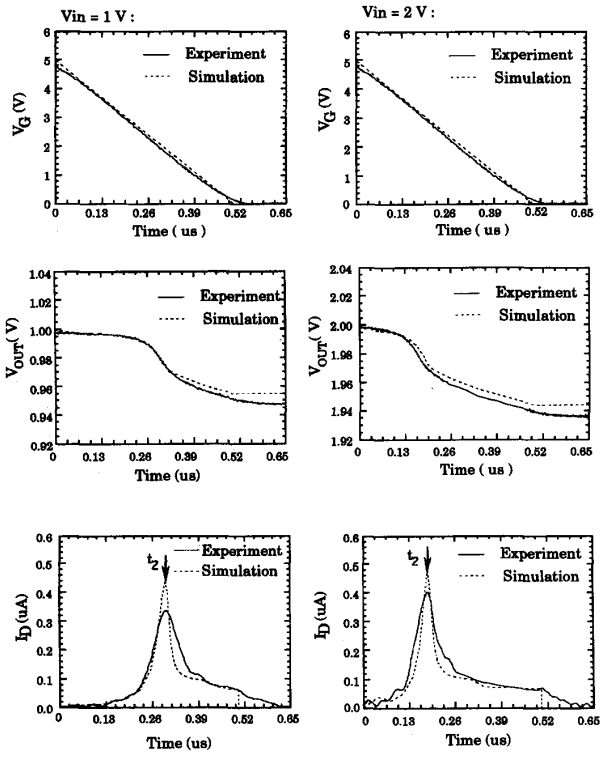


Fig. 2. The comparison of the measured and simulated waveforms for $V_{\text{in}} = 1$ V and 2 V. t_2 represents the time for the gate voltage reaching the threshold. $t_1 = 0$ and $t_3 = 500$ ns, i.e., $t_f = 500$ ns.

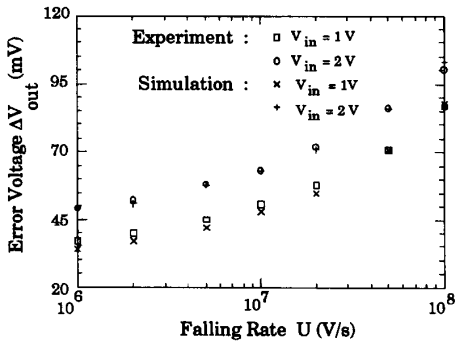
dimensional semiconductor equations are solved as a coupled set. The simulation conditions are: i) the ramp gate voltage waveform $V_G(t)$ in the turn-off duration is represented by $V_G(t) = V_H - (V_H - V_L)(t - t_1)/t_f$ for $t_1 < t < t_3 (= t_1 + t_f)$ where $V_H = 5$ V; $V_L = 0$ V; t_1 is the time for the gate voltage starting to drop; and the fall time t_f is a variable ranging from 50 ns to 5 μs; and ii) the dc V_{in} ranges from 1 to 2 V.

C. Results and Comparison

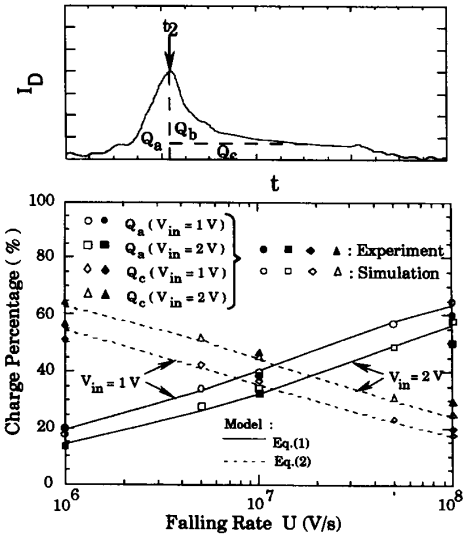
Fig. 2 depicts the measured voltage waveforms at the gate and the output as well as the waveform of the current through the holding capacitance for two different input voltages of 1 and 2 V at a fixed fall time of 500 ns. The corresponding simulated results are also demonstrated together in Fig. 2. From Fig. 2 we can see that the simulated voltage and current waveforms reasonably match the measured ones and thus the waveforms measured from the test circuit can be appropriately reproduced by mixed-mode simulation. The validity of the mixed-mode simulation work can further be testified by comparing the measured results in terms of both the switch-induced error voltage and the charge percentage as functions of the falling rate $U (= (V_H - V_L)/t_f)$ for two different input voltages as depicted in Fig. 3. From Fig. 3 we can observe that the mixed-mode simulation can provide excellent agreement with the experimental data. Therefore, the mixed-mode circuit and device simulations can be properly utilized to examine the charge injection phenomenon.

III. Weak Inversion Charge Injection

Here we demonstrate how to obtain a clear understanding of the charge injection phenomenon including the channel charges in weak inversion by observing the waveform of the current through the switched capacitor as depicted in Fig. 2. According to [4], the turn off of an MOS switch consists of two distinct phases: $t_1 < t < t_2$ and $t_2 < t < t_3 (= t_1 + t_f)$. Here t_2, as labeled in Fig. 2, represents the time for the gate voltage $V_G(t)$ reaching the sum of the input voltage V_{in} and the threshold voltage V_{th}, i.e., $V_G(t_2) = V_{\text{in}} + V_{\text{th}}$. Note that an increase in V_{in} also causes an increase in the threshold voltage V_{th} due to back-gate bias effect, together constituting the increase in the duration of the second phase as clearly reflected in Fig. 2. During the first phase, some of the channel mobile charges in strong inversion are injected into the switched capacitor. At t_2 where a peak occurs, the transistor enters the second phase of turn off. During this phase, the current first decays continuously with time and then tends to saturate until it drops to zero. This indicates that when the gate voltage drops below threshold, the MOS transistor is operated in weak inversion and thus not only the channel charges in weak inversion but also the feedthrough charges via gate-to-diffusion overlap capacitance contribute to the error voltage. Finally, the MOS transistor is fully empty of mobile charges in the channel and only the charges coupled through the overlap capacitance continue to charge the holding capacitance. These



(a)



(b)

Fig. 3. (a) The comparison of the measured and simulated switch-induced error voltage versus the falling rate for two different input voltages; and (b) the charge percentage in terms of Q_a/Q_{total} and Q_c/Q_{total} versus the falling rate for two different input voltages, which comes from the experimental and simulated $I_D(t)$ waveforms as well as from (1) and (2). The total charge $Q_{\text{total}} = Q_a + Q_b + Q_c$. For the case of applying (1) and (2), the Q_{total} for calculating the percentage comes from the simulation. The area under the $I_D(t)$ curve is schematically separated into these three components.

descriptions of the different operations have been supported by the simulated results in terms of the surface electron density distribution and electron current vector (not shown here). The area under the current $I_D(t)$ curve can thus be separated into three distinct components Q_a, Q_b, and Q_c as schematically labeled in Fig. 3(b), where Q_a represents part of the channel charges in strong inversion; Q_b represents the channel charges in weak inversion; and Q_c represents the charges coupled through the gate-to-diffusion overlap capacitance. The validity of such separation has been confirmed by excellent agreement as demonstrated in Fig. 3(b). From Fig. 3(b) we can also observe that the component Q_b contributes to a considerable amount of about 20% for each of the falling rates studied here. These charges injected into the switched capacitor cause the error voltage expressed as $\Delta V_{\text{out}} = (Q_a + Q_b + Q_c)/C_H$. Good agreement in Fig. 3(a) ensures this relationship.

The component Q_a due to the channel charges in strong inversion can be modeled analytically as [4]

$$Q_a = \sqrt{\frac{\pi U C_H}{2\beta}} \frac{(2C_{\text{ol}} + C_{\text{ox}})}{2} \text{erf}\left(\sqrt{\frac{\beta}{2UC_H}} V_{HT}\right) \quad (1)$$

where C_{ox} is the gate oxide capacitance; C_{ol} is the gate-to-diffusion overlap capacitance; $V_{HT} = V_H - V_{\text{in}} - V_{\text{th}}$; $\beta = uC_{\text{ox}}/L^2$; u is the carrier mobility; and W/L is the channel width to length ratio. The component Q_c due to the charges coupled through the gate-to-diffusion overlap capacitance can be expressed as [4]

$$Q_c = C_{\text{ol}}(V_{\text{in}} + V_{\text{th}} - V_L). \quad (2)$$

The calculated charge percentage versus the falling rate with respect to Q_a and Q_c for two different input voltages is together plotted in Fig. 3(b). From Fig. 3(b) we can observe that without adjusting any parameter, the model expressions (1) and (2) can provide excellent agreement with not only the experimental data but also the mixed-mode simulation results. This agreement again validates the separation of the area under the $I_D(t)$ curve into three different components.

IV. Conclusion

Based on experimental test circuit and mixed-mode simulations, the charge injection component due to channel charges in weak inversion has been separated from the waveform of the current through the switched capacitor. The channel charges in weak inversion have been found to contribute comparably to the switch-induced error voltage on a switched capacitor and neglecting the channel charges in weak inversion can seriously underestimate the correct value of the error voltage.

References

[1] D. A. Hodges, "Analog switches and passive elements in MOS LSI," in *Analog MOS Integrated Circuits*, P. R. Gray, D. A. Hodges, and R. W. Brodersen, Eds. New York: IEEE Press, 1980, pp. 14–18.

[2] R. E. Suarez, P. R. Gray, and D. A. Hodges, "All-MOS charge redistribution analog-to-digital conversion techniques-Part II," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 379–385, 1975.

[3] P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a Miller hold capacitance," *IEEE J. Solid-State Circuits*, vol. 26, pp. 643–651, 1991.

[4] B. J. Sheu and C. Hu, "Switch-induced error voltage on a switched capacitor," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 519–525, 1984.

[5] W. B. Wilson, H. Z. Massoud, E. J. Swanson, R. T. George, and R. B. Fair, "Measurement and modeling of charge feedthrough in n-channel MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1206–1213, 1985.

[6] J. H. Shieh, M. Patil, and B. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 277–281, 1987.

[7] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1091–1097, 1987.

[8] C. Eichenberger and W. Guggenbuhl, "On charge injection in analog MOS switches and dummy switch compensation techniques," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 256–264, 1990.

[9] M. J. Chen, Y. B. Gu, T. Wu, P. C. Hsu, and T. H. Liu, "New observation of charge injection in MOS analog switches," *Electron. Lett.*, vol. 30, pp. 213–214, 1994.

[10] TMA MEDICI: Two-dimensional device simulation program, Technology Modeling Association, Inc., 1993.