An Accurate Hot Carrier Reliability Monitor for Deep-submicron Shallow S/D Junction Thin Gate Oxide n-MOSFET's

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ABSTRACT

In this paper, an accurate criterion has been proposed for reliability evaluation of state-of-the-art deep-submicron S/D extension n-MOSFET's. *A new monitor for HC reliability evaluation* has been developed using total values of N_{it} in the effective channel length region, instead of commonly used substrate current(I_B), impact ionization rate (I_D/I_B), or peak/average N_{it} values. An accurate degradation model has thus been developed based on the N_{it} distribution and mobility scattering effect. Moreover, this approach has been successfully used to demonstrate the feasibility for gate-engineering studies.

INTRODUCTION

It has been reported that the drain current degradation of MOSFET is mainly due to the interface state generation [1]. However, there exists an ambiguity that the oxide dependence of this degradation also depends on the device drain structures [2]. For example, the drain current degradation has different gate oxide thickness dependence for conventional and LDD structure MOSFET's. It is known from the measurements that a thinner gate oxide n-channel LDD MOSFET has poorer drain current degradation. It is mainly due to the spacer induced degradation which results from the interface states generated in the spacer region [3]. On contrary to that of LDD MOSFET's, different mechanism exists for conventional single drain MOSFET's. A thinner gate oxide device has better HC reliability for these devices [4]. This smaller degradation is mainly attributed to the smaller mobility reduction due to interface state generation.

On the other hand, the substrate current, I_B[1] , the impact ionization rate, I_B/I_D [5], and the peak or average value of interface states [6] have been used as a monitor to evaluate HC reliability, which has not been sufficient to accurately correlate I_B with drain current degradations.

In this paper, we will propose a new and accurate technique to evaluate the hot carrier reliability for the state-of-the-art deep-submicron n-MOSFET's with shallow S/D n^+ extension structure. For these devices, the generated interface states are usually located at the drain extension region inside the gate-drain overlap region. The main degradation mechanism of $\Delta I_D/I_D$ is mobility degradation in the S/D extension region underneath the gate. An accurate degradation model has thus been developed based on the N_{it} distribution and mobility scattering effect. Moreover, the same approach has been successfully used to demonstrate the feasibility for gate-engineering studies. The present method is valid for deep-submicron devices with effective channel length down to 0.1μm.

DEVICE FABRICATION

The devices used in this work were fabricated using 0.25 μm CMOS technology (Fig. 1 and Table 1). Two groups of n-MOSFET's were made. Type I has gate oxide thickness of 7nm, 4nm, and 3nm for studying the gate oxide dependence of HC reliability. Type II has 4nm gate oxide thickness and with various pure oxide and N_2O oxide in combination with RNO spacer. All these n-MOSFET's have shallow S/D n^+ extension. The n^+ S/D extension are formed using implanted Arsenic with dose and energy of 4.0×10^{14} cm^{-2} and 10Kev. Device effective channel lengths are 0.2μm and 0.1μm for types I and II respectively.

	Type I			Type II		
Device	(A)	(B)	(C)	(a)	(b)	(c)
Gate oxide thickness	7nm	4nm	3nm	4nm	4nm	4nm
$L_m(\mu m)/L_{eff}(\mu m)$	0.4/0.2	0.4/0.2	0.4/0.2	0.3/0.1	0.3/0.1	0.3/0.1
Gate oxide material	pure oxide	pure oxide	pure oxide	pure oxide	pure oxide	N_2O oxide
Sidewall spacer material	pure oxide	pure oxide	pure oxide	pure oxide	RNO	RNO

Table 1 Device parameters for test samples used in this study.

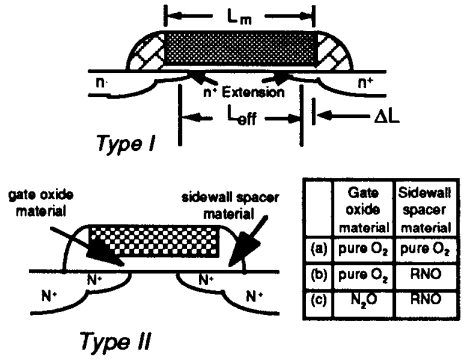

Fig. 1 Two types of MOSFET's used in this study.

GATE OXIDE THICKNESS DEPENDENCE OF S/D EXTENSION N-MOSFET's

Hot Carrier Stress Measurements

For hot carrier stress measurements, maximum substrate current stress conditions, $I_{B,max}$, were used. First we measure the substrate currents of three type I devices at V_{DS}= 3V, as shown in Fig. 2. The impact ionization rates (I_B/I_D) are also shown. Then, dc hot carrier stress was performed at $I_{B,max}$ with V_{DS}= 3V. This ensures that interface states were generated and no trapped charges were generated [7]. Also, the dominant mechanism of the drain current degradation is interface state. Fig. 3 shows the drain current degradations of these devices with different gate oxide thickness, in which the drain currents were measured at V_{GS}-V_T = 1V and V_{DS}= 0.1V. Results show that thinner gate oxide device has smaller drain current degradation. If I_B is used as a monitor (as in Fig. 2) of HC reliability, we can not identify which oxide thickness device has better reliability since 7nm and 4nm devices have approximately the same peak I_B values. The device with smaller I_B will not ensure a smaller I_D degradation. Therefore, further development of the correlation between drain current degradation, substrate current, and interface states is essential for both drain and gate engineering applications.

Profiling of Interface States

To solve the aforementioned problems and to find a correct correlation between Fig. 2 and Fig. 3, charge pumping technique [8]

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IEEE 99CH36296. 37th Annual International Reliability Physics Symposium, San Diego, California, 1999

has been employed to calculate the interface state profiles of these devices. Based on a fixed base level charge pumping measurement, the measured CP current is as shown in Fig. 4(a) for fresh and stressed devices, in which I_{CP} is plotted as V_{gh} (the applied high level of gate voltage). The difference between 2 curves (ΔI_{CP}) gives the values of N_{it}. On the other hand, Fig. 4(b) shows the distribution of the local threshold voltage along the channel. Based on the analytical expression (Eq.(5)) of the ΔI_{CP} derived in Table 2, we can calculate the spatial distribution of N_{it}, in which dV_{gh}/dx can be obtained directly by differentiating I_{CP}-V_{gh} and V_{gh}-x can be obtained from simulation. In Table 2, f is the pulse frequency. q is electronic charge, and W is the device channel width. This improved charge pumping method does not need to calculate troublesome depletion width and can characterize the interface states ranged from gate edge to the middle of the channel. Calculated results of the N_{it} distribution for type I devices are given in Fig.5. Here, the drain junction was determined from simulation. We see that the peak values of N_{it} distributions are all located inside the drain-gate overlap region and near the drain junction.

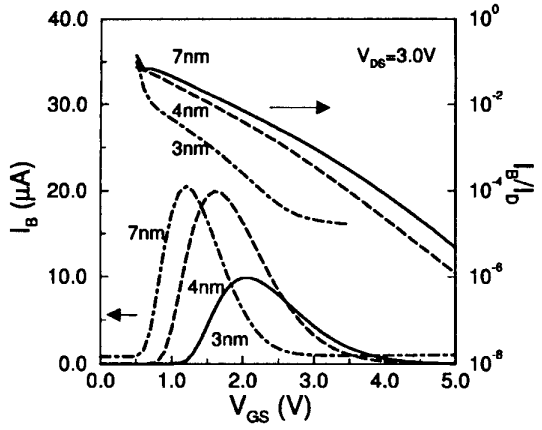

Fig. 2 Measured substrate current I_B and impact ionization rate (= I_B/I_D) for type I devices with different gate oxide thickness. 7nm and 4nm devices have about the same peak values of N_{it} while 7nm device has larger impact ionization rate.

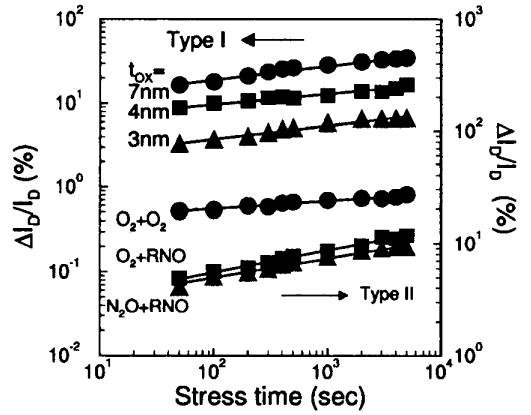

Fig. 3 Measured drain current degradations for type I and type II devices. Both type I and type II were stressed at $I_{B,max}$ conditions with V_{DS}= 3V.

Results and Discussion

It is noted that thicker oxide device 7nm shows the largest N_{it} values which seems to be consistent with the measured drain current degradations in Fig. 2, however, it can not explain the correlation between peak N_{it} values and I_B results in Fig. 3 where 7nm has the same value with that of 4nm device. In addition to the interface state characterization, we use a modified shift and ratio technique [9] to determine the effective channel length of these devices with results given in Fig. 6. Also, the total values of N_{it} in 7nm device in the effective channel region (Fig. 6) is plotted as a function of the gate voltage drive (V_{GS}- V_{TH}-0.5V_{DS}). It is this total $N_{it,total}$ value (bottom figure of Fig. 6) which causes the largest I_D degradation.

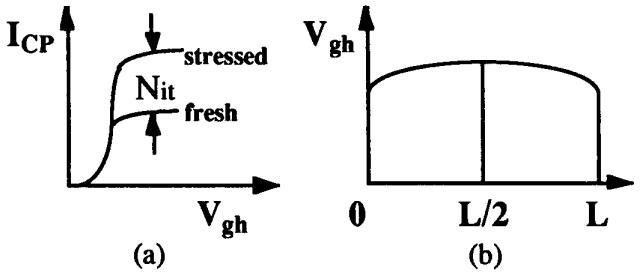

Fig. 4 (a) Schematic diagram showing the measured charge pumping currents for fresh and stressed devices.
(b) Schematic diagram of the local threshold voltage distribution along the channel.

$$\Delta I_{CP} = k \int_{V_{gl}}^{V_{gh}} D_{it}(V)\, dV, \quad k = f \cdot q \cdot W, \tag{1}$$

$$\Delta I_{CP} = k \int_{x_0}^{x_1} D_{it}(V) \frac{dV}{dx}\, dx, \tag{2}$$

$$\text{let } N_{it}(x) = D_{it}(V) \cdot \frac{dV}{dx}, \tag{3}$$

$$\Delta I_{CP} = k \int_{x_0}^{x_1} N_{it}(x)\, dx, \tag{4}$$

$$\frac{d\Delta I_{CP}}{dV_{gh}} \frac{dV_{gh}}{dx} = k\, N_{it}(x), \tag{5}$$

$$\Rightarrow N_{it}(x) = \frac{1}{k} \frac{d\Delta I_{CP}}{dV_{gh}} \frac{dV_{gh}}{dx}. \tag{6}$$

Table 2 Equations used to calculate N_{it} distributions.

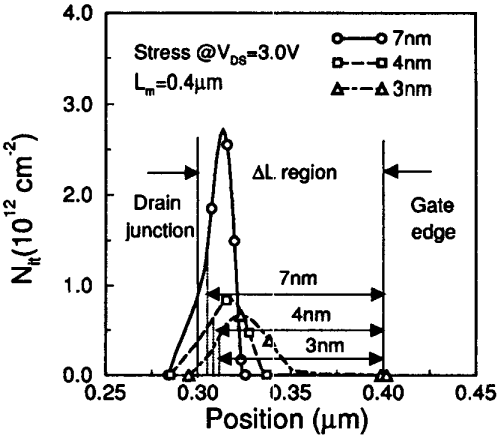

Fig. 5 Extracted N_{it} distributions for type I device with different gate oxide thickness. 30Å device has smaller number of N_{it} in the effective channel length region.

The reason for the largest degradation of the 7nm device is explained in Fig. 7, where damaged regions are represented by regions I and II in the channel and spacer regions respectively. The electrical field in a thinner gate oxide device is pushed toward the spacer region and is located inside the gate-drain overlap region. This results in a wider channel length region. Also, much less N_{it} is covered in the effective channel length region. Thick oxide device has larger number of N_{it} covered in region I which yields a larger I_D degradation. To support this argument, we propose an I_D degradation model as in Table 3 using a new definition of this N_{it} effect. Excellent agreement between model and experiment can be achieved as given in Fig. 8. We conclude that thinner gate oxide has smaller I_D degradation for S/D extension devices based on this total N_{it} concept. Furthermore, the main degradation of S/D extension device is similar to that of a conventional MOSFET's, in which mobility scattering [6] is the dominant mechanism of drain current degradation. In short, the concept of total N_{it} values provides a correct monitor for evaluating HC reliability of deep-submicron MOSFET's.

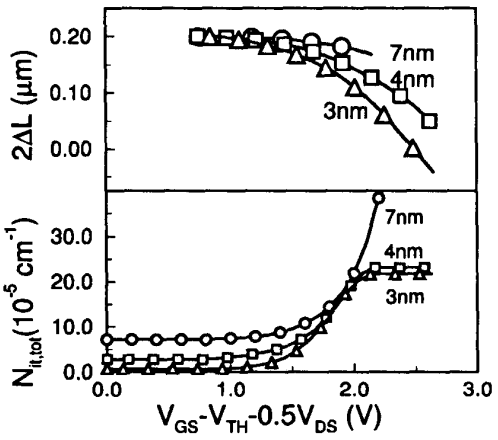

Fig. 6 Effective channel length $2\Delta L = L_{mask} - L_{eff}$ and total number of interface states N_{it} inside the effective channel length regions for type I devices with different gate oxide thickness. We see that 70A device has smaller L_{eff} but the largest total N_{it} values.

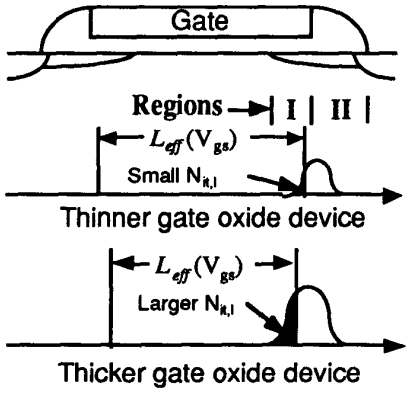

Fig. 7 Illustration of the N_{it} distributions for devices with thinner and thicker gate oxide thicknesses.

RELIABILITY FOR GATE-ENGINEERING APPLICATIONS

To improve the reliability of deep-submicron S/D extension devices, N_2O as the gate oxide and RNO(Reoxidized Nitridation Oxide) as the spacer can achieve this purpose. To show the validity of the present criterion, reliabilities of type II devices with N_2O and pure gate oxides were compared. The lower part of Fig. 2 shows the measured I_D degradation. Fig. 9 shows the measured I_B and impact ionization rate. Fig. 10 shows the interface state distribution profiles for type II devices. Results show that device (a) has the smallest I_B but its $\Delta I_D/I_D$ is the largest. Previous accepted criterion [1] is that device with smaller I_B should have better reliability, which is in conflict with the results here.

$$\frac{\Delta I_D}{I_D} = \{1+\frac{L_{eff}}{\alpha}[\int_0^{L_{eff}} N_{it}(x)dx]^{-1}\}^{-1} \quad (1)$$

where

$$\mu = \frac{\mu_0}{1+\alpha N_{it,tot}} \quad (2)$$

$$N_{it,tot} = \int_0^{L_{eff}} N_{it}(x)dx \quad (3)$$

Table 3 A generalized hot carrier model of I_D degradation for n^+ S/D extension MOSFET's.

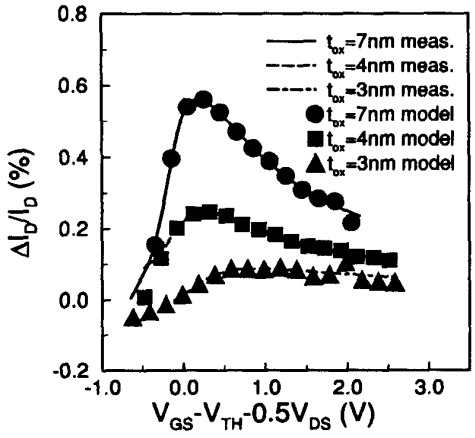

Fig. 8 Measured and modeled drain current degradation for type I (with different gate oxide thickness) devices.

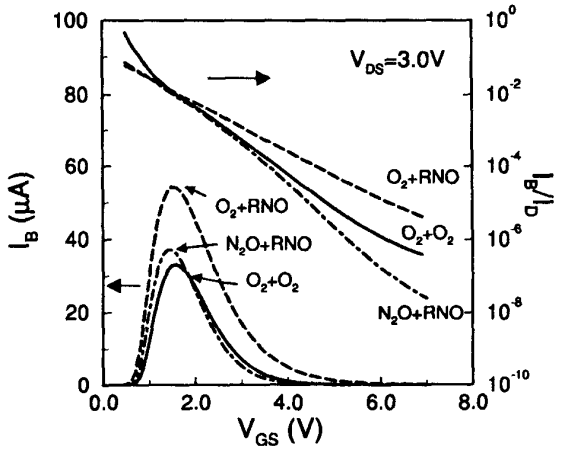

Fig.9 Measured I_B and impact ionization rate ($= I_B/I_D$) for type II devices with different gate oxide and spacer materials.

By calculating the total values of N_{it} in the effective channel length region ($L_{eff} = L_{mask} - \Delta L$) (Fig. 11) for three test samples, we found that total values of N_{it} (bottom figure of Fig. 11) give

(a)>(b)>(c). This means that device (a) has the largest $N_{it,total}$ values in the effective channel region and hence exhibits poor reliability even though it has smaller I_B, impact ionization rate, and peak N_{it} values. In other words, device (a) with pure O_2 gate oxide and O_2 spacer has a wider channel length since its electrical field is pushed toward the gate edge by comparing with those of devices (b) and (c). It has also the largest total values of N_{it} in Fig. 11 which is consistent with the $I_D/\Delta I_D$ degradation in Fig. 2. However, it is not consistent with the monitor using I_B or impact ionization rate in Fig. 9. It further manifests that HC reliability is not appropriate to use I_B as a monitor since N_{it} is not proportional to I_B. The new criterion shown in Fig. 11 or 12 can be used to justify the above reasoning. Again, Fig. 13 shows the comparison of drain current degradation between modeled and measured results for tyee type II devices. Excellent agreement has also been achieved. In short, in terms of the gate-enginnering for different gate and spacer oxides, results show that N_2O as thin gate oxide and RNO as spacer has been proved to be successful for deep-submicron MOSFET's. Furthermore, device with O_2 gate oxide and RNO spacer is most efficient for suppressing the hot carrier effect as revealed in Fig. 10.

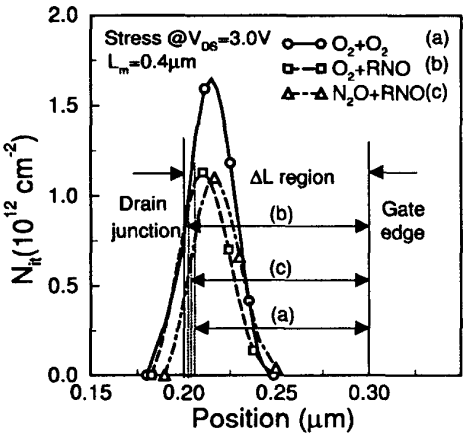

Fig. 10 Extracted N_{it} distributions for type II devices with different gate oxide materials. Combined N_2O gate oxide and RNO sidewall spacer has smaller number of N_{it} in the effective channel length region.

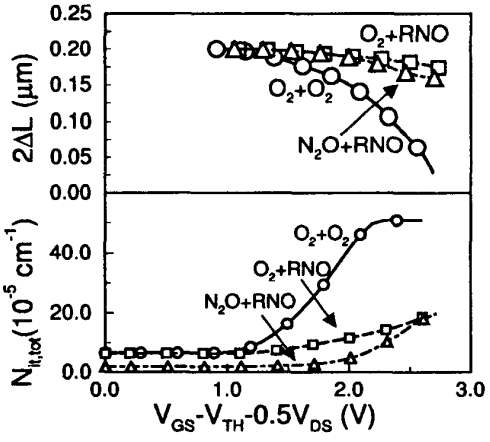

Fig. 11 Effective channel length 2ΔL and total number of N_{it} inside the effective channel length regions for different gate oxide and sidewall spacer materials. Note that pure gate oxide and spacer device (a) has the largest number of total N_{it} in the effective channel due to a wider effective channel length.

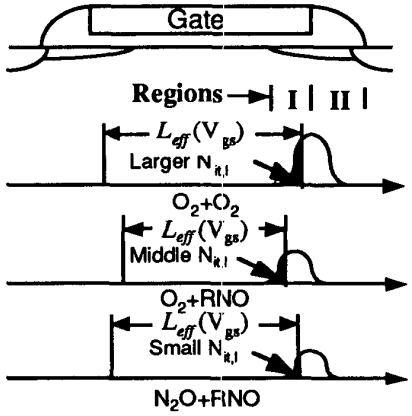

Fig. 12 Schematic diagram to show the comparison of N_{it} distribution and the effective channel length regions. Device (c) has the smallest number of N_{it} in the effective channel length region and hence a smallest drain current degradation.

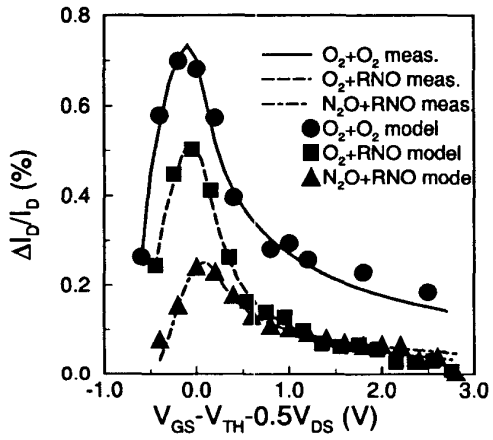

Fig. 13 Comparison of the measured and modeled drain current degradation for type II devices.

In summary, a new and accurate criterion has been proposed for reliability evaluation of deep-submicron n-MOSFET's. Several salient features include: (1) *A new monitor for HC reliability evaluation* has been proposed using total values of N_{it} in the effective channel length region, instead of commonly used I_B, I_B/I_D, or peak/average N_{it} values [1],[5],[6]. (2) The mobility scattering is the dominant factor of I_D degradation in state-of-the-art S/D extension devices. (3) An analytical I_D degradation model including the interface state and mobility scattering effect has been developed, and (4) The ambiguity of the HC reliability monitors in thin gate oxide deep-submicron ULSI devices can thus be solved using the present approach.

Acknowledgments This work was supported by the National Science Council, Taiwan, under contract *NSC86-2215-E009-027*.

REFERENCES

[1] C. Hu et al., *IEEE T-ED.*, ED-35, p. 375, 1985.
[2] S. S. Chung et al., *IEEE SISC*, PII.8, Dec. 3-5, 1998.
[3] F. Hsu, et al., *IEEE EDL.*, EDL-5, p. 71, 1984.
[4] H. S. Momose et al., in *IEDM Tech. Dig.*, p. 453, 1997.
[5] T. Hori et al., *IEEE T-ED.*, ED-39, p. 2312, 1992.
[6] S. Sun et al., *IEEE T-ED*, ED-27, p. 1497, 1980.
[7] S. Cheng et al., *IEEE T-ED*, ED-44, p. 1908, 1997.
[8] S. Chung et al., *SSDM*, Chiba, Japan, p. 841, 1993.
[9] S. Biesemans et al., *Symp. VLSI Technology*, p. 166, 1996.