Applying Selective Liquid-Phase Deposition to Create Contact Holes in Plasma Damage-Free Process

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Abstract- *We apply an alternative plasma damage-free process -- the selective liquid-phase deposition (S-LPD), instead of the conventional RIE to form metal/semiconductor contact holes. This paper studies the performance comparison between S-LPD and RIE to form contact hole in n+/p junction diode, Schottky diode, and ohmic contact. In our experiments, if the plama-free S-LPD technique is adopted, there is excellent performance including lower reverse current, lower ideality factor, higher forward current, higher Schottky barrier, lower contact resistance and better thermal stability in these devices.*

RIE is widely employed to etch silicon oxide to form contact holes owing to its anisotropic etching ability. However, because of inevitable energetic ions and fluorine-contained radicals in plasma ambient, RIE easily causes energetic surface contamination and rf damage in SiO_2/Si interface. In addition, the selectivity issue of RIE has become more critical in ultra-shallow junction, because overetch is less allowed. To avert these problems, an alternative method without etching is urgently required to replace conventional RIE method. According to our previous investigation[1],[2], the liquid-phase deposition (LPD) method can selectively deposit silicon oxide against photoresist, shown in Fig.1, if the condition of hydro-fluorosilicic acid solution is adequately controlled. This SEM photograph reveals the possibility of further applying S-LPD to the deep submicron process. In this work, we apply S-LPD to form contact holes in n^+/p diodes, Schottky diodes and Kelvin resistors and, thereby, study the superiority of utilizing plasma-free S-LPD over the conventional method by comparing the current-voltage (I-V) characteristics of prepared devices.

The P-type (100) wafers with 15~25 Ω-cm resistivity are adopted in the n^+/p diodes and Kelvin resistors fabrication. Following formation of the channel stopper and field oxide, phosphorus with dose of $5 \times 10^{15}cm^{-2}$, and energy of 40keV is implanted to make n^+/p junction. As the left side of Fig.2 indicates, for the S-LPD samples, the photoresist on the site of contact hole region is first patterned and, then, the LPD oxide is selectively grown on the region without photoresist. After removing the photoresist, contact holes without plasma damage are automatically formed. For the RIE samples, as shown in the right side of Fig.2, LPD oxide is globally deposited all over the wafers, and then the contact holes are formed by using RIE technique (only CF_4 gas: 5sccm, 50mtorr; rf power: 100W) through lithography photoresist patterns. After metallization, some n^+/p junction diodes are sintered at 400℃, 30min, in N_2. The Kelvin resistors, illustrated in Fig.3, were fabricated with the same condition. Meanwhile, for Schottky diodes, the fabrication procedures closely resemble those of n^+/p diodes except for 1~5 Ω-cm resistivity N-type (100) wafers used and no ion-implantation needed. In these devices, typical current-voltage (I-V) characteristics and contact resistance are investigated to clarify the better performance of damage-free devices.

Fig.4 shows the I-V characteristics of n^+/p diodes fabricated by S-LPD, RIE and partial-RIE, respectively. Herein, the partial RIE method is adopted to buffer some plasma damage. Such an application suggests that the 85% oxide is etched by RIE and, then, the remaining 15% oxide is etched by wet-etching in BHF solution. The n^+/p junction area is 100x100μm and the contact hole area is 60x60μm. The reverse current of S-LPD samples is much less than those of RIE and partial RIE samples. Several key characteristic parameters are summarized in Table1. Although partial-RIE can slightly improve some diode characteristics relatively to RIE only used, the damage-free S-LPD diodes exhibit excellent performance relative to the RIE or partial-RIE ones whether in forward bias or in reverse bias.

Table 1 also lists the reverse area current density, J_{RA}, and the reverse periphery current density, J_{RP}. To extract these two reverse current density, we have to apply two n^+/p diodes with different size.

1998 3rd International Symposium on Plasma Process-Induced Damage.
June 4-5, Honolulu, HI, USA. Copyright © 1998 American Vacuum Society.

Combining the 200x200 μm diode and the foregoing 100x100 μm diode, by the following equation:

$$I = J_{RA} WL + J_{RP} \times 2(L+W),$$

we can calculate the J_{RA} and J_{RP}. As listed in this table, S-LPD exhibits much smaller J_{RA} and J_{RP}. Especially, the J_{RA} of RIE is two-order higher than the J_{RA} of S-LPD. This finding indicates that RIE damages and contaminates in contact area very seriously, relative in the periphery junction region. The damage and contamination can serve as generation centers to enlarge reverse current and serve as recombination centers to degrade ideality factor. Therefore, the performance of S-LPD diodes is much better than that of RIE diodes in reverse bias and in small forward bias because this problem doesn't exist in the S-LPD process. Meanwhile, as Fig.4 depicts, the partial RIE can reduce damage and improve reverse current. However, comparing to the S-LPD, it is still worse very much. This seems to result from the following two reasons: First, in RIE plasma ambient, there are some high energy ion or radial which can penetrate the 15% remaining oxide into the silicon bulk region. Secondly, the rf radiation of RIE can also damage device. Thirdly, the micro-trenching effect[3] due to ion reflection from the photoresist sidewall can enhance the etching at contact periphery and cause more serious penetration. Therefore, only using S-LPD can avoid the RIE damage problem and get the advantages due to plasma-free.

Fig.5(a) and Fig.5(b) show the diode performance before and after sintering treatment, 400 ℃, 30min, in N_2. Sample diodes of aluminium directly contact to silicon are shown in Fig.5(a). After sintering treatment, the reverse current of RIE diode drastically increase. It's almost three order higher than S-LPD diode after the same sintering. Sample diodes, shown in Fig.5(b), are to add titanium silicide between aluminium and silicon. The similar trend also exists, but the increase magnitude of reverse current is not so serious. By these two figure, this results attribute to two factors as following. First, the Al spiking effect cause this degradation. Especially, the spiking effect of RIE is more serious than that of S-LPD. It indicates that RIE damage will enhance the Al spiking effect. Secondly, the contamination and impurities due to RIE further penetrate into the depletion region of n^+/p junction after thermal sintering and, therefore, enlarge the reverse current. Therefore, even if we add titanium silicide, the reverse current increase level of RIE is still larger than that of selective-LPD.

To investigate the Si near-surface region in ultra-shallow junction, we utilize Schottky diodes to demonstrate the plasma damage problem of near-surface region between RIE and S-LPD. Fig.6 depicts the performance of S-LPD and RIE Schottky diodes, and Table 1 also summarizes the key characteristics. Before sintering, RIE sample nearly loses the rectifying characteristics of Schottky diode under reverse bias, but S-LPD sample exhibits satisfactory Schottky characteristics. However, after sintering (solid curve), the S-LPD sample still exhibits about four order smaller than that of RIE sample in reverse current; meanwhile the ideality factor 1.03 of the former is also lower than 2.03 of the latter. This finding reveals that the sintering is necessary for the RIE sample to release a part of residues and defects from the Si surface, but unnecessary for the S-LPD sample. For RIE Schottky diode, the worse ideality can be attributed to the large surface recombination velocity. According to the curve slope of $\ln\{I/[1-\exp(-qV/kT)]\}$ versus forward-bias voltage, the potential barriers is 0.83eV and 0.6eV for S-LPD and RIE Schottky diode, respectively. This result attributes to that the donor-like bonding defects and the polymer residues make the depletion region thinner and the potential barrier lowering. The barrier lowering effect seriously degrades both reverse and forward I-V characteristics. Above results imply that RIE will be increasingly critical and requires more severe after-RIE-treatment in ultra-shallow junction. However, utilizing S-LPD can avert these problems, and is expected to be a highly promising candidate as novel plasma damage-free and plasma contamination-free technology.

In the contact investigation, at first, we measure the contact resistance Rc with Kelvin D-resistors. The Kelvin contact resistance is widely defined by the voltage 1 to 3 over the fed current 2 to 4, illustrated in Fig.3, i.e., the slope of V_{13}-I_{24} plot in Fig.7. Fig.7 depicts the V-I characteristics at the current fed from -20mA to 20mA for the resistor with contact size LxL=10x10μm^2 and collar width d=10μm. The S-LPD resistor shows a linear V-I relationship and exhibits a good ohmic contact. However, the RIE resistor shows a non-linear V-I relationship and, therefore, exhibits a non-constant and larger Rc value, especially in the small current region. This result indicates that the RIE with fluorine carbide plasma enlarges contact resistance very seriously. This serious problem seems to be resulted from that RIE causes the mobility decrease in etched surface because the impurities impinged by RIE will scatter carriers when electrons or holes move through the damaged contact surface.

We incorporate the measured Rc results of different L/d ratio into the universal curves of 4-terminals Kelvin D-resistor simulated by J. Santander et al[4]. By the measured Rc/Rs ratio versus the contact/collar ratio L/d of resistors, shown in Fig.8, the Rc/Rs values of S-LPD samples are much smaller than those of RIE samples in all resistors with various geometry size. Combining the dash lines which show the simulated universal curves in Fig.8, the L_T/d value of S-LPD with 10μm collar is 1/2~1/8 factor smaller to that of RIE. By this figure for the 10μm collar resistors, we estimate that the transfer length, $L_T=(\rho c/Rs)^{1/2}$, of S-LPD samples is about 2.7~5.5μm, but that of RIE is about 10~22μm. Therefore, with Rs=26Ω/sq measured, we get that the specific Al/Si contact resistivity ρc, which only depends on the material and process issues, approximates to 10^{-6} Ω-cm^2 for S-LPD; meanwhile, the ρc of RIE is higher than 10^{-5} Ω-cm^2. Even if we cleaned the RIE contact holes with RCA cleaning in our experiments, it seems to be impossible to clean the RIE contamination, which is impinged by rf-power or dc-bias, by the conventional clean method. However, the photoresist contamination of S-LPD is easily cleaned by the conventional clean method. Because the contact resistivity is very sensitive to the clean problem in metal/Si interface[5], the specific ρc of RIE must be much larger than that of S-LPD except that a severe and complex after-RIE-treatment is employed[6].

In this paper, the S-LPD technique has been successfully adopted to form contact hole. As described above, the plasma-free S-LPD technique is superior to the conventional RIE with the following advantages: very low reverse current for n+/p diode, good stability for thermal treatment, rather high potential barrier for Schottky diode, and low contact resistance. In contrast, the conventional RIE technology cannot be utilized in damageless contact-hole formation. The S-LPD technique is highly promising to replace conventional RIE for contact hole formation. In general, S-LPD method doesn't damage and contaminate the device surface; thus, no additional treatment is required. Therefore, the novel S-LPD technology can be applied to ultra-shallow junction and deep submicron process in the near future.

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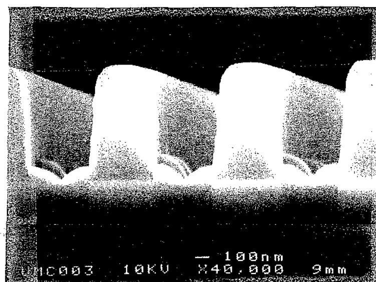


Fig.1 SEM cross section view of oxide profile against photoresist for selective-LPD deposition.

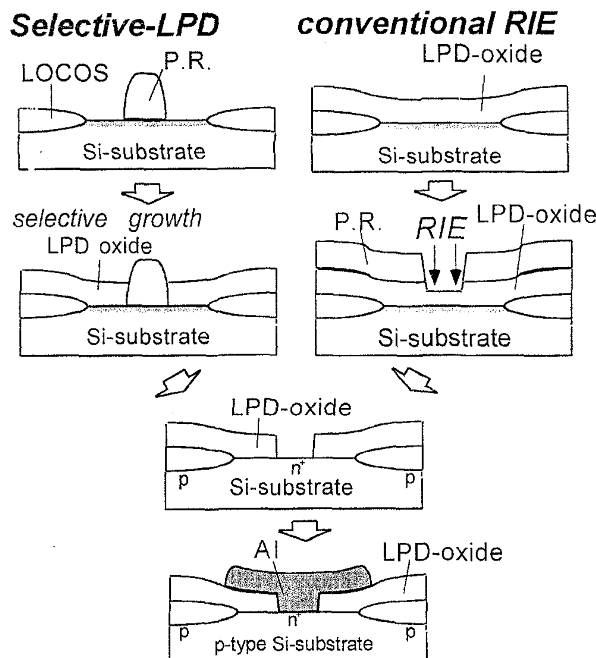


Fig.2 The brief diagram of key processes for the metal/semi-conductor contact hole fabricated by the S-LPD (left) and the conventional RIE (right), respectively.

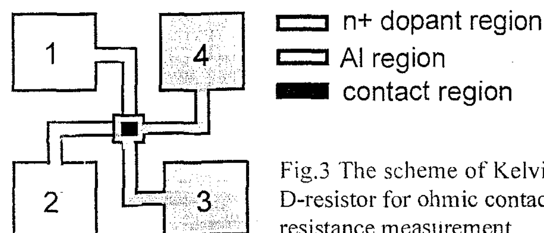


Fig.3 The scheme of Kelvin D-resistor for ohmic contact resistance measurement.

Table 1 Key parameter comparison of n^+/p diodes and Schottky diodes fabricated by S-LPD and RIE.

	n^+/p junction diode					Schottky diode		
	before sintering				after sintering			
	ideality factor η	reverse current at 5V: I_R (A)	J_{RA} (A/cm²)	J_{RP} (A/cm)	reverse current (A) at 5V	Schottky ideality factor η_{Sc}	reverse current (A) at -5V	barrier height (eV)
S-LPD	1.11	2.77e-11	5.72e-8	1.72e-9	6.09e-9	1.03	4.14e-9	0.83
RIE	1.69	2.57e-9	9.25e-6	4.10e-8	5.82e-6	2.03	1.85e-5	0.6

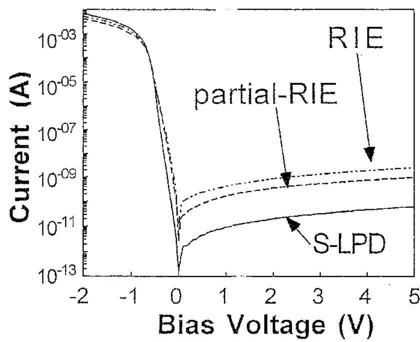


Fig.4 I-V characteristics of n^+/p diode fabricated by S-LPD, RIE, and partial-RIE, respectively.

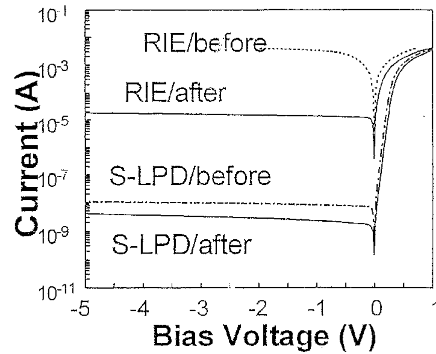
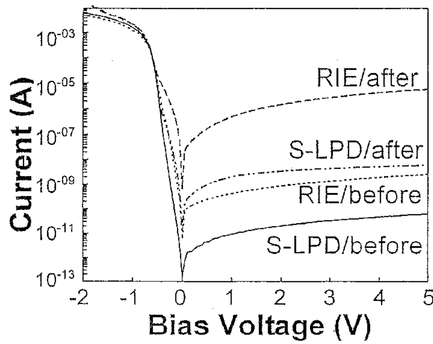
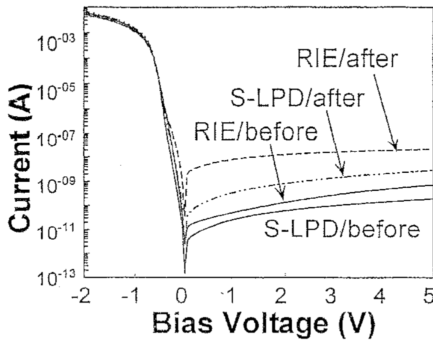


Fig.6 I-V characteristics of Schottky diodes fabricated by S-LPD and RIE, before and after sintering.



(a)



(b)

Fig.5 I-V characteristics of n^+/p diode before/after sintering for (a) Al/Si contact, (b) Al/Ti/Si contact.

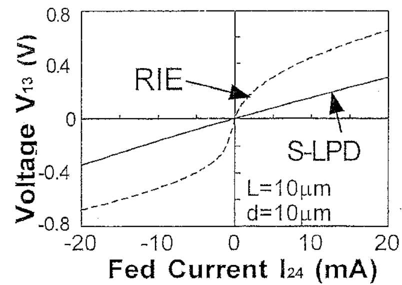


Fig.7 V-I plot of Kelvin D-resistors fabricated by S-LPD and RIE, respectively.

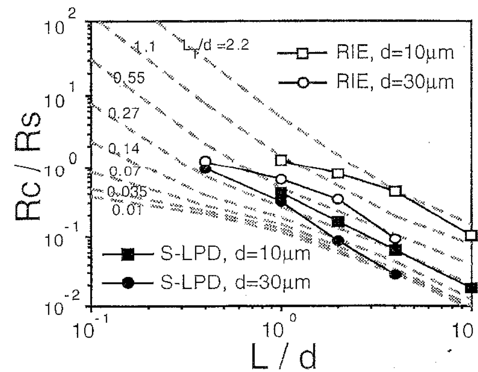


Fig.8 Measured Rc/Rs in simulated universal curves for the Kelvin D-resistors fabricated by S-LPD and RIE, respectively.