Voltage Scaling and Temperature Effects on Drain Leakage Current Degradation in a Hot Carrier Stressed n-MOSFET

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ABSTRACT

Drain leakage current degradation at zero V_{gs} in a hot carrier stressed n-MOSFET is measured and modeled. The dependences of drain leakage current on supply voltage and temperature are characterized. In modeling, various drain leakage current mechanisms including drain-to-source subthreshold leakage current, band-to-band tunneling current and interface trap assisted leakage current are taken into account. Our result shows that interface trap induced leakage current appears to be a dominant drain leakage mechanism as the supply voltage is scaled below 3.0V. Drain leakage current degradation by orders of magnitude has been observed due to hot carrier stress.

INTRODUCTION

The reduction of drain leakage current at zero V_{gs} has been a major concern in CMOS device scaling. Gate induced drain leakage (GIDL) current resulting from band-to-band tunneling has been recognized as one of the major drain leakage mechanisms in thin-oxide MOSFET's [1]. Recently, hot carrier stress effects on device degradation have received much interest [2-6]. However, most of the studies concentrate on stress induced on-state drain current reduction [2,3]. The stress effect on off-state drain leakage current degradation has not received as much attention [4,7]. The stress effect on drain leakage current is attributed to the creation of oxide trapped charge and interface traps. The build-up of negative oxide charge shifts the device flat-band voltage and results in an enhancement of band-to-band tunneling current. In addition, the generated interface traps can introduce an additional trap-assisted leakage mechanism [8]. At scaled supply voltages, while band-to-band tunneling can be greatly alleviated, the trap-assisted current may appear to be a dominant leakage mechanism. Furthermore, experimental results showed that the trap-induced leakage current exhibits a dependence on temperature [9]. In a certain bias range, the leakage current becomes much aggravated as temperature rises and thus may have impact on a DRAM refresh time. In this work, it is our intention to investigate the hot carrier stress effect on drain leakage current degradation in thin-oxide MOSFET's. The drain leakage current mechanisms at different supply voltages and temperatures are characterized and modeled.

DRAIN LEAKAGE CURRENT MECHANISMS

Various drain leakage paths in a stressed MOSFET are considered in our model. The trap-independent leakage mechanisms include band-to-band tunneling current (I_{BB}) and drain-to-source subthreshold current (I_S),

$$I_{BB} = AE_t^2 exp(-B/E_t) \quad (1)$$

$$I_S = I_o exp(\frac{q}{nkT} V_{gs}) \quad (2)$$

where the parameters A and B are defined in Ref. [10]. E_t denotes the total Si surface field. Drain junction leakage current is small in this work and can be neglected. Fig. 1 illustrates these two components in the lateral direction and in the vertical direction respectively.

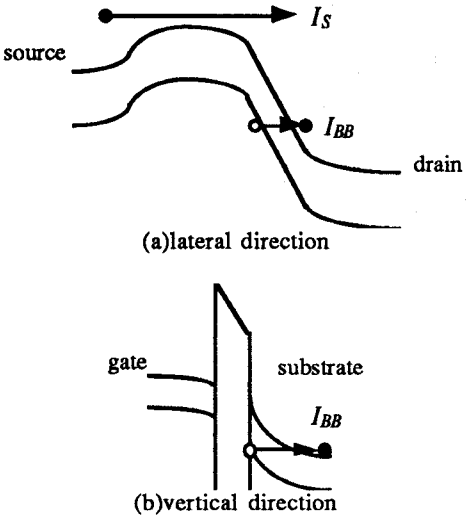


Fig. 1 Illustration of subthreshold leakage current (I_S) and band-to-band tunneling current (I_{BB}) (a) in the lateral direction and (b) in the vertical direction.

The interface trap assisted leakage mechanisms are the Shockley-Read-Hall current (ΔI_{SRH}), thermionic-field emission current (ΔI_{TF}), and sequential tunneling current (ΔI_{TAT}). A complete trap-assisted drain-to-substrate leakage path at the Si/SiO_2 surface is formed by hole emission from traps to the valence band and electron emission from traps to the conduction band. Both electron emission and hole emission are carried out via either thermionic emission or field emission. The carrier transition processes are drawn in Fig. 2. In the figure, G_e and G_h stand for electron and hole thermionic emission rates and T_e and T_h denote electron and hole tunneling rates. Each carrier transition rate is formulated as follows,

$$G_e = v_{th}\sigma_n[n_i exp(\frac{\mathcal{E}_t - \mathcal{E}_i}{kT}) - n_s(1-f_t)] \quad (3)$$

$$G_h = v_{th}\sigma_p[n_i exp(\frac{\mathcal{E}_i - \mathcal{E}_t}{kT}) - p_s f_t] \quad (4)$$

$$T_e = \frac{f_t - f_c}{\tau_e} \quad (5)$$

$$T_h = \frac{(1-f_t)-(1-f_v)}{\tau_h} \quad (6)$$

where σ_n and σ_p are electron and hole capture cross sections, $\mathcal{E}_i$ and $\mathcal{E}_t$ stand for the intrinsic Fermi-level and trap energy. f_v, f_t and f_c are the electron occupation factors in the valence band, trap states and in the conduction band, respectively. n_s and p_s are electron and hole concentrations at the Si surface, which are calculated from a two-dimensional device simulation. τ_e and τ_h are electron and hole tunneling times from the WKB approximation. In a steady-state, the trap occupation factor f_t can be evaluated from the equality $G_e+T_e=G_h+T_h$ with $f_c\approx 0$ and $f_v\approx 1$. The three trap-assisted leakage current components are therefore expressed in the following [8],

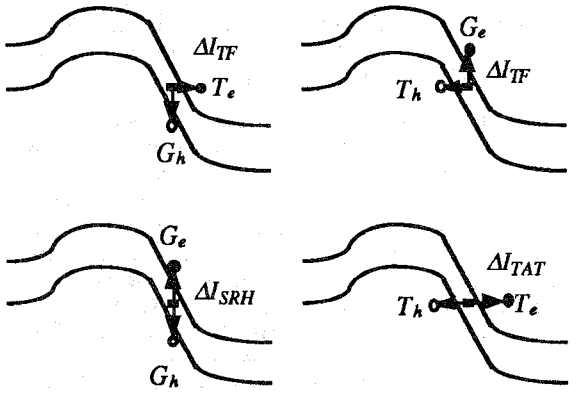
$$\Delta I_{TAT} = qW\int_{\Delta L}\int_{bandgap} \Delta N_{it}(x,\mathcal{E})\frac{T_eT_h}{G_e+T_e}d\mathcal{E}dx \quad (7)$$

$$\Delta I_{TF} = qW\int_{\Delta L}\int_{bandgap} \Delta N_{it}(x,\mathcal{E})\frac{T_eG_h+T_hG_e}{G_e+T_e}d\mathcal{E}dx \quad (8)$$

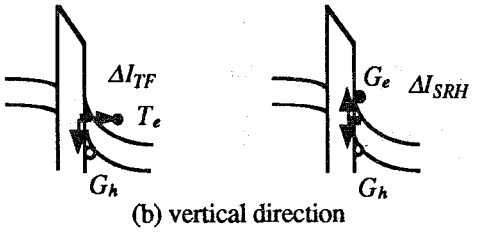
$$\Delta I_{SRH} = qW\int_{\Delta L}\int_{bandgap} \Delta N_{it}(x,\mathcal{E})\frac{G_eG_h}{G_e+T_e}d\mathcal{E}dx \quad (9)$$

where ΔL is the width of the interface trap (ΔN_{it}) region and W is the channel width. The total trap-assisted leakage current ΔI_d is the summation of the above three components,

$$\Delta I_d = \Delta I_{SRH} + \Delta I_{TF} + \Delta I_{TAT} = qW\int_{\Delta L}\int_{bandgap} \Delta N_{it}(x,\mathcal{E})(G_e+T_e)d\mathcal{E}dx \quad (10)$$



(a) lateral direction



(b) vertical direction

Fig. 2 Illustration of various carrier transition processes (a) in the lateral direction and (b) in the vertical direction. Note that T_h only occurs in the lateral direction.

The temperature-dependent parameters used in the calculation are bandgap ($\mathcal{E}_g$), thermal velocity (v_{th}) and intrinsic concentration (n_i). They are given below [11],

$$\mathcal{E}_g(T) = \mathcal{E}_g(0) - \alpha T^2/(T+\beta) \quad (11)$$

$$v_{th} = \sqrt{3kT/m^*} \quad (12)$$

$$n_i = \sqrt{N_cN_v}\exp[-\frac{\mathcal{E}_g(T)}{2kT}] \quad (13)$$

The field-dependent parameters are τ_e and τ_h,

$$\tau_e = \tau_{oc}\exp[\frac{4}{\hbar}(2m_n)^{1/2}\frac{(\mathcal{E}_c-\mathcal{E}_t)^{3/2}}{3qE_t}] \quad (14)$$

$$\tau_h = \tau_{ov}\exp[\frac{4}{\hbar}(2m_p)^{1/2}\frac{(\mathcal{E}_t-\mathcal{E}_v)^{3/2}}{3qE_t}] \quad (15)$$

where τ_{oc} and τ_{ov} are effective transit times in the conduction band and in the valence band, E_l is the surface field in the lateral direction and other variables have their usual definitions. Note that the hole tunneling T_h occurs only in the lateral direction. Thus, T_h is a function of only a lateral field whereas the tunneling process I_{BB} and T_e are dependent on a total field.

DEVICE CHARACTERIZATION

The test device is a 0.35μm n-MOSFET with source/drain extension. The gate oxide thickness is about 40Å and the gate width is 100μm. The device was subject to maximum substrate current stress V_{gs}=2V and V_{ds}=4.5V for 3000 seconds. The pre-stress and post-stress I_d-V_{gs} characteristics are shown in Fig. 3 (T=292K) and in Fig. 4 (T=353K), respectively. Under the stress condition, interface trap generation is almost saturated and oxide charge creation is minimal [7]. Interface trap generation is evidenced by the change of the subthreshold swing in Figs. 3 and 4. The DIBL effect is not significant in the device.

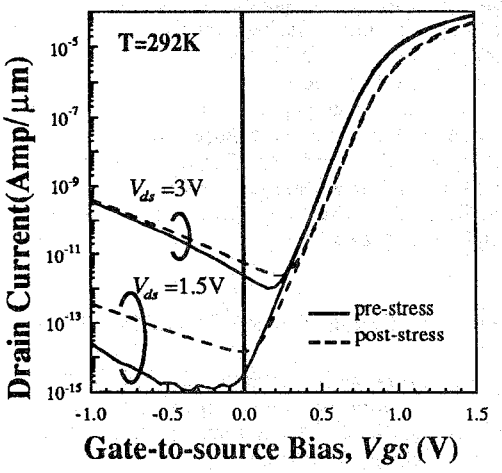


Fig. 3 Measured pre-stress and post-stress I_d-V_{gs} characteristics at V_{ds}=1.5V and 3.0V, T=292K.

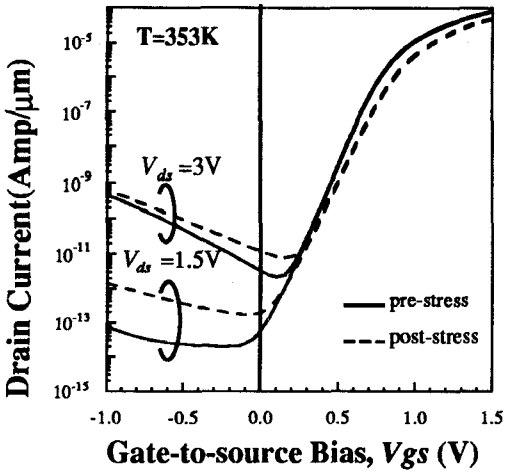


Fig. 4 Measured pre-stress and post-stress I_d-V_{gs} characteristics at V_{ds}=1.5V and 3.0V, T=353K.

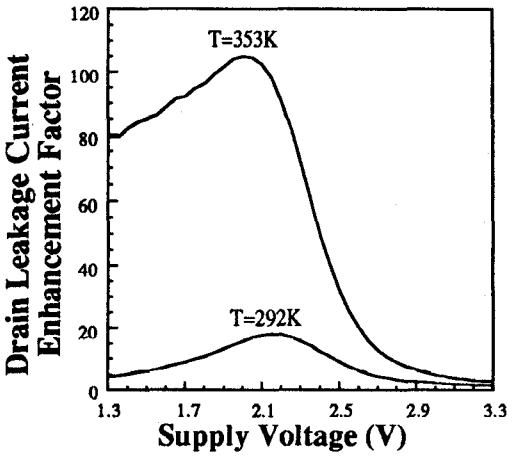


Fig. 6 The ratio of the post-stress drain leakage current to the pre-stress (T=292K) drain leakage current versus supply voltage.

RESULTS AND DISCUSSIONS

The dependence of pre-stress and post-stress drain leakage currents on supply voltage (V_{dd}) is measured in Fig. 5. The leakage current enhancement factor, defined as the ratio of the post-stress drain leakage to the pre-stress drain leakage at T=292K, is shown in Fig. 6. The trap effect on the leakage current enhancement becomes particularly pronounced around a supply voltage of 2.2V. An enlargement of the drain leakage current by a factor of 18 is observed at T=292K. Various drain leakage current components I_{BB}, I_S and the trap induced ΔI_d are plotted in Fig. 7. The solid lines are the measured result and the circles represent the calculated result.

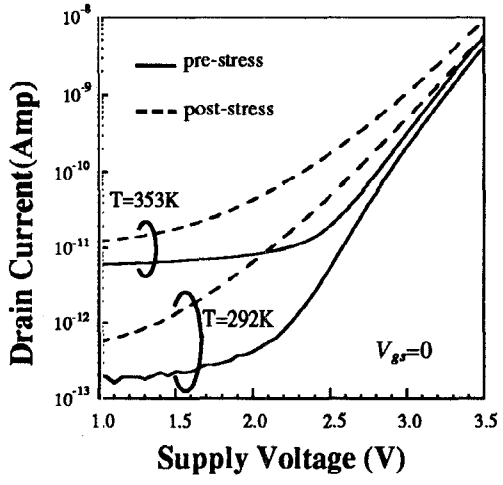


Fig. 5 Measured drain leakage current characteristics before and after stress at two different temperatures, T=292K and T=353K.

The interface trap density N_{it} used in the calculation is $1.4\text{x}10^{12}\text{cm}^{-2}$ and the length of the trap distribution (ΔL) is 400Å. σ_n and σ_p in Eqs. (3) and (4) are 10^{-15}cm^2 [11]. The following features are observed. At a large supply voltage (V_{dd}≥3.0V), the band-to-band tunneling current (I_{BB}) manifests itself as a dominant mechanism even in a stressed device. In addition, the trap induced component ΔI_d exhibits a weaker field dependence than the I_{BB} due to a smaller tunneling barrier from traps to the conduction band (electron tunneling) or to the valence band (hole tunneling). As a result, as the supply voltage scales, the I_{BB} drops more quickly and the ΔI_d appears to be a major drain leakage mechanism in a stressed device. When the V_{dd} is further reduced, the tunneling effect becomes unimportant. The enhancement of the drain leakage is achieved mainly through the SRH component. Therefore, the enhancement factor in Fig. 6 peaks around 2.2V. At T=353K, the enhancement factor in Fig. 6 is significantly increased up to 110. The temperature effect is apparent at a lower V_{dd}. The enhancement factor at V_{dd}=1.3V increases from about 5 at T=292K to 80 at T=353K. The I_{BB}, I_S and the ΔI_d at T=353K are shown in Fig. 8.

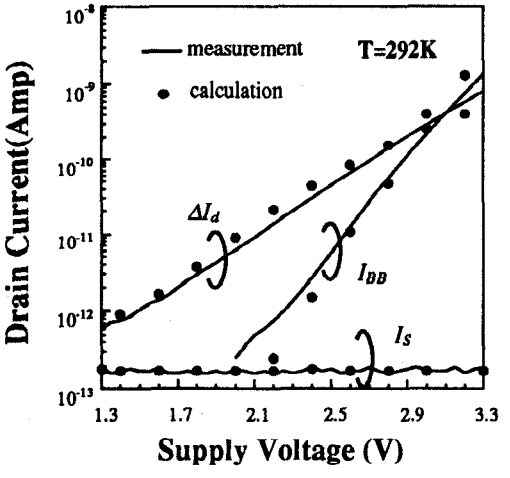


Fig. 7 Various drain leakage current components at T=292K from measurement (solid lines) and calculation (full circles).

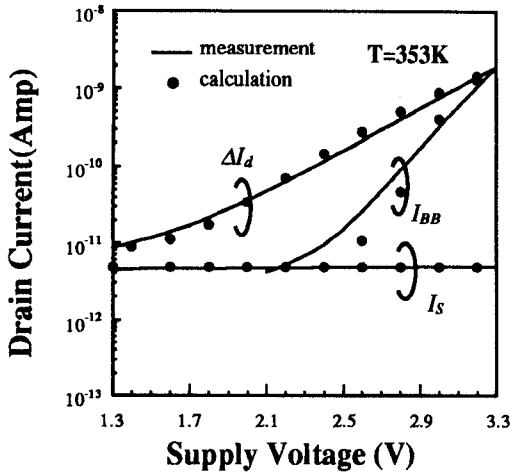


Fig. 8 Various drain leakage current components at T=353K from measurement (solid lines) and calculation (full circles). ΔI_d reprensents the trap-induced drain leakage.

Furthermore, the components in the ΔI_d are analyzed in Fig. 9 (T=292K) and in Fig. 10 (T=353K). In Fig. 9, the trap-induced drain leakage is dictated by the ΔI_{TAT} for V_{dd}>1.7V, by the ΔI_{TF} for 1.7V≥V_{dd}≥1.5V, and by the ΔI_{SRH} for 1.5V≥V_{dd}. In Fig. 10, the thermally related components ΔI_{TF} and ΔI_{SRH} are more prominent. As the supply voltage scales, the field dependent current component (ΔI_{TAT}) can be greatly alleviated, while the temperature dependent components (ΔI_{TF} and ΔI_{SRH}) become dominant drain leakage mechanisms.

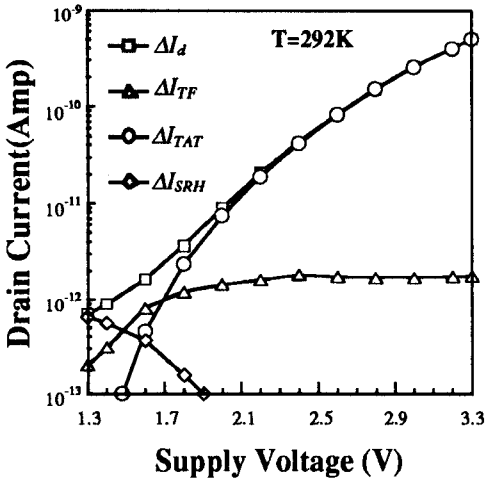


Fig. 9 Calculation of various interface trap induced drain leakage current components at T=292K.

The vertical field and the lateral field effects on drain leakage current are also assessed. Our calculation reveals that the band-to-band tunneling current is mainly contributed by the vertical field whereas the trap-assisted tunneling is mostly determined by the lateral field due to the dependence of T_h (hole tunneling) only on the lateral field.

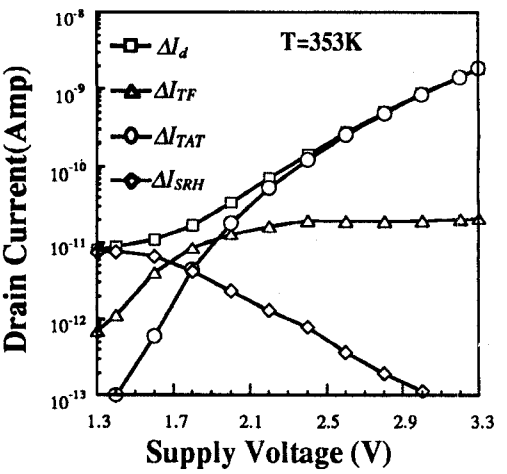


Fig. 10 Calculation of various interface trap induced drain leakage current components at T=353K.

CONCLUSIONS

The band-to-band tunneling current is found to be a dominant drain leakage mechanism at V_{dd}=3.3V in the current device structure. At a reduced supply voltage, the trap-induced current appears to be the major leakage component. We have observed that hot carrier stress can degrade the drain leakage current by orders of magnitude. While the vertical field has a larger effect on the band-to-band tunneling current, the trap-induced leakage is mostly caused by lateral field enhanced tunneling. The reduction of lateral field is necessary to suppress the trap-induced drain leakage in deep submicron devices.

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