Low Temperature Formation of Shallow p⁺n Junctions by BF_2^+ Implantation into Thin Pd_2Si Films on Si Substrates

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ABSTRACT

Excellent silicided shallow p^+n junctions have been successfully achieved by the implantation of BF_2^+ ions into thin Pd_2Si films on Si substrates to a dose of 5×10^{15} cm^{-2} and subsequent low temperature (even at 550°C) furnace annealing. The formed junctions have been characterized for respective implantation conditions. In this experiment, the implant energy is the key role in obtaining a low leakage diode. Reverse current density of about 3 nA/cm^2 and an ideality factor of about 1.05 can be attained by the implantation of BF_2^+ ions at 80 keV and subsequent annealing at 550°C. The junction depth is about 0.09 μm, measured by the spread resistance method. As compared with the results of unimplanted specimens, the implantation of BF_2^+ ions into a thin Pd_2Si layer can stabilize the silicide film and prevent it from forming islands during high temperature annealing.

Introduction

Metal silicides have been used to lower the contact resistance of source or drain and gate electrodes as well as interconnections.[1-3] The self-aligned metal-silicide technology[4-7] has proven to be a highly desirable technique for improving micrometer and/or submicrometer device and circuit performances.

In metal-oxide-semiconductor (MOS) very-large-scale-integrated (VLSI) circuits, the channel length of an MOS field effect transistor has been scaled down to submicron dimensions. Accordingly, a concomitant reduction in source/drain junction depth is required to minimize short channel effect.[8] Conventionally, shallow p^+n junctions were difficult to realize since anomalous rapid boron diffusion in Si would occur at high processing temperatures. To further reduce the junction depth, new techniques must be employed. A method to make silicided shallow junctions is to deposit a layer of metal and then implant dopants through the metal layer (ITM). This technique is promising because the implantation also serves to ion-mix the metal/Si interface and thus promotes silicide formation.[9,10] A drawback to this technique is the possibility of knocking metal into junction regions by heavy, high-energy dopant ions. It was reported that all diodes fabricated by As^+ implantation through a thin Co layer showed reverse currents of about 100 $\mu A/cm^2$ at 5 V.[11] The knock-on Co can act as generation centers by forming deep levels in Si. However, the silicides formed by this approach have a finer grain size and a smoother silicide/Si interface than those forming the junction first. On the other hand, the high reverse leakage present in the ITM scheme can be reduced greatly by implanting dopant through silicides (ITS).[11] In this technique, the source/drain implants are done after the silicides have been formed by the self-aligned process. The silicide in the source/drain regions is formed on a lightly doped substrate, alleviating many of the problems associated with the poor silicide growth observed on heavily doped n-type Si.[12-14] In addition, much of the implant-induced damage only affects the silicide layer rather than the Si substrate. Therefore, a shorter thermal cycle can be used to anneal out the damage. Several metal silicides, such as $TiSi_2$ [15,16] and $CoSi_2$, [11] have been investigated in this respect. $TiSi_2$ has the lowest resistivity, but its sensitivity to chemicals and oxygen residues during silicidation, possible reaction with SiO_2, and silicide lateral growth leave only a very critical condition for the silicide formation.[17] Some reports showed that Ti could react with the implanted dopants to form the compounds such as TiB_2 and TiAs.[18,19] This compound formation phenomenon makes $TiSi_2$ a less effective diffusion source for B and As. Cobalt has been shown to have promising properties for the application to the salicide process, but $CoSi_2$ suffers from a large volume silicon consumption during silicidation. This may result in a deeper junction than desired.

Pd_2Si has the merits of chemical stability and oxide-endurance. Pd metal also has an important characteristic in that it can penetrate through native oxide and react with Si. [20] This made Pd_2Si have a good contact to Si and stable electric properties. Pd metal is also a heavy metal (with atomic weight equal to 106.4) and can act as a most effective energy barrier to reduce the projection range of implanted ions. Furthermore, the knock-on effect of Pd metal can be neglected during ion implantation. Moreover, Pd_2Si is a metal rich silicide. The reaction volume ratio of silicon to silicide is 0.42 which is far less than 0.94 for $TiSi_2$ and 1.00 for $CoSi_2$. [21] The Pd_2Si formation temperature of Pd_2Si is relatively low, about 100-300°C. [22] These peculiarities make Pd silicide suitable for usage in the low temperature IC process.

In this study, silicided shallow p^+n junctions were fabricated by implanting BF_2^+ ions at various energies into thin Pd_2Si films on Si substrates to a dosage of 5×10^{15} cm^{-2} and subsequent conventional furnace annealing (CFA). Low temperature formation of the Pd-silicided shallow junctions was reported. The impact of implantation conditions on the junction characteristics and high temperature stability of the Pd silicide films were also investigated.

Experimental

(100) oriented, 15-50 Ω-cm, phosphorus-doped, n-type Si wafers were first chemically cleaned by using the standard RCA process. A layer of 5000 Å thick SiO_2 was thermally grown for defining the junction area. After the patterning, a thin Pd film of 500 Å thick was deposited at room temperature in an electron-beam evaporation system with a base pressure better than 4×10^{-6} Torr. Although little influence was found on the Pd silicidation for the native oxide on silicon substrate,[20] the native oxide was removed on the Pd silicidation for the native oxide on silicon substrate,[20] the native oxide was removed by dipping the substrate into dilute HF solution immediately before loading into the electron-beam evaporation system. An amorphous-Si (a-Si) capping layer with 50 Å in thickness was then deposited to prevent the Pd from contamination during silicide formation. A two-step annealing process for patterning the silicide was used. At first, the specimens were annealed at 300°C for 30 min in an N_2 ambient to selectively form Pd_2Si on the exposed Si and then the unreacted Pd on SiO_2 was chemically removed by utilizing the etchants consisting of 40 ml H_2O:8 g KI:1 g I_2 at room temperature. Then the samples were BF_2^+-implanted at energies ranging from 40 to 120 keV to a dose of 5×10^{15} cm^{-2}. Second-step sintering was performed by CFA for 60 min at temperatures ranging from 500 to 750°C.

Simulation of ion implantation was carried out using the TRIM program to estimate the as-implanted dopant pro-

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file. Sheet resistance was measured by four-point probe (FPP) on the unpatterned area, and the junction depth was determined by spreading resistance probe (SRP) measurement. The silicon surface after removal of the silicide layer was inspected by scanning electron microscopy (SEM). The microstructures of the silicide films were analyzed by transmission electron microscopy (TEM). The current-voltage (*I-V*) characteristics of the junctions were measured by a PC-controlled HP-4145B semiconductor parameter analyzer. The open-circuit leakage current of the measuring system was kept below 0.5 pA.

Results and Discussion

In this study, the TRIM (transport of ions in matter) simulation program was used to predict the distribution of as-implanted dopants in Pd silicide and silicon substrate. TRIM has been proven to be more accurate than SUPREM-3 in the case of boron implantation into Co, $CoSi_2$, Ti, and $TiSi_2$.[23] When implanted ions are totally inside the silicide layer, the TRIM simulations seem accurate.[24,25] However, the TRIM simulation program does not take the channeling effect of silicon crystal into account; the actual distribution of the as-implanted ion should go into the silicon substrate deeper than that of the simulation profiles.[26,27] For the BF_2^+ ion implantation, the BF_2^+ ions were believed to dissociate upon their first atomic scattering.[28-30] Therefore, the boron energy could be obtained by multiplying the BF_2^+ energy by the mass ratio of B^+ to BF_2^+, which was 11/49. There are several strategies for employing the ITS technique in junction formation. In this work, we examined the possible implantation and annealing conditions for a Pd silicide film of 700 Å in thickness and evaluated the feasibility of the ITS scheme. TRIM simulation results for BF_2^+ implantation at various energies to a dose of 5×10^{15} cm^{-2} are illustrated in Fig. 1. For the 40 and 60 keV implantation, the implanted dopants are entirely located inside the silicide layer, and no damage to the Si substrate is expected. In this case, the silicide film serves as a diffusion source for the p^+n junction formation during the subsequent annealing treatment. Thus, high diffusivity of boron in silicide is indispensable. The diffusivity of dopants in silicide is orders of magnitude higher than that of single crystal silicon thus making it suitable as a diffusion source. However, dopant evaporation from the silicide (10-70%) during heat-treatment requires a higher dose to preserve junction integrity. For 80 keV implantation, most of the implanted dopants are confined within the silicide, but an implantation tail is left in the SI substrate. We chose the energy of 80 keV to make the dopant concentration at the silicide/silicon interface higher than 5×10^{19} cm^{-3} for an implantation dose of 5×10^{15} cm^{-2} and to keep the projection range within the silicide and far from the silicide/silicon interface. Because the implantation damage is mainly located within the projected range, this energy scheme (80 keV) would produce good diode characteristics provided that most of the implanted dopants are activated. Thus, lower thermal budget, shorter anneal time, and lower implantation dose become practical.

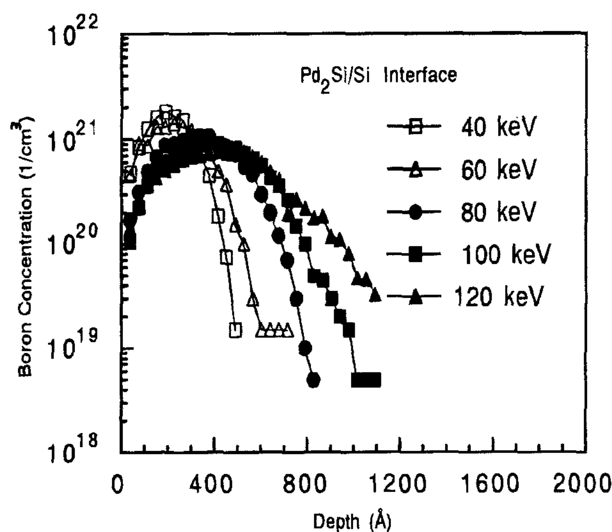

Fig. 1. TRIM simulation result of boron distribution for the ITS samples implanted with BF_2^+ ions at different implantation energies of 40, 60, 80, 100, and 120 keV, respectively.

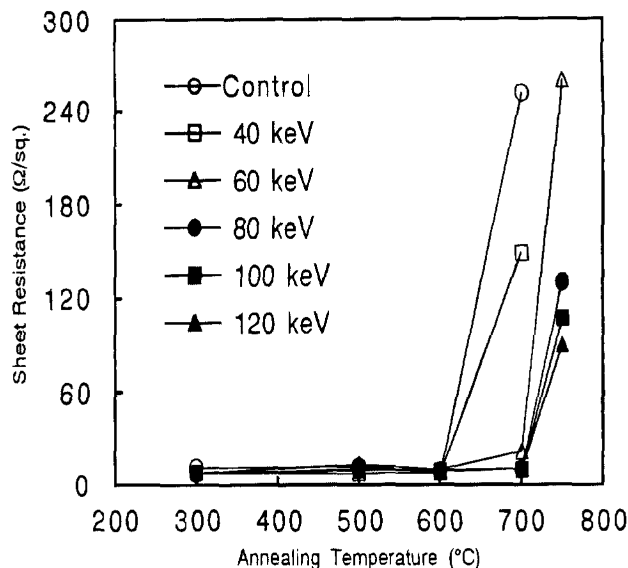

Fig. 2. Curves of sheet resistance R_s vs. annealing temperature for the ITS specimens.

When the implantation energy is raised to 120 keV, the Si substrate is severely damaged in addition to many dopants that are situated in the Si substrate. The implantation damage will cause poor junction characteristics; thus high temperature annealing is needed and the defect enhanced diffusion of dopants make shallow junction impossible.

Figure 2 shows the sheet resistance (R_s) as a function of annealing temperature for the Pd samples implanted with BF_2^+ ions at different energies of 40, 60, 80, 100, and 120 keV. The effective energy of fluorine ions was 16, 24, 32, 40, and 48 keV, accordingly. The unimplanted samples (control samples) were included for comparison. For all specimens, R_s decreased slightly with increasing annealing temperature up to 600°C because of the recovery of the implantation damage and/or the grain growth of the formed silicide. But after an annealing at 700°C, the R_s value increased tremendously for the control samples. The R_s value of the control samples annealed at 700°C was 251.7 Ω/□ The increase of sheet resistance of the silicide layer was due to the formation of islands (which causes discontinuous structure of the silicide film) at high annealing temperature, as shown later in the SEM photographs. In contrast, the BF_2^+-implanted samples show a very different situation. The R_s value of the samples implanted with the lowest energy (40 keV) increased to 149 Ω/□ after a 700°C annealing, and the 60 keV implanted sample showed less increase in the R_s value (21.8 Ω/□). When the implantation energy was raised above 80 keV, the R_s value remained stable at 700°C but increased drastically after 750°C annealing. Higher energy implantation conditions exhibited lower R_s values.

Figure 3 shows TRIM simulation results of as-implanted fluorine distributions in Pd_2Si/Si structure for various implantation energies. The percentage of fluorine atoms within 510 ~ 910 Å was used to inspect the effect of fluorine near the interface. For the 40 and 60 keV implantation, the as-implanted fluorine atoms situated in the silicide/silicon interface region are 0.37 and 2.4%, respectively. This ratio raises to 10% for an energy of 80 keV and becomes 24.3% for the 100 keV implantation. For the 120 keV implantation, the ratio is 33.7. At annealing temperatures of 700 and

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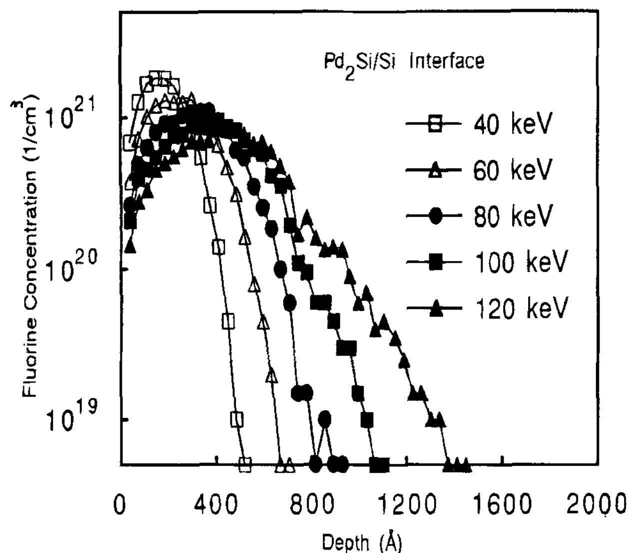

Fig. 3. TRIM simulation result of boron distribution for the ITS samples implanted with BF_2^+ ions at different implantation energies of 40, 60, 80, 100, and 120 keV, respectively.

750°C, the variation tendency of the amount of fluorine at the silicide/silicon interface *vs.* implantation energies is consistent with that of the sheet resistance of silicide with respect to the implantation energies. Hence, it is reasonable to believe that high temperature stability of thin silicide films is dependent upon fluorine concentration around the silicide/silicon interface. Figure 4 shows the secondary ion counts of fluorine ions at the silicide/silicon interface after 700°C annealing for the 40 and 100 keV implanted samples. It clearly shows that the fluorine concentration at the silicide/silicon interface is much higher for the 100 keV implanted samples, which is consistent with the TRIM results. So the 100 keV implanted specimens show better thermal stability than the 40 keV implanted samples.

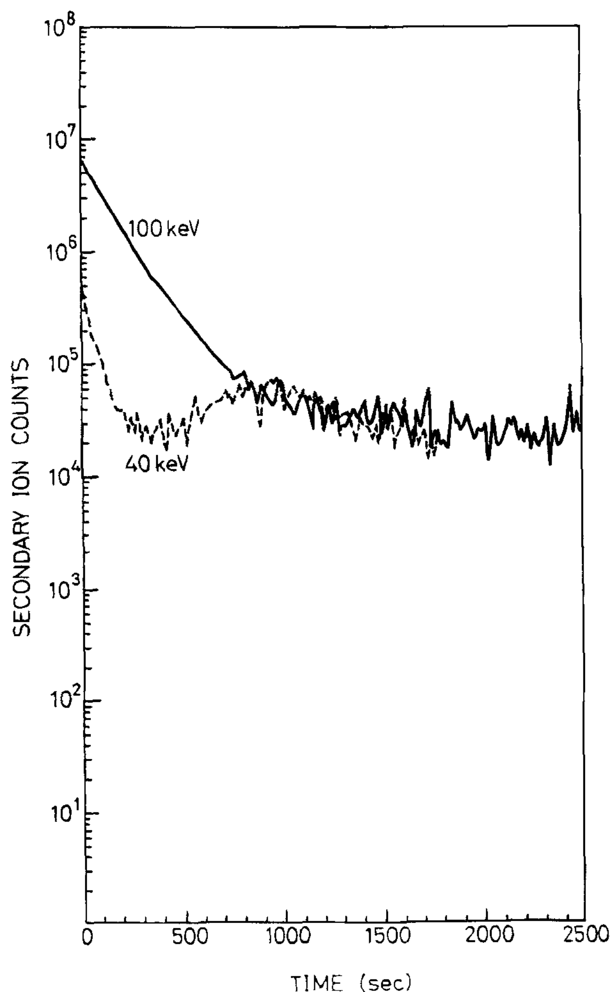

Fig. 4. Secondary ion counts of fluorine ions at the silicide/silicon interface after 700°C annealing for the 40 and 100 keV implanted samples.

Figure 5(a)-(c) are SEM micrographs of the silicon surfaces after the removal of the silicide layers for the control sample, 40 keV, and 80 keV implanted samples annealed at 700°C. Obviously, thermal grooving phenomenon appeared at the silicide/silicon interface for the control samples and larger etching pits were observed on the silicon surface after the silicide was stripped off. In other words, the silicide film exhibited island structure because the severe agglomeration of the silicide films. The formation of island structure led to large increase in the R_s value because the film is discontinuous. No evident grooving effects was observed for the 80 keV implanted samples. For the 40 keV implanted samples, less thermal grooving than the control samples were observed. It is consistent with the results of the sheet resistance measurements. Previous literature has reported that a large interface energy would help to resist the film agglomeration.[31,32] Hence, the smoother silicide/silicon interface of the implanted samples would be explained from this point of view. Presumably, the presence of fluorine atoms around the silicide/silicon interface may increase the interface energy.[33] At elevated annealing temperatures, the fluorine effect becomes less efficient because of the larger driving force of the grain boundary migration as well as the decrease of the fluorine concentration at the interface.

Figure 6 shows the SEM micrographs of the silicon surface after the removal of the silicide layer for the 80 keV implanted samples annealed at 750°C. Corresponding to the sheet resistance result, the silicide film was unstable and formed island structures.

The effect of ion mixing of native oxides on the thermal stability of silicide films is not thought to be the major factor in this work, because little influence was found on the Pd silicidation for the native oxide on the silicon substrate.[20] Moreover, according to the results of previous papers dealing with thermal stability of Co and Pt silicide,[33-35] ion mixing effect is not the major factor for the improvement of thermal stability.

Spreading resistance probe (SRP) measurements were used to determine junction depths (measured from Pd_2Si/Si interface) in this work. The results are shown in Table I. For the 60 keV implanted samples, the junction depth was measured to be about 0.12 μm after the 600°C/60 min annealing. Since all the implanted dopants were confined in the silicide film for the 60 keV implantation, the junction must be formed by the diffusion of boron from the silicide during the thermal anneal. Since the diffusivity of boron in silicon is negligibly small at 600°C, our results suggest that the diffusivity of boron in silicon may be enhanced by the presence of silicide film.[36-39] This enhancement in diffusivity is attributable to the vacancy injection from the silicide. For the 100 keV implanted specimens, a deeper junction of 0.16 μm is attained after 600°C/60 min annealing. Hence the implantation damage in the silicon substrates also plays an important role on the enhancement of the boron diffusion. The junction depths for all the samples in Table I after a 550°C annealing are less than 0.15 μm and are suited for ULSIs utility.

Several factors may influence the properties of p^+n junctions fabricated using the ITS scheme. The degree of undulation of the silicide film determines the true distance between the projected range of ions and the silicide/silicon interface. The implantation energy, which is a key factor related to the junction characteristics, affects the dopant concentration in silicon; this is particularly important for the case of medium-dose implantation and low thermal budget.

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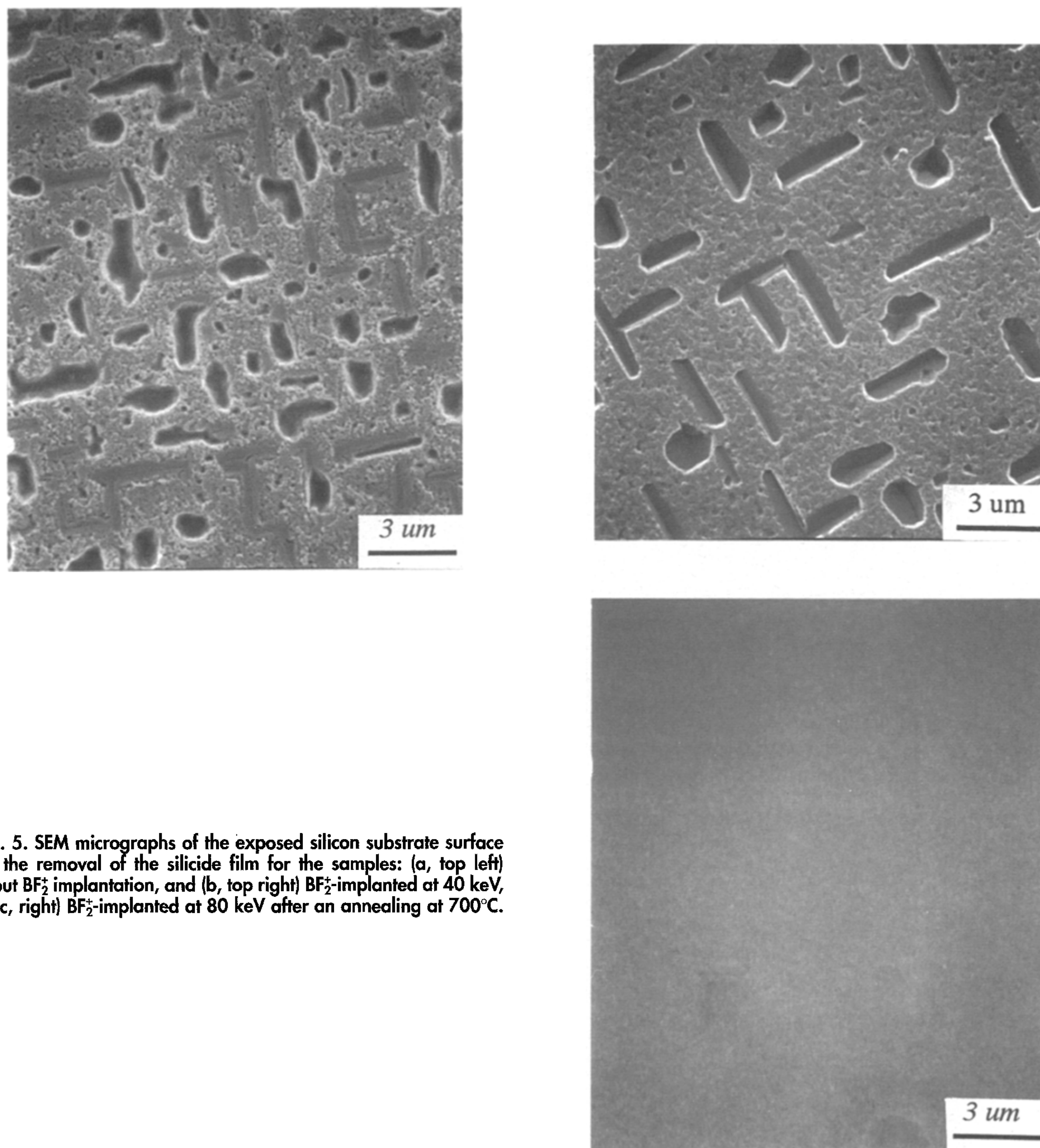

Fig. 5. SEM micrographs of the exposed silicon substrate surface after the removal of the silicide film for the samples: (a, top left) without BF_2^+ implantation, and (b, top right) BF_2^+-implanted at 40 keV, and (c, right) BF_2^+-implanted at 80 keV after an annealing at 700°C.

It should be noted that the dopant activation level for the BF_2^+-implanted silicon was much higher than that for the B^+-implanted silicon after a low-temperature anneal (500-600°C).[30] Thus, it was possible to fabricate a high-quality p^+n diode at a low temperature provided that no significant implant-related defects are introduced.

The forward behavior of a p^+n diode can be described by the following equation

$$I = I_s [\exp(qV/nkT) - 1] \approx I_s \exp qV/nkT \qquad [1]$$

where I_s is the saturation current and n is the ideality factor. The extracted n values are shown in Table II. All the samples were annealed at 700°C for 1 h. The ideality factors are about 1.03 ~ 1.08. It seems that there was no absolute dependence of ideality factor (n) on implantation energy.

The leakage current densities (J_r) of the Pd_2Si silicided p^+n junctions with an area of 0.01 cm^2 measured at a reverse bias of -5 V are given in Fig. 7. All measurements were performed at room temperature, and each value was obtained by averaging more than ten randomly selected diodes. The J_r was determined by directly dividing the measured current by the diode area. It is obvious that the leakage current density at about 3 nA/cm^2 can be easily achieved for 80 and 100 keV implanted samples annealed at 550°C for 60 min. Thus the ITS scheme is promising in low-temperature processing.

For a p^+n diode with a shallow implantation with the ITS scheme, the diffusion current may exceed the generation-recombination component and dominate the reverse behavior. For the samples implanted at 40 and 60 keV, annealing at 550 and 600°C resulted in a insufficient doping and thus led to poor leakage characteristics because of the increased reverse current, which was now dominated by the diffusion component. In addition, a lightly doped p region was always accompanied by a high metal/silicon contact resistance. It is apparent that a higher dose implantation must be performed for the 40 and 60 keV implant to increase the dopant level so that good junction performance can be obtained. When an implantation dose of 1×10^{16} cm^{-2} at 60 keV is performed, a J_r value less than 10 nA/cm^2 is obtained by a 550°C/60 min annealing.

From this figure, J_r values of the diodes are reduced when annealing temperature is raised from 500 to 550 to 600°C because of higher dopant activation/drive-in efficiency

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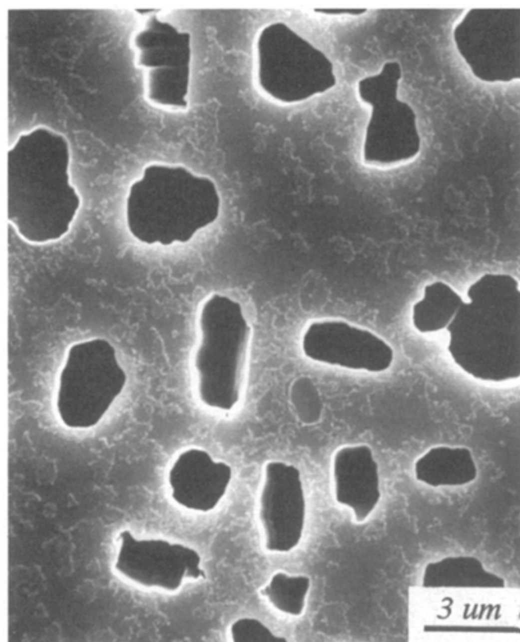

Fig. 6. SEM micrograph of the samples BF_2^+-implanted at 80 keV and subsequently annealed at 750°C.

and better damage annihilation. J_r values at about 3 nA/cm^2 were obtained for the samples implanted at 80 and 100 keV after a 550°C/60 min annealing, and the junction depths were 0.09 and 0.12 μm, respectively. After a 600°C annealing, further improvement was observed. For the ITS scheme, the damage is mostly confined in the silicide region and the vacancy injection during annealing of silicide thus enhances defect annihilation, with both contributing to the low J_r values of the diodes. The implantation energy also shows impact on the characteristics of the diodes. Implantation energies at 40 and 60 keV confined all the dopants in the silicide films, so the lower dopant concentration resulted in larger J_r values than the 80 and 100 keV implantation cases. On the other hand, high energy implantation (120 keV) also resulted in large J_r values at all annealing temperatures because the Si substrates were severely damaged. Consequently, the medium energy (80 and 100 keV) resulted in better diode characteristics at 550°C because the implantation tail into the Si substrate led to higher dopant concentration than the low energy case and also much less damage than the high energy case.

Several factors would influence the characteristics of the ITS junctions fabricated at high temperatures. At first, boron diffusion became prominent, and deeper junctions were expected leading to a decrease in J_r. Second, a higher damage recovery level also resulted in lower J_r. However, the roughness of the silicide film would cause the formation of a local Schottky contact[40] or lightly doped p-n junction, which would increase the J_r value. In addition, the roughness would also thin the thickness of the junction buffer layer and enhance the electrical field to increase the leakage current. The ultimate electrical properties of the junctions depend on which factor was dominant.

For the Pd_2Si silicided junctions after an annealing at 700°C, 70 keV case tended to degrade. It could be attributed to the formation of silicide islands at 700°C annealing. The formation of island structure of the silicide films, and the

Table I. List of junction depth (in units of μm) of ITS diodes after annealing at 550 and 600°C, respectively.

Implantation energy (keV)	550°C	600°C
60	0.07	0.12
80	0.09	0.13
100	0.12	0.16

Table II. List of ideality factors of ITS diodes after annealing at 700°C.

Implantation energy (keV)	n value
40	1.0871
60	1.0375
80	1.0439
100	1.0504

associate severe interface roughness of the structure led to the penetration of silicide through the junction, so the diodes degraded after a 700°C annealing. Not all the diodes degraded seriously at 700°C annealing, and the larger the implantation energies, the more stable the diodes. It was because the higher implantation energy made the junction deeper and the thermal grooving of the Pd silicide would show less impact on the junction characteristics of the deeper junction. Another cause was that the higher implantation energy possesses many more fluorine atoms distributed at the silicide/Si interface to improve the thermal stability of the silicide. However, for the 80 keV implanted samples, although no island formation occurred at 700°C annealing, the J_r value increased slightly to about 7-8 nA/cm^2, probably due to greater undulation at the silicide/silicon interface after 700°C annealing for this shallow junction. In addition, dopant evaporation from the silicide surface also became serious at high temperature and also was thought to be responsible for this degradation.

Figure 8 illustrates a typical *I-V* characteristic of a Pd_2Si/p^+n junction processed with 100 keV/5 × 10^{15} cm^{-2} BF_2^+ implantation followed by a 550°C/60 min anneal. From this curve, it is clear that Pd_2Si can serve as an effective diffusion source for boron during low-temperature annealing. With proper processing conditions, performance of Pd-silicided shallow junctions fabricated with the ITS technique using low thermal budget is comparable to that of conventional junctions fabricated by a higher temperature process.

Conclusions

In this experiment, excellent p^+n diodes have been fabricated using Pd_2Si as the implantation barrier. Good diode with an ideality factor of about 1.05 and a leakage current at about 3 nA/cm^2 could be obtained under annealing temperatures as low as 550°C. Implantation of BF_2^+ ions near the silicide/silicon interface was found effectively to stabilize the silicide films after high temperature annealings. The degradation of Pd silicide films at high temperature annealings would induce large reverse current because of the penetration of the silicide through the junction for the

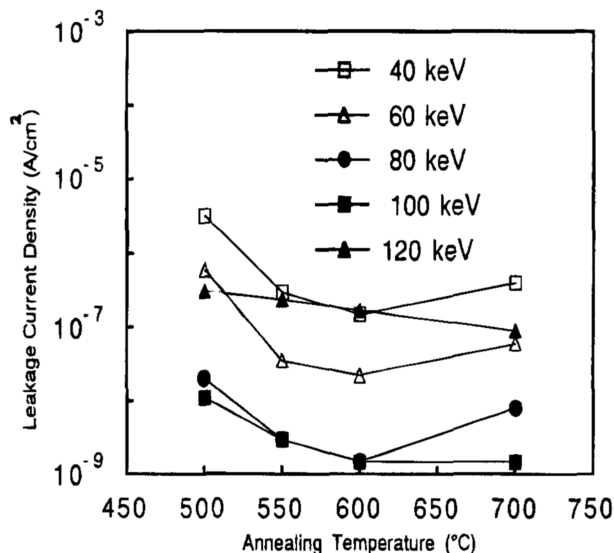

Fig 7. The curves of leakage current density against annealing temperature for the Pd_2Si/p^+n diodes fabricated by ITS process.

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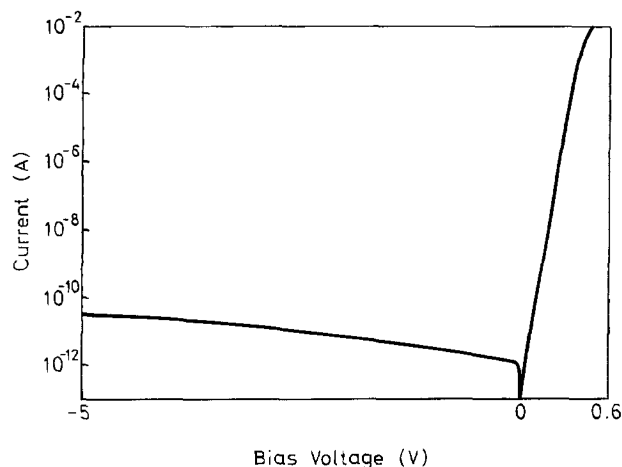

Fig. 8. Forward and reverse current of the p⁺n diodes implanted at 100 keV and subsequently annealed at 550°C.

energy implant conditions. The improvement of thermal stability for the silicide films by the higher energy implantation resulted in good characteristics even after high temperature annealing. However, too high an implant energy will damage the silicon substrate and cause high current leakage. Hence, implantation energy is the key step for the ITS scheme to obtain better high temperature stability of the silicide films and excellent Pd-silicided junction diodes.

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