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Flip-Chip Packaging of Low-Noise Metamorphic High Electron Mobility Transistors on Low-Cost Organic Substrate

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The rapid growth of high-frequency wireless communication demands high-performance packaging structures at low cost. A flip-chip interconnect is one of the most promising technologies owing to its low parasitic effect and high performance at high frequencies. In this study, the in-house fabricated $In_{0.6}Ga_{0.4}As$ metamorphic high electron mobility transistor (mHEMT) device was flip-chip-assembled using a commercially available low-cost organic substrate. The packaged device with the optimal flip-chip structure exhibited almost similar DC and RF results to the bare die. An exopy-based underfill was applied to the improvement of reliability with almost no degradation of the electrical characteristics. Measurement results revealed that the proposed packaging structure maintained a low minimum noise figure of 3 dB with 6 dB associated gain at 62 GHz. Such a superior performance after flip-chip packaging demonstrates the feasibility of the proposed low-cost organic substrate for commercial high-frequency applications up to the W-band. © 2011 The Japan Society of Applied Physics

1. Introduction

The demand for communication systems at frequencies up to the W-band has been growing rapidly in recent years because such systems have the potential of providing high data transmission rates.[1,2] The high-frequency performance of these systems mainly depends on the device characteristics and packaging structure. In terms of the device technology, indium-rich $In_xGa_{1-x}As/In_xAl_{1-x}As$-based metamorphic high electron mobility transistors (mHEMTs) are gaining increasing popularity owing to the high electron mobility and saturation velocity of the InGaAs materials, which in turn delivers a lower noise figure with higher gain at high frequencies.[3–6]

The packaging structure is also an essential issue for practical implementation concerns. Generally, such a structure should provide a reliable transmission path from chip to substrate and protect the device from external hazards, such as environmental effects, mechanical stress, and humidity.[7] Conventionally, the chip is assembled on ceramic-based substrates, such as Al_2O_3,[8] and then the ceramic-based substrates are integrated into the systems made of printed circuit boards (PCBs).

Despite the major advantages provided by the flip-chip packaging, such as good thermal management, good mechanical stability, and high reliability,[9–11] mounting ceramic-based substrates onto PCBs unavoidably introduces additional transitions in signal paths, which will induce extra parasitic effects to impact the system performance. In addition, the approach also causes additional cost owing to the transition from ceramic substrates to PCBs.

This work is performed to develop a low-cost yet robust flip-chip-on-board (FCOB) technology for high-frequency applications up to the W-band. A commercially available PCB (RO3210 organic substrate from Rogers) was adopted for the feasibility study of the proposed technology. To further improve the reliability of the overall structure, an epoxy-based underfill, which can alleviate the stress on the bump transitions between the chips and the PCB,[12–14] was applied. Possible performance degradations at high frequencies due to the inclusion of the underfill (though with low dielectric constant) were taken care of by the optimal design of the geometries on the RO3210 organic substrate through full-wave electromagnetic simulation.

In the following sections, the in-house fabrication process of the proposed technology is presented in detail. $In_{0.6}Ga_{0.4}As$ mHEMT devices were flip-chip-assembled onto the RO3210 organic substrate to demonstrate the applicability of such a technology to high-frequency applications. The optimal design of the layout patterns on the RO3210 organic substrate was verified by the measurement of flip-chip-bonded 50 Ω transmission lines. To investigate the effect of the epoxy-based underfill on the overall performance, comparisons were performed on the flip-chip-assembled devices with and without underfill injection. Measurement results revealed an insertion loss of less than 1 dB and a return loss lower than 20 dB up to 110 GHz for the flip-chip-bonded 50 Ω transmission lines with an optimal design. For a flip-chip-bonded mHEMT with an optimal transmission line design, a minimum noise figure of 3 dB with 6 dB associated gain at 62 GHz was achieved. The superior performance proves that it is possible to flip-chip assemble mHEMT devices onto commercially available organic substrates for operation up to the W-band at competitive cost.

2. Experimental Procedure

Both the GaAs substrate with 50 Ω coplanar waveguide (CPW) transmission lines and the $In_{0.6}Ga_{0.4}As$ mHEMT device with 150 nm gate length were flip-chip-assembled on the RO3210 organic substrate for performance characterization. The interconnect structure is shown in Fig. 1. The $In_{0.6}Ga_{0.4}As$ mHEMT device with 150 nm gate length used in this study was fabricated using in-house process described in detail in ref. 15. For the passive structures on the RO3210 organic substrate, the fabrication process started with the metallization of the GaAs substrate. The seed layers of titanium (Ti) and gold (Au) metals with thicknesses of 500 and 1000 Å were deposited by an E-gun evaporator. A thin photoresist was patterned for the following gold electroplating of the CPW transmission lines. After electroplating, the thin photoresist and seed layers were removed. The GaAs substrate was then thinned down to 100 µm and diced.

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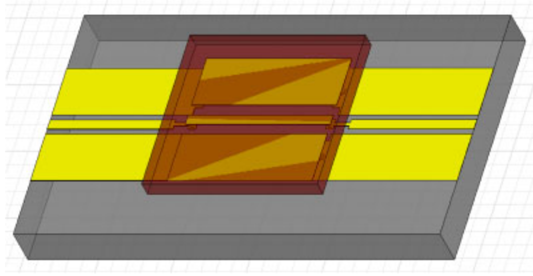

Fig. 1. (Color online) Schematic view of the flip-chip interconnect structure.

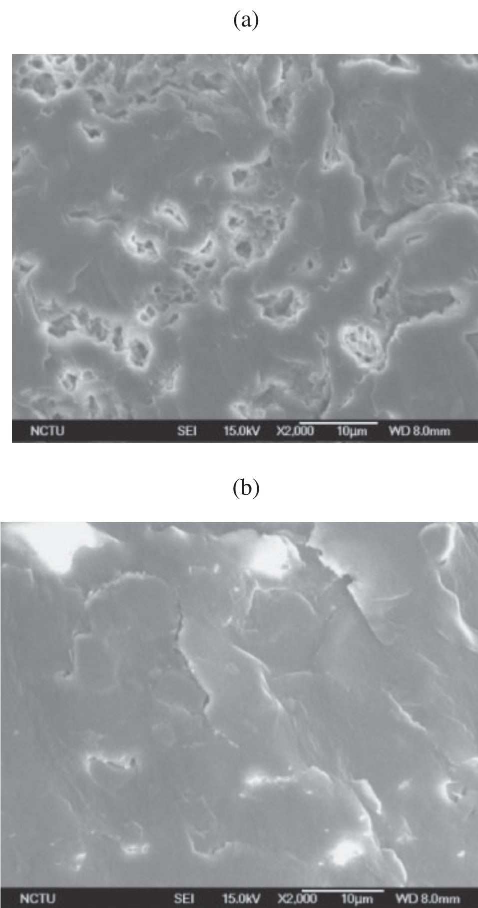

Fig. 2. SEM images of the low-cost RO3210 organic substrate (a) before and (b) after CMP lapping process.

The choice of commercially available PCBs as the substrates instead of the ceramic-based substrates helps to meet the low-cost target. However, surface treatment played an important role in the proposed FCOB technology. Figure 2(a) shows the SEM image of the RO3210 organic substrate, which has a surface roughness of 3 µm. To improve the adhesion between the metallization layer and the PCB substrate, the PCB surface roughness was reduced through a chemical mechanical polishing (CMP) process. Figure 2(b) shows the SEM image of the PCB surface after CMP, where an improvement in surface roughness from 3 to 1 µm can obviously be seen. The flip-chip interconnect structure on the RO3210 organic substrate was in-house-

Table I. Materials properties of epoxy-based underfill.

	T_g (°C)	CTE (ppm/°C)	Moisture absorption (%)	ε_r	tan δ
Epoxy-based underfill	140	46	<1	3.2	0.02

fabricated by photolithography and electroplating. Firstly, the seed layers of Ti and Au metals were deposited by an E-gun evaporator with thicknesses of 500 and 1000 Å, respectively. The Ti layer was used as the adhesion layer between the Au circuit and the RO3210 organic substrate. The CPW transmission line with a characteristic impedance of 50 Ω was patterned on the photoresist and gold-electroplated to a thickness of 3 µm. Then, the thick photoresist for bump transition was performed. Subsequently, the gold bump transition was electroplated with optimization conditions to achieve enough bump height for the following flip-chip bonding process.

After the chip and RO3210 organic substrate were fabricated, the flip-chip bonding process was performed using M9 flip-chip bonder system. The chip was flip-chip-assembled on the RO3210 organic substrate by Au-to-Au thermal compression process with optimization bonding conditions, such as bonding temperature, bonding time, and bonding force.

To improve the reliability, the epoxy-based underfill with low dielectric constant was injected into the gap between the chip and the substrate using an underfill capillary process. The material properties of the underfill are listed in Table I. This underfill has a low viscosity that allows it to flow into the gap between the device and the substrate by capillary force. Finally, the flip-chip structure with the underfill was cured at 150 °C for 2 h in oven. The curing process helps to reduce the air entrapment and increase the reliability of the package itself.

3. Design and Optimization

Prior to the assembly of active devices through the flip-chip bonding process, the high-frequency characteristics of the RO3210 organic substrate were investigated by the measurement of a 50 Ω CPW transmission line. A 50 Ω CPW transmission line designed on the RO3210 organic substrate with a line width of 50 µm and a spacing of 27 µm between the signal trace and the ground, and a length of 854 µm was fabricated and measured. Figure 3 shows the measured results up to 110 GHz using an on-wafer probing system after load–reflection–reflection–match (LRRM) calibration. The simulated results using electromagnetic simulators[16] are also included. The measured and simulated insertion losses (S21) match well with a difference of less than 0.7 dB up to 110 GHz. The measured return loss of the CPW thru line was below 20 dB up to 90 GHz. Generally, the organic substrate exhibited low insertion and return losses for W-band applications.

An underfill is commonly used in flip-chip packaging for reliability improvement. It is clear that the impedance will change with the inclusion of the underfill between the chip and the RO3210 organic substrate since the additional dielectric layer will alter the distribution of the electro-

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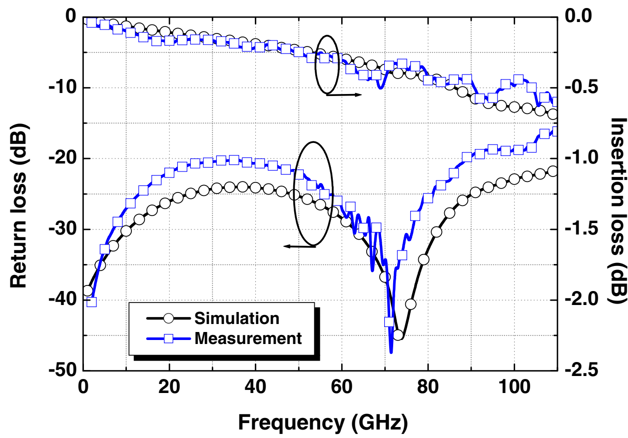


Fig. 3. (Color online) Simulated and measured results of the CPW transmission lines on low-cost organic substrate.

(a)

(b)

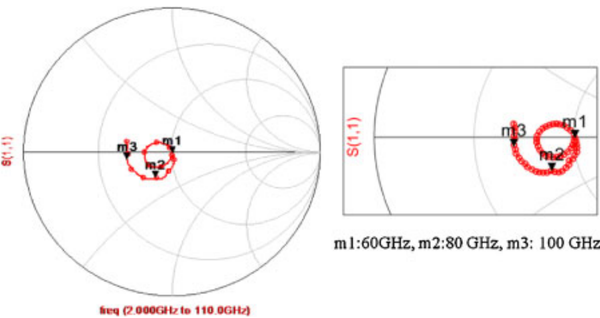
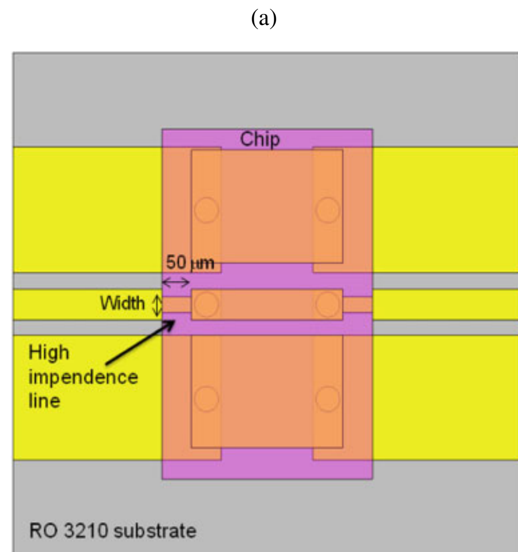


Fig. 4. (Color online) (a) Measured S-parameter of the common flip-chip interconnect structure and (b) Smith chart of the corresponding S_{11} results.

(a)



(b)

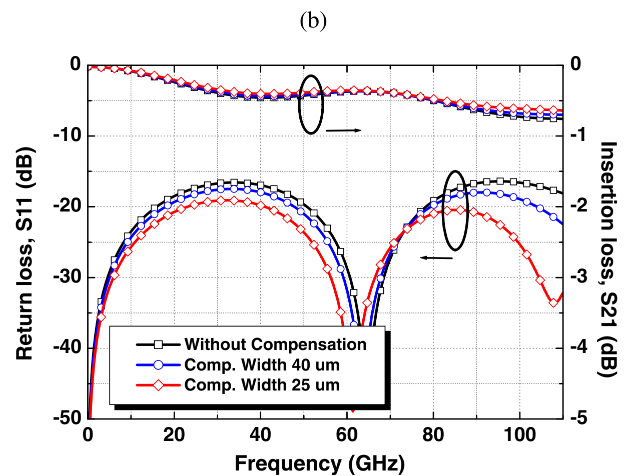


Fig. 5. (Color online) (a) Schematic and (b) simulation results of the compensation design in flip-chip interconnect structure.

magnetic field with the epoxy-based low dielectric constant material adopted. Figure 4(a) shows the measured S-parameters of the 50 Ω CPW transmission line on GaAs flip-chip-assembled on the RO3210 organic substrate with and without the underfill, and the pattern is also included for reference. Cylindrical bumps of 40 μm diameter and 20 μm height were used throughout the structure. As can be observed in Fig. 4(a), both frequency shift and impedance degradation occur at frequencies above 60 GHz for the structure with the underfill compared with the structure without the underfill. The corresponding S_{11} plotted in the Smith chart is shown in Fig. 4(b). It is clearly seen in Fig. 4(b) that the impedance is mainly capacitive at high frequencies. To compensate for this capacitive characteristic of the impedance, a 50-μm-long high-impedance transmission line section was introduced into the RO3210 organic substrate, as shown in Fig. 5(a). Figure 5(b) shows the effect of the width of this high-impedance line simulated using an HFSS simulation tool.[16] Apparently, a length of 25 μm gave the optimal performance over the frequency range of interest. Such an observation was then verified by experiment. Figure 6 shows the measured response of the 50 Ω CPW transmission line on GaAs flip-chip-assembled on the RO3210 organic substrate with the high-impedance line including the optimized compensation structure. As expected, good impedance match is observed up to 110 GHz with an insertion loss of less than 0.6 dB, indicating that excellent transmission properties were obtained from the optimal design.

4. Performance Characterization of the Packaged Device

To demonstrate the capability of the proposed technology for device application, an $In_{0.6}Ga_{0.4}As$ mHEMT device with

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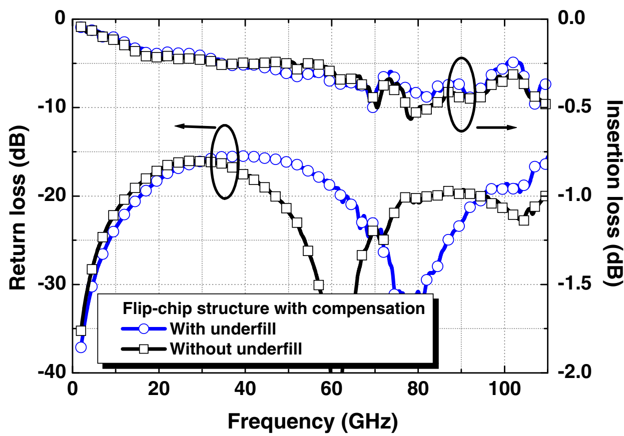

Fig. 6. (Color online) Measured S-parameter results of the optimized flip-chip interconnect structure with and without underfill.

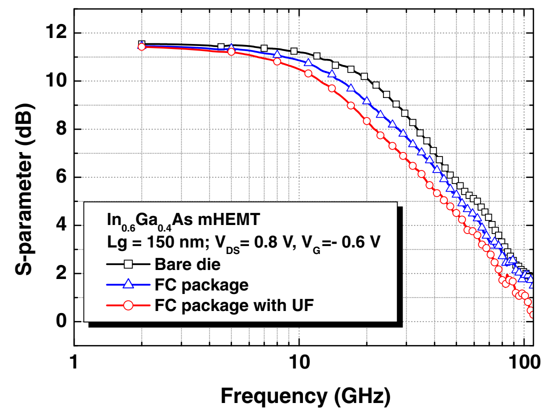

Fig. 8. (Color online) Comparison of insertion gain (S_{21}) between the $In_{0.6}Ga_{0.4}As$ MHEMT device, packaged device, and packaged device with underfill.

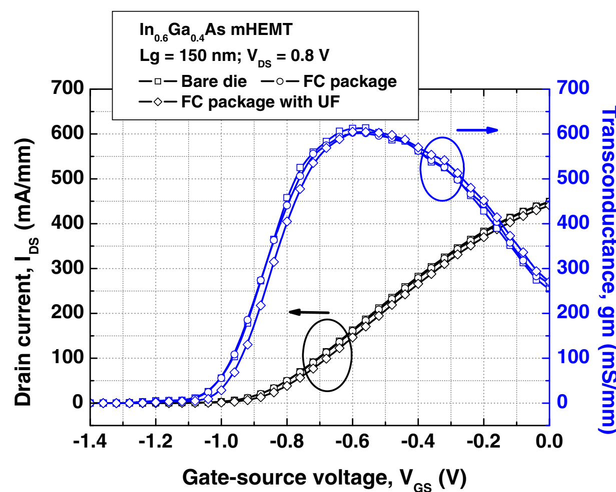

Fig. 7. (Color online) Comparison of drain current density (I_{DS}) and transconductance (g_m) as a function of gate–source voltage (V_{GS}) at $V_{DS} = 0.8$ V between the $In_{0.6}Ga_{0.4}As$ mHEMT device, packaged device, and packaged device with underfill.

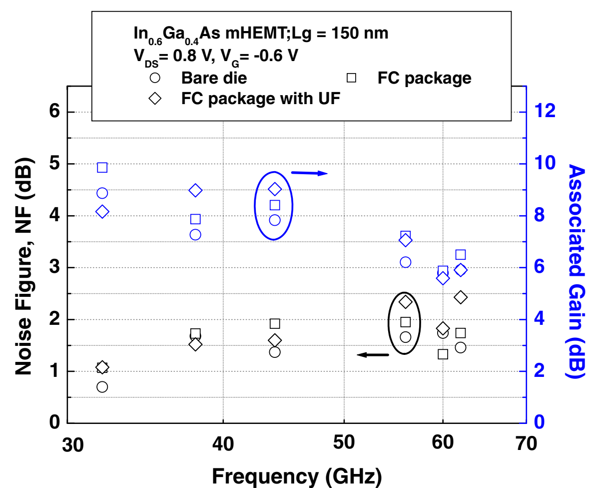

Fig. 9. (Color online) Comparison of the minimum noise figure and associated gain at $V_{DS} = 0.8$ V, $V_G = -0.6$ V between the $In_{0.6}Ga_{0.4}As$ MHEMT device, packaged device, and packaged device with underfill.

150 nm gate length was flip-chip-assembled on the RO3210 organic substrate for performance evaluation. Note that the high-impedance transmission lines used to compensate for the capacitive impedance were included in the patterns on the RO3210 organic substrate to connect the gate and drain of the device. Figure 7 shows the measured DC characteristics where the transconductance (g_m) and drain current (I_{DS}) are plotted as functions of drain voltage at various gate bias levels. Similar performance characteristics were obtained for the flip-chip-packaged device. The RF performance was characterized using an on-wafer probing system with a vector network analyzer up to 110 GHz. Figure 8 shows the measured S_{21} against frequency up to 110 GHz for the bare die, flip-chip-packaged device without the underfill, and flip-chip-packaged device with the underfill. All the devices were biased at peak g_m occurrence with the input and output terminated by a 50 Ω load. A degradation of less than 2 dB was observed for the flip-chip-packaged device with the underfill compared with the bare die over the entire frequency range of interest. The effect of the compensation through high-impedance lines was evidenced by the minor degradation observed for frequencies above 60 GHz. In this aspect, the proposed FCOB approach showed a certain competitive edge over the conventional approach. In ref. 17, a Ka-band LNA MMIC chip was firstly packaged into a ceramic-based QFN package and then integrated into an RO4003C PCB. A gain degradation of 4.5 dB at 40 GHz compared with the bare die case was presented. Finally, the minimum noise figure (NF_{min}) was measured and is plotted in Fig. 9. As is shown, the flip-chip-packaged device with the underfill exhibited an NF_{min} of 3 dB with an associated gain of 6 dB at 62 GHz, indicating promising results of the proposed low-cost FCOB technology for applications in the W-band.

5. Conclusions

In this study, we have successfully demonstrated the FCOB technology for applications in the W-band at very low cost. The main breakthrough for the proposed technology lies in the fact that commercially available organic substrates were used as the carriers instead of conventional ceramic-based

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substrates. Design optimization was performed on the layout patterns of the RO3210 organic substrate through electromagnetic simulations, which also took into account the change in impedance due to the existence of the epoxy-based underfill for reliability improvement. High-impedance lines were introduced into the structure on the RO3210 organic substrate to compensate for the capacitive impedance and thus achieved good transmission properties when the 50 Ω transmission line was flip-chip-assembled. The $In_{0.6}Ga_{0.4}As$ mHEMT device was packaged and characterized with the optimized structure design. The measured DC and RF performance characteristics of the assembled mHEMT using the proposed low-cost FCOB technology showed very promising features, indicating that this technology can be used for applications up to the W-band.

Acknowledgement

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