A Novel Extraction Technique for the Effective Channel Length of MOSFET Devices

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***Abstract*—A novel method using the charge pumping technique for extracting the effective channel length of MOSFET devices is presented, in which the effective area approach is used and the edges of the area are defined clearly. It is shown that the extracted effective channel length is independent of the measuring biases and the proposed new method is simple, accurate, and reliable, as compared to those using the I-V method. With the knowledge of the device dopant profiles, the extracted channel length with 0.01 μm accuracy can be achieved. Moreover, the proposed method is applicable to either n- or p-channel, conventional or LDD, surface or buried channel MOSFET's.**

NOMENCLATURE

V_{FB}	Flat band voltage.
T_{ox}	Gate oxide thickness.
$V_{GH}(V_{GL})$	High (low) voltage of gate pulses.
$T_H(T_L)$	Duration time of high (low) gate bias per cycle.
$L_{mask}(L_{eff})$	Drawn (effective) channel length.
V_g	Gate voltage.
V_T	Threshold voltage.
$V_d(V_s)$	Drain (source) voltage.
p_c	Critical hole concentration at the effective area edges.
p_s	Surface hole concentration.
$R_{hc}(R_{ec})$	Hole capture (emission) rate.
$R_{ec}(R_{ee})$	Electron capture (emission) rate.
v_{th}	Thermal velocity.
$\sigma_p(\sigma_n)$	Hole (electron) capture cross section.
E_i	Intrinsic Fermi energy.
$E_{FP}(E_{FN})$	Hole (electron) quasi-Fermi energy.
n_i	Intrinsic carrier concentration.
n_{it}	Occupied interface-trap density.
N_{it}	Interface-trap density.
$E_c(E_v)$	Energy of conduction (valence) band edge.
q	Elementary charge.
W	Effective channel width.
f	Frequency of gate pulses.
T_p	Period of gate pulses.
x	Lateral position along the channel.
Δx	Distance between metallurgical junction and effective area edge.
I_{cp}	Charge pumping current.
$I_{cp,\,max}$	Maximum charge pumping current per unit length related to the gate waveform along the channel.
$S_R(S_F)$	Absolute slope of the rise (fall) edges of gate pulses.
D_{it}	Average interface trap density.
k_B	Boltzmann constant.
T	Absolute temperature.
$t_{em,\,e}(t_{em,\,p})$	Time for trapped electrons (holes) to emit before recombination.

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I. INTRODUCTION

As the channel length of MOSFET's becomes shorter, the short-channel effects on the device characteristics become very important. In general, the deviations of the channel length from the mask length may come from the errors due to the lithographic process and the lateral diffusion of source/drain islands. The effective channel length of a MOSFET is often defined as the surface spacing between the metallurgical source/drain junction, which may differ from the electrical channel length, depending on the device structure of MOSFET's. In order to accurately characterize the I-V and C-V characteristics of an experimental short channel-length MOSFET, accurate determination of the effective channel length becomes very important.

Up to now, many efforts have been made to find a simple and accurate method to measure the effective channel length of a MOSFET device [1]–[10]. Most of them are based on the turn-on I-V characteristics of MOSFET's operated at low drain bias [1]–[6], in which the method proposed by Terada *et al.* [1] has been used widely and is called the resistance method. However, this method and its modifications [2]–[6] become inaccurate for lightly doped drain (LDD), double diffused drain (DDD) or short-channel MOSFET devices, due to the variations of the source/drain resistances with the gate voltage and the threshold voltage with the channel length. To avoid these problems, some other approaches have been proposed, based on the characteristics of the parasitic bipolar transistor [7], the saturation velocity [8], the punch-through voltage [9], and the gate capacitance [10]. However, the accuracy of the parasitic bipolar transistor and punch-through voltage methods becomes questionable for practical MOS devices with nonuniform substrate dopant profile. For the gate capacitance method, the source/drain overlapping and fringing capacitances are much larger than the intrinsic gate capacitance using the measured C-V data, the errors produced

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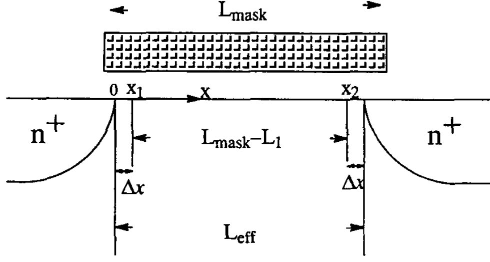


Fig. 1. A schematic device cross section showing the definition of L_{eff}, L_{mask}, L_1 and Δx.

become larger for short-channel MOSFET's. The saturation velocity method seems to be a better one, but the accuracy is dependent on the extraction equation for the saturation velocity.

In this paper, a novel method using the charge pumping technique to extract the effective channel length is introduced. The basic principle of the proposed method is to measure the charge pumping current of a set of MOSFET devices with varying mask lengths. This technique doesn't have the problems of the resistance method and is applicable to conventional and LDD MOSFET's with either surface or buried channel. In Section II, the basic principle of the charge pumping technique for the determination of the effective channel length is presented. The extraction technique using a set of conventional n-MOSFET devices is demonstrated as an example. It is shown that the extracted effective channel length is almost the same for different measuring conditions used. In addition, the proposed method is also applied to the case of LDD n-MOSFET's. Furthermore, the extracted ΔL's are compared to those using the resistance method and a very good agreement is achieved only for the conventional MOSFET's. In Section IV, the possible errors produced by the extraction process are discussed. A conclusion is made in the last section.

II. Basic Principle

The charge pumping technique has been developed to measure the Si/SiO_2 interface-trap parameters in MOSFET devices [11]–[25]. In general, the charge pumping phenomena can be explained by the Shockley-Read-Hall theory [15]. According to the Shockley-Read-Hall theory, the capture and emission rates of electrons and holes through the Si/SiO_2 interface traps can be written as

$$R_{hc}(E_t, x, t) = v_{th}\sigma_p n_i \, exp\,(E_i - E_{FP}) n_{it}(E_t, x, t), \quad (1)$$

$$R_{he}(E_t, x, t = v_{th}\sigma_p n_i \, exp\,(E_i - E_t) \cdot (N_{it}(E_t, x) - n_{it}(E_t, x, t)), \quad (2)$$

$$R_{ec}(E_t, x, t) = v_{t\sigma n} n_i \, exp\,(E_{FN} - E_i) \cdot (N_{it}(E_t, x) - n_{it}(E_t, x, t)), \quad (3)$$

$$R_{ee}(E_t, x, t) = v_{th}\sigma_n n_i \, exp\,(E_t - E_i) n_{it}(E_t, x, t). \quad (4)$$

For the steady state in a periodic waveform, the net electron density transferred in one repetition period (T_p) from the conduction band of the semiconductor to the Si/SiO_2 interface traps located at E_t is equal to that transferred from E_t to the valence band of the semiconductor. As shown in Fig. 1, the net charge density transferred through E_t in one period at the position x along the Si/SiO_2 interface can be expressed as

$$N(E_t, x) = \int_0^{T_p} (R_{ec}(E_t, x, t) - R_{ee}(E_t, x, t))\, dt = \int_0^{T_p} (R_{hc}(E_t, x, t) - R_{he}(E_t, x, t))\, dt. \quad (5)$$

The charge pumping current density at x can be derived by integrating all the Si/SiO_2 interface-trap levels in bandgap and can be written as

$$I_{cpx}(x) = qWf \int_{E_v}^{E_c} N(E_t, x)\, dE_t. \quad (6)$$

Then, the total charge pumping current can be calculated by

$$I_{cp} = \int I_{cpx}(x)\, dx = \int I_{cp,\,max}(x) g(x)\, dx \quad (7)$$

where $g(x)$ is a shape function with the value between 0 and 1. It is clear that only the Si/SiO_2 interface traps in the region where the silicon surface being cycled between accumulation and strong inversion will contribute to the charge pumping current. If the edges of this area are sharp, the "effective area" approach will be very accurate. This means that $g(x)$ is equal to 1 in the effective area and equal to 0 outside the area. If the interface-trap density is constant along the channel and the source/drain proximity effect [25] due to the potential perturbation near the source/drain junctions can be ignored, $I_{cp,\,max}(x)$ in (7) is a constant and is equal to $I_{cp,\,max}$, then (7) can be simplified as

$$I_{cp} = I_{cp,\,max} L_{cp} \quad (8)$$

where L_{cp} is the effective length of the effective area. From (8) and Fig. 1, the L_{cp} can be expressed as

$$L_{cp} = L_{mask} - L_1. \quad (9)$$

Note that the uniformity of the interface-trap density along the channel, the source/drain proximity effect, and the sharpness of the effective area edges will be discussed later.

The basic principle of the proposed method is to measure the charge pumping currents from a set of MOSFET devices with varying mask lengths. Plotting (8) versus L_{mask}, the intercept L_1 at the L_{mask} axis can be derived.

If the distance from metallurgical source/drain junctions to the nearby surface depletion edges under the gate is defined as Δx and the source/drain islands are symmetrical, as shown in Fig. 1, the effective channel length can be expressed as

$$L_{eff} = L_{cp} + 2\Delta x = L_{mask} - \Delta L \quad (10)$$

where ΔL is the difference between L_{mask} and L_{eff} and can

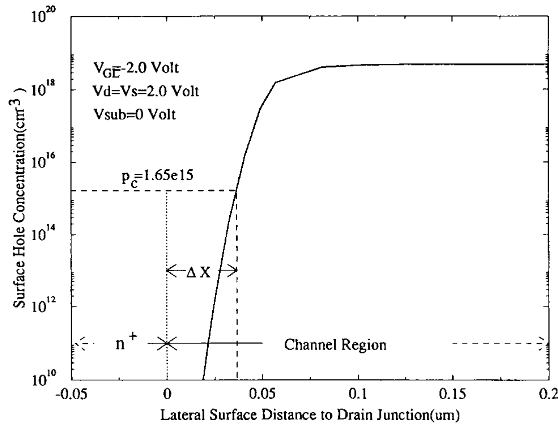


Fig. 2. The method for determining Δx for a specified p_c using a 2-D device simulator.

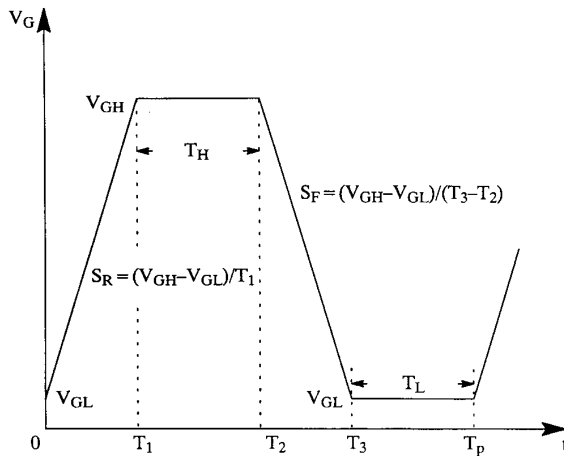


Fig. 3. Gate pulses used and the definition of the related parameters.

be expressed as

$$\Delta L = L_1 - 2\Delta x. \tag{11}$$

To obtain Δx, the edges of the effective length must be determined. Note that the magnitude of Δx is dependent on the applied source/drain bias during the charge pumping measurement. Due to the nonideal charge pumping current shape, the surface depletion edges of the effective length is defined as $g(x_1) = g(x_2) = 0.5$. From [24], when T_L is kept constant and V_{GH} strongly inverts the silicon surface, the half-maximum of I_{cp}/f is only related to a specified surface hole concentration which is defined as the critical hole concentration (p_c). With the specified p_c, the Δx can be obtained easily from a 2-D device simulator, as shown in Fig. 2.

To obtain p_c, the I_{cp}/f versus V_{GL} curve of a long-channel MOS device should be measured because the charge pumping current contributed by the source/drain proximity effect can be ignored. The applied gate waveform is shown in Fig. 3,

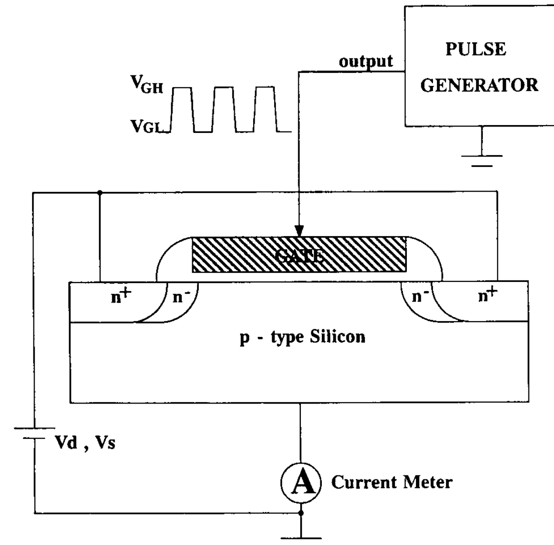
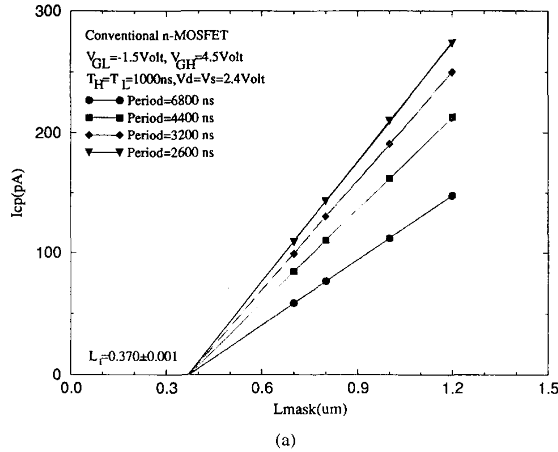


Fig. 4. Setup used for the charge pumping measurement.

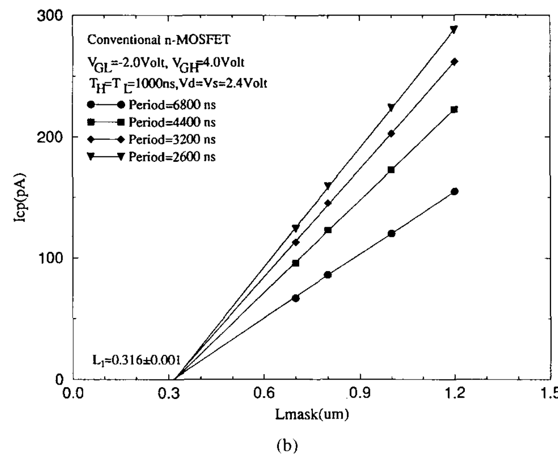
in which V_{GH} is kept constant to strongly invert the silicon surface; T_H is a constant and is long enough to fill all the "effective interface traps" with electrons during V_{GH}. The "effective interface traps" is defined to be all the interface traps that can contribute the charge pumping current. T_L and S_R/S_F are kept the same as those used to derive L_1 and the period changes with V_{GL}. It should be noted that the waveforms used should be careful to prevent the effect of the geometric current. From the I_{cp}/f versus V_{GL} curves, the gate voltage related to the half-maximum of I_{cp}/f can be derived. Then, the critical hole concentration in the channel can be calculated using a numerical 2-D device simulator. Using the similar waveforms to measure L_1, the edges of the effective area, named x_1 and x_2 shown in Fig. 1, can be defined as the positions where the surface hole concentration is p_c at V_{GL}. Since the hole concentrations near x_1 and x_2 vary rapidly, the "effective area" assumption is reasonable. The error introduced from this assumption will be discussed in Section IV.

III. Experimental Method and Results

The experimental transistors used to demonstrate the novel method in detail are n-channel MOSFET's with different drawn channel lengths of 0.7, 0.8, 1.0, and 1.2 μm and the channel width of the devices is 100 μm. The related device parameters are listed in Table I. The setup used for the charge pumping measurement is illustrated in Fig. 4. Several S_R and S_F values of the gate pulses are used to extract L_1 while V_{GL} and T_L are kept the same. With the same V_{GL} and T_L, the effective area is kept the same. As shown in Fig. 5, the extracted L_1 using different S_R and S_F are almost the same with a standard deviation of about 0.001 μm. This means that the extracted results are insensitive to the measuring gate waveforms and the error introduced from the measurement itself is small. Note that the V_{GL} value used is -1.5 V for Fig. 5(a) and -2.0 V for Fig. 5(b). It should be noted that

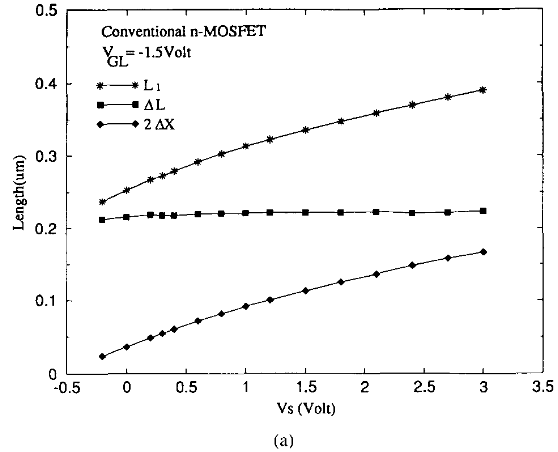


(a)

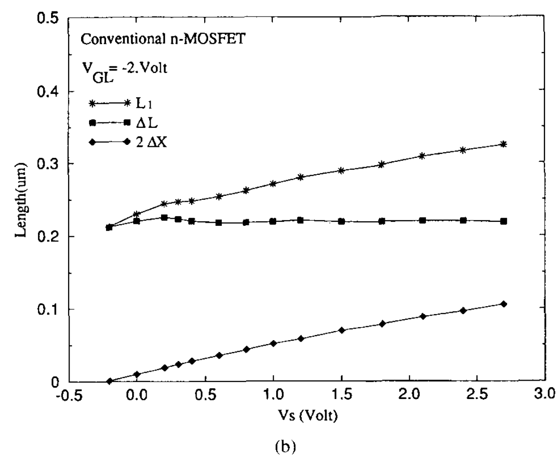


(b)

Fig. 5. The L_1 extraction from the conventional nMOSFET's using several waveforms with $T_H = T_L = 1000$ nsec, $V_S = V_D = 2.4$ V. (a) $V_{GL} = -1.5$ V, $V_{GH} = 4.5$ V. (b) $V_{GL} = -2.$ V, $V_{GH} = 4.$ V.



(a)



(b)

Fig. 6. The extracted L_1, $2\Delta x$ and ΔL versus different V_S/V_D with (a) $V_{GL} = -1.5$ V. (b) $V_{GH} = -2$ V.

the applied source/drain biases are restricted to a range so that the source/drain junction leakage current is much smaller than the charge pumping current. As the source/drain reverse bias increases, the junction depletion width at a fixed V_{GL} increases and the effective area becomes smaller. Therefore, the deduced L_1 increases with the source/drain bias, as shown in Fig. 6. Usually, the Si/SiO_2 interface-trap density is constant in the channel region and may vary near the source/drain junctions [23] due to the variations of dopant concentration near the source/drain junctions and the mechanical stresses at the polysilicon-gate edges. If the interface-trap density increases near the effective area edges, the deduced ΔL will be underestimated. Therefore, we should choose proper measurement conditions so that the effective area edges may locate in the channel region.

To suppress the current ratio induced by the source/drain proximity effect, the long-channel devices are suggested to be used to derive the I_{cp}/f versus V_{GL} curves. However, the device with the drawn channel length of 100 μm is the only-long channel device in our test pattern. For such a long channel device, the S_R and S_F of the gate pulses should keep small to prevent the geometric current, as shown in Fig. 7(a) ($S_R = S_F = 100$ V/sec). Such low-frequency waveforms are not suitable for the charge pumping current measurement of the short-channel devices, because the measured current will be too small (near the resolution of the current meter) to derive L_1 accurately. Therefore, the charge pumping current difference of two MOSFET's with different L_{mask} are used to derive p_c, as shown in Fig. 7(b). Using this method, we can derive the I_{cp}/f versus V_{GL} curves at high frequencies without both the source/drain proximity components and the geometric component of charge pumping current. Using the device dopant profiles derived from the calibrated SUPREM IV process simulator for a two-dimensional device simulator, the surface hole concentration related to the half-maximum of I_{cp}/f can be calculated. The derived p_c is 1.65E15 cm^{-3}. Note that the accuracy of the substrate doping profile had been verified by simulating the subthreshold current versus different back-gate biases.

The L_1 and $2\Delta x$ related to the source/drain bias with $V_{GL} = -1.5$ and -2 V are shown in Fig. 6(a) and (b), and the ΔL

TABLE I
DEVICE PARAMETERS OF THE MOSFET'S USED IN THIS PAPER

Parameters \ Devices	Conventional n-MOSFET	LDD n-MOSFET
V_{FB}(Volt)	-0.845	-0.845
T_{OX}(nm)	14.3	14.0
Junction Depth(μm)	0.22 (n^+)	0.25 (n^-)
Substrate Dopant Concentration(cm^{-3})	3.5E15	1.E15
Implantation Dose 1 (cm^{-2})	1.04E13	1.58E12
Implantation Depth 1 (μm)	0.513	0.27
Standard Deviation of Implantation 1 (μm)	0.753	0.113
Implantation Dose 2 (cm^{-2})		1.57E12
Implantation Depth 2 (μm)		0.022
Standard Deviation of Implantation 2 (μm)		0.061

derived from (11) are 0.220 and 0.219 μm, respectively. Fig. 8 shows the deduced ΔL using the resistance method. Compared to the extracted ΔL using the charge pumping method, the resistance method overestimates the ΔL value for low gate voltage ($V_{GS} - V_T - 0.5V_{DS} < 1.0$V) due to the invalidity of the linear-region current equation used and underestimates the ΔL value for high gate voltage ($V_{GS} - V_T - 0.5\ V_{DS} >$ 1.0 Volt) due to the inclusion of n^+ tail. Compared to the resistance method, the charge pumping method has a smaller extraction deviation and is self-consistent at any measurement condition.

One of the major advantages of the charge pumping method is that it is suitable to all kinds of the MOSFET devices with substrate contacts. A set of LDD nMOSFET's are used for the ΔL extraction, the drawn channel lengths are 0.6, 0.7, 0.8, and 0.9 μm, respectively. The ΔL extraction process is the same as that applied to the conventional nMOSFET's. The device parameters are also listed in Table I. For the LDD devices, the measurement error for L_1 is still small and the derived ΔL is 0.26 μm, as shown in Fig. 9 and Fig. 10(a). The reliable ΔL values are derived from the higher source/drain voltages, because the edges of the effective area may locate in the channel region. The interface-trap density near the source and drain junctions could be higher than that in the channel, and this will introduce the underestimation of ΔL if the effective area edges are located near the source/drain region. For comparisons, the ΔL values derived from the resistance

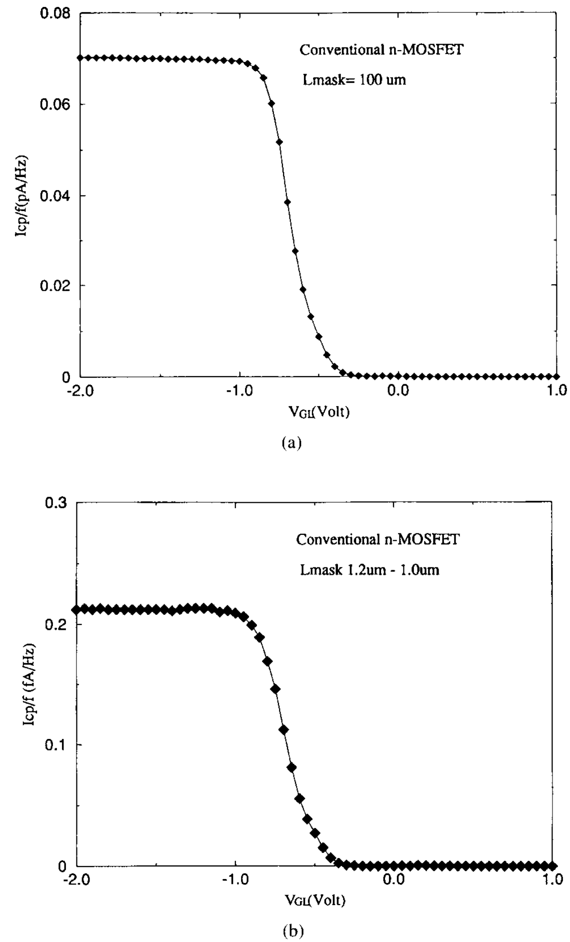


Fig. 7. The I_{cp}/f–V_{GL} curve derived from (a) A single n-MOSFET with $L_{mask} = 100\ \mu$m. (b) The difference of two n-MOSFET devices with different L_{mask}.

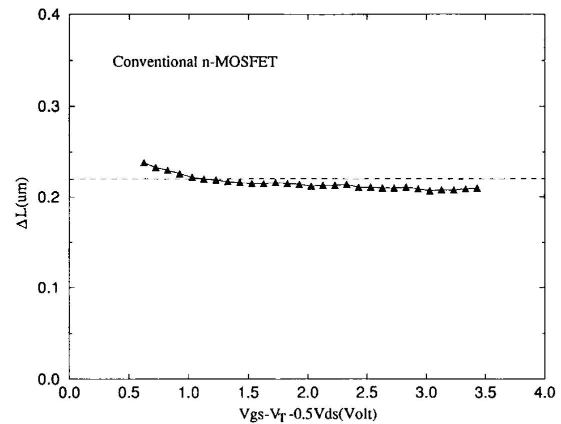


Fig. 8. The extracted ΔL from the conventional n-MOSFET devices using the resistance method.

method are shown in Fig. 10(b). It is clearly seen that the extracted ΔL's using the resistance method are strongly gate-

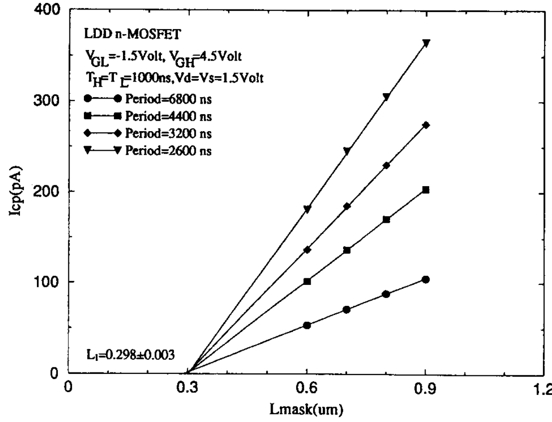


Fig. 9. Charge pumping current versus L_{mask} for several frequencies to derive L_1 from the LDD nMOSFET.

bias dependent. Similarly, the resistance method overestimates the ΔL value for low gate voltage and underestimates the ΔL value for high gate voltage. Therefore, the charge pumping method becomes important to extract the metallurgical channel length, especially in the case of LDD devices.

IV. Discussion

The accuracy of this new technique and the validity of several assumptions used are discussed in this section. Conventional n-channel MOSFET's are used as an example. The errors introduced by the deviation of p_c, the waveform rise/fall slopes, the effective area approach, and the source/drain proximity effect are discussed.

A. p_c Deviation and Waveform Rise/Fall Slopes

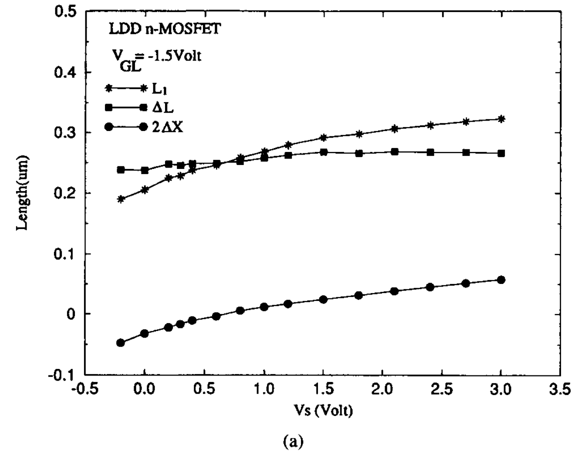
The p_c is a key parameter of this extraction technique. If the derived ΔL is sensitive to p_c, a serious error can be generated due to a bad estimation of p_c. For example, if 50% error for the substrate dopant profiles is given by SUPREM IV, then about 100% error of p_c is produced. To discuss the sensitivity of ΔL related to p_c, we calculate $2\Delta x$ related to both $p_c =$ 1.65E15 and 3.3E15 cm^{-3}, as shown in Fig. 11. The $2\Delta x$ (or ΔL) deviations due to 100 % p_c error are still acceptable and are less than 0.007 μm. Besides, according to the recent study [24], the p_c is only sensitive to T_L. Therefore, the p_c variation related to the four S_R/S_F values used in Fig. 5(a) and (b) are small and the induced ΔL difference can be ignored.

B. The Effective Area

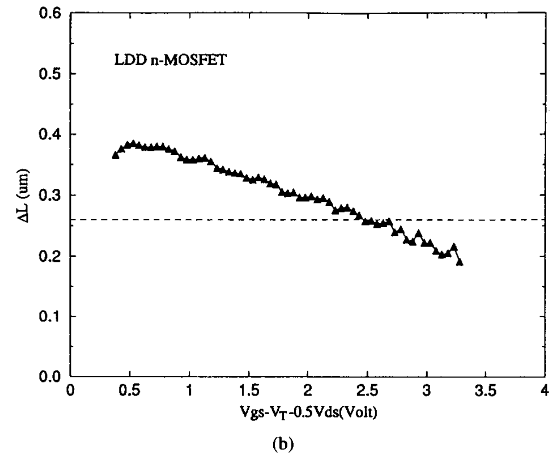
The effective area approach is used for the simplicity of the ΔL extraction shown in Section II. If $I_{cp,\,max}(x)$ is constant along the channel, then $I_{cp}(x)$ is only related to the surface hole concentration of x at V_{GL} [24]. The total charge pumping current can be expressed as

$$I_{cp} = I_{cp,\,max} \int g(p_s(V_{GL},\,x))\,dx \tag{12}$$

where $g(p_s)$ is the weighted factor related to the surface hole concentration. The $g(V_{GL})$ can be derived easily from the



(a)



(b)

Fig. 10. LDD nMOSFET devices. (a) L_1, $2\Delta x$ and ΔL versus V_S/V_D. (b) ΔL extracted from the resistance method.

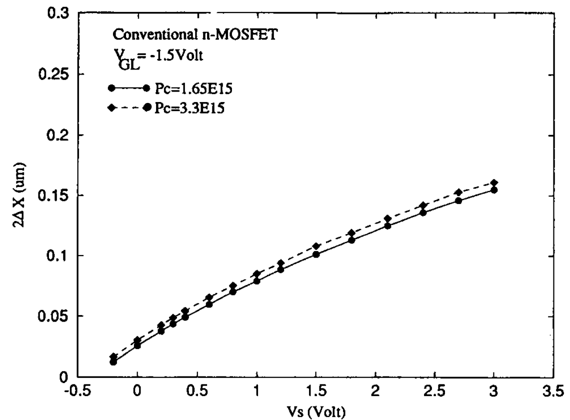


Fig. 11. $2\Delta x$ versus V_S/V_D with critical hole concentration of $p_c =$ 1.65E15 and 3.3E15 cm^{-3}.

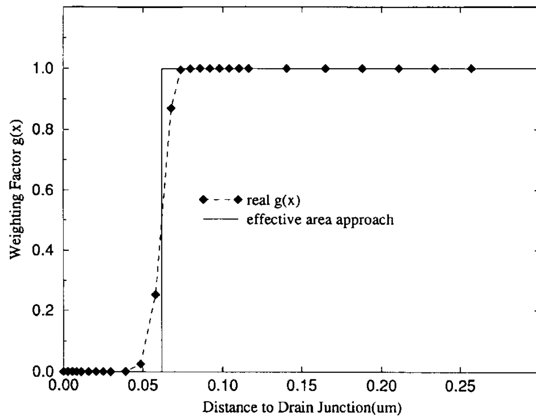


Fig. 12. Real weighting factor and the weighting factor of effective area approach along the channel.

I_{cp}/f versus V_{GL} curves in Fig. 7(b). The I_{cp}/f in Fig. 7(b) can be expressed as

$$I_{cp}/f = (I_{cp,\,max}/f)\Delta L_{mask}\, g(V_{GL}(p_s)) \quad (13)$$

where ΔL_{mask} is the drawn channel-length difference of two devices. Using a numerical 2-D device simulator to calculate the relation between V_{GL} and p_s, the $g(p_s)$ can be derived.

On the other hand, the weighted factor of the effective area approach, $g_e(p_s)$, can be expressed as

$$g_e(p_s) = 1, \quad \text{if} \quad p_s \geq p_c$$
$$g_e(p_s) = 0, \quad \text{if} \quad p_s < p_c.$$

The $g(p_s)$ and $g_e(p_s)$ near the junctions are plotted in Fig. 12. The error of the effective area approach can be derived as

$$L_{error} = \int (g_e(p_s(V_{GL}, x)) - g(p_s(V_{GL}, x)))\, dx. \quad (14)$$

As shown in Fig. 12, the L_{error} is less than 0.001 μm.

C. Potential Perturbation Near the Source/Drain Junctions

$I_{cp,\,max}(x)$ in (7) is assumed to be a constant to derive (11). However, $I_{cp,\,max}(x)$ is not exactly constant along the channel, even the interface-trap density is constant. At the proximity of source and drain junctions, the nonsteady-state emission times for electrons and holes are different. We can estimate the charge pumping current density using the equations derived by Groeseneken [14]:

$$I_{cp,\,max}(x) = 2q\overline{D_{it}}f\, k_B T[ln\,(v_{th} n_i \sqrt{\sigma_n \sigma_p}) + 0.5\, ln\,(t_{em,\,e}(x)\, t_{em,\,h}(x))]. \quad (15)$$

The induced error can be approximated by

$$L_{error} = \int_{x_1}^{x_2} (I_{cp,\,max0} - I_{cp,\,max}(x))/I_{cp,\,max0}\, dx \quad (16)$$

where x_1 and x_2 are the edges of the effective area and $I_{cp,\,max0}$ is the charge pumping current density near the middle of the channel. The L_{error} is about 0.001 μm at $V_{GL} = -1.5$ V and $V_D/V_S = 3$ V.

From the above discussions, we conclude that 0.01 μm accuracy of ΔL extraction is feasible using the proposed charge pumping method.

V. Conclusion

The charge pumping technique is shown to be a simple and accurate method to extract the effective channel length of MOSFET's. Similar to the capacitance method, no I-V models are needed for the ΔL extraction. It is shown that the proposed novel method is a direct measurement of L_{eff} with much higher resolution. The derived results are clear, reliable, and independent of the measurement biases. With the knowledge of the device dopant profiles, 0.01 μm accuracy can be achieved easily. In addition, this method is applicable to either n- or p- channel, conventional or LDD, surface or buried channel MOSFET's.

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