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High Performance Ir/TiPrO/TaN MIM Capacitors for Analog ICs Application

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In this paper, we demonstrate high quality material TiPrO and high density $Ti_xPr_{1-x}O$ (x~0.67) metal-insulator-metal (MIM) capacitors using high work function (~5.3 eV) Ir top electrode. Very low leakage current of 7×10^{-9} A/cm^2 at -1 V and high 16 fF/μm^2 capacitance density are achieved for 400 °C anneal TiPrO, which also meets the ITRS goals (at year 2018) of 10 fF/μm^2 density and $J/(C\cdot V) < 7$ fA/(pF·V) . Furthermore, the improved high 20 fF/μm^2 capacitance density TiPrO MIM is obtained at higher annealing temperature, where low leakage current 1.2×10^{-7} A/cm^2 is measured at -1 V. These good performances indicate TiPrO MIM is suitable for analog/RF ICs Applications.

Introduction

The technology evolution for Metal-Insulator-Metal (MIM) capacitors (1)-(16) requires higher capacitance density with low leakage current at evaluating temperature (17). Besides, the MIM capacitors are also used for Analog/RF ICs and DRAM technology. Low voltage- or temperature-dependence of capacitance (*VCC* or *TCC*) is also needed for the multi-functional System-on-Chip (SoC) applications. Since the capacitance density equals $\varepsilon_0\kappa/t_\kappa$, the only method for higher density, without increasing unwanted leakage current by decreasing dielectric thickness (t_κ), is to use higher dielectric constant dielectric (κ) materials. Thus, the MIM capacitors are continuously integrated with higher κ dielectrics from Al_2O_3 (κ=10) (3), HfO_2-Al_2O_3 (κ~15) (9), ZrO_2, TiTaO (13), TiHfO (15) and TiNiO (κ~36) (16). One major drawback for higher-κ MIM device is the large leakage current due to low conduction band offset (ΔE_C) at evaluated temperature that leaks out the stored charge in capacitor (Q=C·V). However, increasing dielectric constant (κ) usually leads to decreasing of ΔE_C with respect to the electrode. This is also the challenge of flash memory but unavoidable during IC operation due to large circuit density and high DC power dissipation due to leakage current. The possible solution is using high bandgap (E_G) dielectric to form the laminate (9) or multi-layer structure (10), but the overall κ value and voltage coefficient of capacitance (*VCC*) are largely degraded. Pr_2O_3 is one of attractive rare earth metal oxides with many merits such as large conduction band offset (ΔE_C~ 1 eV) (18), moderate dielectric constant (κ~15) and large bandgap (E_G ~4 eV) (18). Furthermore, significantly larger Gibbs free energy of Pr_2O_3 (+106 kcal/mol) (19)-(21) in contact with silicon than that of TiO_2 (+7.5 kcal/mol), Ta_2O_5 (-52 kcal/mol), HfO_2 (+47 kcal/mol) and NiO (-51.4 kcal/mol) can avoid metal/oxide inter-diffusion or chemical reaction caused by oxygen exchange, which not only reduce the interfacial layer between dielectric layer and bottom electrode but also performs excellent thermal stability. Combining above advantages of high-κ Pr_2O_3 with the high dielectric constant of TiO_2 (~50), mixed TiPrO dielectric overcomes the issue of leakage current without scarifying capacitance density.

In this paper, we report Ir/TiPrO/TaN capacitors with capacitance density of 16 fF/μm^2 and further improved capacitance density of 20 fF/μm^2 using higher annealing temperature. High-k values 26-32 were obtained in this work by using mixed $Ti_xPr_{1-x}O$(x~0.67). By using high-κ TiPrO with the ratio of Ti to Pr 2:1 and high work function electrode Ir, we can achieve high capacitance density of 16-20 fF/μm^2, and low leakage current of 7×10^{-9} A/cm^2 to 1.2×10^{-7} A/cm^2 at 25 °C at-1 V, small quadratic *VCC* (α) of 1720~2174 ppm/V^2, and small *TCC* of 532~758 ppm/°C. The lower leakage shows improved quadratic *VCC* (α) and *TCC*, which are important for analog/RF functions. It would be important to note that the device shows large orders of magnitude lower thermal leakage at 25 °C and 125 °C at -1V than our previous work on TiTaO (13) and TiNiO (16), at comparable capacitance density. Such good device integrity is due to the mixed high-κ TiPrO (κ~26-32) with larger bandgap (E_G~4 eV), larger high-κ/Si conduction band offset (ΔE_C~1 eV) and larger Gibbs free energy (+106 kcal/mol) of Pr_2O_3.

Experimental Procedure

After depositing 2 μm SiO_2 on a Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN/Ta bi-layers. The Ta was used to reduce the series resistance and the TaN served as a barrier layer between the high-κ TiPrO and the Ta electrode. The TaN was treated by NH_3 plasma nitridation at 100W to improve the bottom interface. The TaN layer with NH_3 surface nitridation (22)-(23) can improve electrode stability and prevent CET (capacitance equivalent thickness) degradation by forming interfacial TaON during post-deposition anneal (PDA). Then 14 nm thick $Ti_xPr_{1-x}O$ (x~0.67) dielectric layer were deposited on the TaN/Ta electrode by PVD respectively followed by 400 °C and 430 °C oxidation and annealing step to reduce the leakage current. Finally, Ir was deposited and patterned to form the top capacitor electrode. The fabricated devices were characterized by *C-V* and *J-V* measurements using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter.

Results and Discussion

Fig.1 shows the *C–V* characteristics of Ir/TiPrO/TaN capacitors, which were processed differently. The capacitance density increased from 16 to 20 fF/μm^2 with increasing O_2 PDA temperature from 400 °C to 430 °C. In Fig. 2a and 2b, we perform the *J–V* characteristics of the TiPrO MIM capacitors with capacitance density of 16 fF/μm^2 and 20 fF/μm^2 respectively, measured at 25 and 125 °C. The good *J-V* and *C-V* characteristics are obtained with the use of high work function top electrode Ir (~5.27 eV) and nitrogen plasma (N^+) treatment on bottom electrode TaN. The nitrogen plasma (N^+) treatment reduces the interfacial layer growing between the bottom electrode TaN and TiPrO layer during oxygen annealing (22)-(23). It is very important to note that the TiPrO MIM with capacitance density of 16 fF/μm^2 achieves the ITRS goals (at year 2018) (17) of 10 fF/μm^2 density and $J/(C\cdot V) < 7$ fA/(pF·V). This excellent result indicates TiPrO is a potential material candidate for future electrical device application.

To further evaluate the device performance, Fig. 3a and 3b show the temperature-dependent *J-V* characteristics of TiPrO MIM capacitors at capacitance density of 16 and 20 fF/μm^2, respectively. The leakage current increases rapidly with increasing

temperature; however, the high temperature operation is unavoidable for modern high performance IC due to the increasing power consumption. In addition, the unwanted interfacial layer between bottom electrode and high-κ dielectric layer would lead to surface roughness between them. The interface layer make the thermal leakage current of the electron bottom injection (voltage= 0~3 V) slightly larger than the leakage of the electron gate injection (voltage= 0~-3 V), which can be observed in Fig. 2. Thus, we only perform the *J-V* characteristics under reverse bias in Fig. 3.

The examination of device performance with comparable capacitance density at 25 °C is performed in Fig. 4. We can see the leakage current of TiPrO MIM is significantly lower than TiO_2 MIM and our previous work TiTaO MIM and TiNiO MIM, at a comparable capacitance density. The lower leakage current of TiPrO MIM is due to the higher ΔE_C between metal and high-κ TiPrO interface, higher bandgap of high-κ TiPrO and larger Gibbs free energy of Pr_2O_3, which reduce the leakage current exponentially. We also plot *ln(J)* versus $E^{1/2}$ relation in Fig. 5. The temperature-dependent leakage current in MIM is typically governed by Schottky emission (SE) or Frenkel-Poole (FP) as:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \quad [1]$$

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} \quad [2]$$

The η is equal to 1 or 4 for FP or SE case and K_∞ is the high-frequency dielectric constant (=n^2). The refractive index n =2.3 for $Ti_xPr_{1-x}O$ (x~0.67) is reasonable by linear interpolation of the reported 2.57 for TiO_2 and 1.75 for Pr_2O_3. From Fig. 5a and 5b, the leakage at 25 °C from Ir top electrode on TiPrO/TaN is ruled by SE at low field and FP at high field by trap-conduction. Besides, the leakage at 125 °C is also dominated by SE at low field and FP at high field. This result would be due to the large ΔE_C of TiPrO and the larger energy barrier ϕ_b of Ir electrode. The different slopes γ, for the *SE* and *FP* cases arise from the different energy barriers V_b, corresponding to the work function of the metal-electrode/dielectric in the *SE* case or the trap energy level in the dielectric for the *FP* case. The fits to the experimental data give slope of 1.56×10^{-5} or 3.14×10^{-5} eV $(m/V)^{1/2}$ for the *SE* or *FP* mechanisms respectively, by using n =2.3 for TiPrO in the above equations.

Since the conduction mechanism at high electric field for Ir electrode on TiPrO is governed by Frenkel-Poole Emission, we plotted the *ln(J/E)-1/KT* relation of TiPrO in Fig. 6a to extract the trapping level. The larger Gibbs free energy of Pr_2O_3 (+106 kcal/mol) contacted with silicon avoids metal/oxide inter-diffusion. Besides, the binding energy between Praseodymium and Oxygen (928 eV~970 eV) (24) is significantly larger than the binding energy between Nickel and Oxygen (855 eV~861 eV) (25) and that between Tantalum and Oxygen (~530 eV) (26). The both reasons indicate the interfacial trap density of TiPrO (between dielectric and electrode) would be smaller than that of other dielectrics, such as TiTaO and TiNiO. Thus, the trapping level in the TiPrO dielectric will be larger than TiTaO (~0.3 eV) (13) and TiNiO (16). For illustration, we also plot this relation of our previous work TiNiO MIM in Fig. 6b. Compared with Fig. 6a and 6b, the trapping level of TiPrO about 0.43 eV is significantly larger than the

trapping level of TiNiO by about 0.17 eV. This result also explains why TiPrO MIM can achieve near 2.5 orders of magnitude lower leakage current at -1V at 125 ^{o}C than TiNiO MIM, which is shown in Fig. 6c. In Fig. 7, the SE barrier height (V_b) at 125 ^{o}C was extracted from $ln(J/T^2)$-$E^{1/2}$ plot. The value for V_b is 1.53 eV for TiPrO device at 125 ^{o}C with Ir top electrode.

VCCs are important parameters for MIM capacitor applications, and can be obtained by fitting the measured data with a second order polynomial equation of $C(V) = C(\alpha V^2 + \beta V+1)$, where C is the zero-biased capacitance, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Fig. 8a shows $\Delta C/C$-V characteristics of Ir/TiPrO/TaN capacitors fitted by the above mentioned equation. The lower leakage using high ϕ_m (Ir) also improves ΔC/C, and VCC α due to the trap-related mechanism (3)-(4), (7)-(8). It should be noted that since linear VCC β can be cancelled by circuit design (27), α is important for Analog/RF functions and it is strongly dependent on electric filed and dielectric physical thickness. To the best of our knowledge, the MIM capacitor with combined higher ϕ_m and higher κ dielectric is the only method to achieve lower thermal leakage and better *VCC* α simultaneously without sacrificing capacitance density in multi-layer or laminate structure. Fig. 8b shows the normalized capacitance versus measured temperature (*TCC*) of MIM capacitor for capacitance density 16 fF/μm^2 and 20 fF/μm^2, respectively. We can find the *TCC* showed increase with the increase of the measured temperature (14).

Amorphous dielectrics like TiPrO have some advantages over crystalline materials including low processing thermal budget, conventional electrode, high uniformity and scalability to very thin layers, which is suitable for BEOL and manufacture. Table I summarizes important device data for MIM capacitors with various high-κ dielectrics and work-function metals. The thermal leakage decreases largely with increasing ϕ_m of metal electrode from TaN to Ir. High 16~20 fF/μm^2 density, reasonable quadratic VCC α of 1702~2174 ppm/V^2 and low 7×10^{-9}~ 1.2×10^{-7} A/cm^2 leakage current at 25 ^{o}C at-1 V are simultaneously measured in Ir/TiPrO/TaN devices, which are comparable with or better than the best reported data in literature (17). In summary, amorphous dielectric TiPrO shows good thermal stability, leakage current, and scalability to very thin layers issue. Besides, TiPrO is also the better amorphous dielectric material than TiO_2, TiTaO and TiNiO.

Conclusion

Due to large conduction band offset (~1 eV), large bandgap (3~4 eV), large Gibbs free energy (~106 kcal/mol) of Pr_2O_3, large binding energy of Pr-O (928 eV~970 eV) and high dielectric constant (~50) of TiO_2, the mixed high-κ TiPrO is a potential material candidate for electronic devices. Dielectric material TiPrO shows its excellent amorphous material properties and gives enough high κ value (κ~26-32). By applying the good properties to our MIM device, the device not only shows apparently lower thermal leakage than other dielectric MIM at comparable capacitance density but also meets the ITRS requirement. Such good device integrity indicates TiPrO dielectric is attractive as a very promising dielectric material for Analog/DRAM applications.

Acknowledgments

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TABLE I. Comparison of important device data for MIM Ir/TiPrO/TaN capacitor with various high-κ dielectrics and work-function metals.

	ITRS @2018	Tb-HfO_2 (6)	Al_2O_3-HfO_2 (9)	Nb_2O_5 (12)	TiTaO (13)	TiNiO (16)	**This work**	
Process Temp. (^oC)	—	420	420	420	400	400	400	430
Top metal	—	Ta	TaN	Ta	Ir (5.3 eV)	Ni (5.1 eV)	Ir*(5.3 eV)	Ir*(5.3 eV)
Lower metal	—	TaN	TaN	Ta	TaN	TaN	TaN	TaN
C Density ($fF/\mu m^2$)	10	13.3	12.8	17.6	23	17.1	**16**	**20**
J (A/cm^2) @25 ^oC	—	1×10^{-7} (2 V)	8×10^{-9} (2 V)	7×10^{-7} (1 V) 8×10^{-6} (2 V)	2×10^{-6} (1 V) 2×10^{-5} (2 V)	7.7×10^{-6} (1 V) 5.6×10^{-5} (2 V)	7×10^{-9} (1 V) 1.1×10^{-7} (2 V)	1.2×10^{-7} (1 V) 7.4×10^{-6} (2 V)
J (A/cm^2) @125 ^oC	—	2×10^{-7} (2 V)	6×10^{-9} (1 V) 5×10^{-8} (2 V)	4×10^{-7} (1 V) 1×10^{-5} (2 V)	—	—	3.6×10^{-7} (1 V) 7.2×10^{-6} (2 V)	5.8×10^{-7} (1 V) 3.8×10^{-4} (2 V)
J/(C•V) (fA/[pF•V])	< 7	37.9 @2 V	3.1 @2 V	14.5 @1.5 V	870 @1 V	4530 @1 V	3.45 @1 V	45 @1 V

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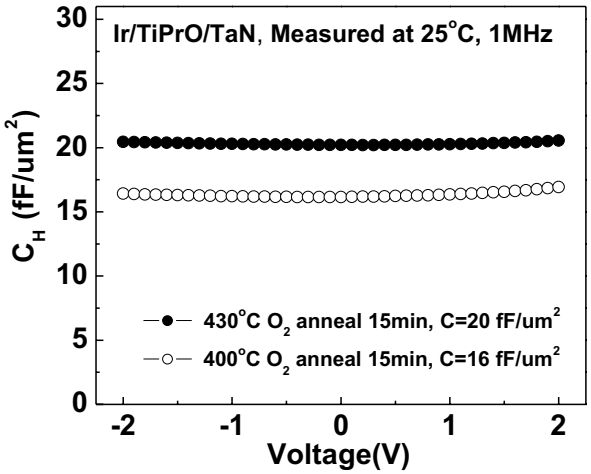


Figure 1. *C-V* characteristics of Ir/TiPrO/TaN capacitors with different annealing temperature measured at 1 MHz.

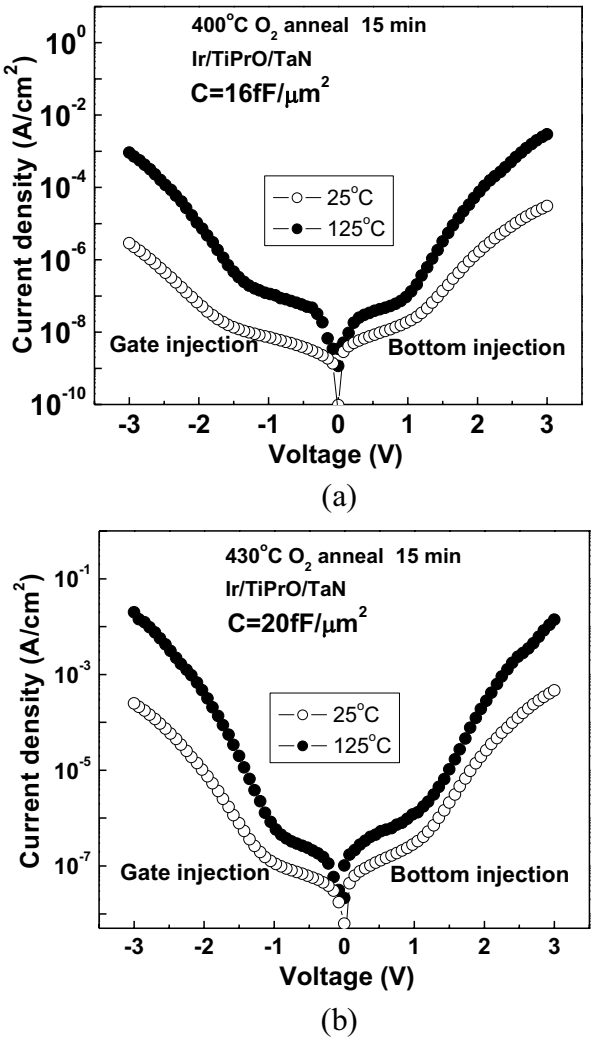


Figure 2. *J-V* characteristics of Ir/TiPrO/TaN capacitors with different capacitance density (16 fF/μm^2 and 20 fF/μm^2) measured at 25 °C and 125 °C, respectively.

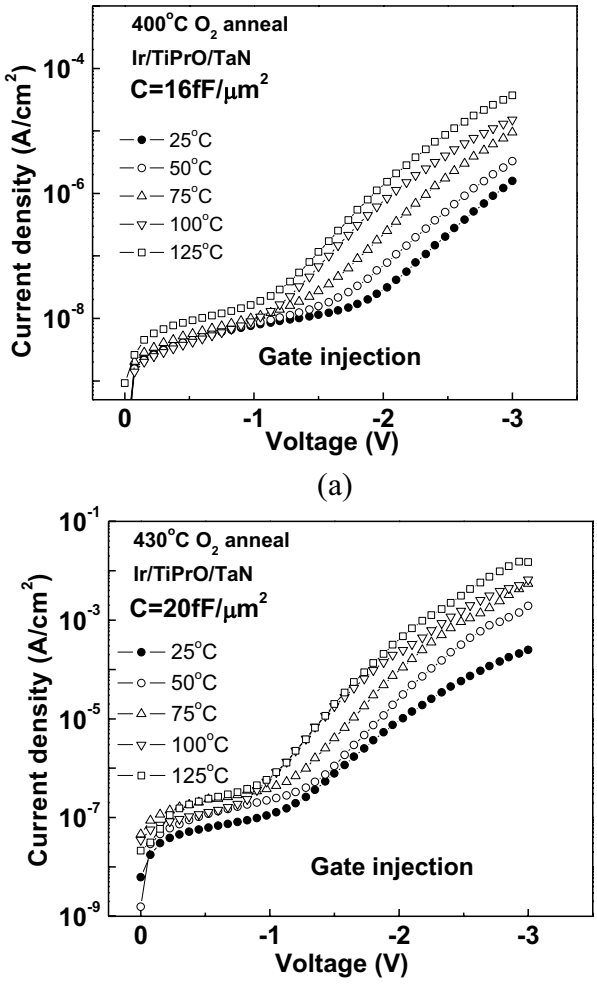


Figure 3. *J-V* characteristics of Ir/TiPrO/TaN capacitors for capacitance density with (a) 16 fF/μm^2 and (b) 20 fF/μm^2 measured from 25 °C to 125 °C, respectively.

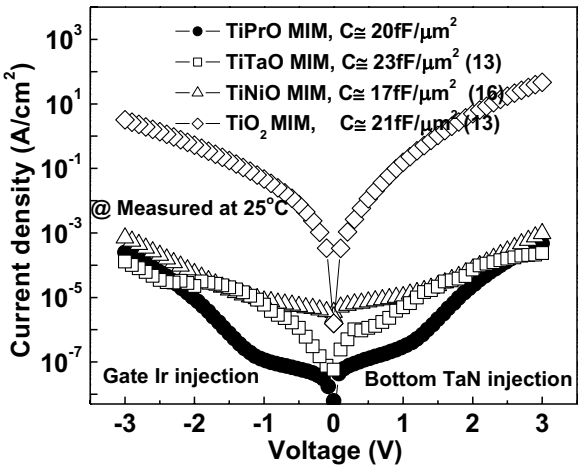


Figure 4. The comparisons of *J-V* for different high-κ material capacitors, at comparable capacitance density. The leakage current of TiPrO MIM is significantly lower than TiO_2 and previous work TiTaO and TiNiO MIM.

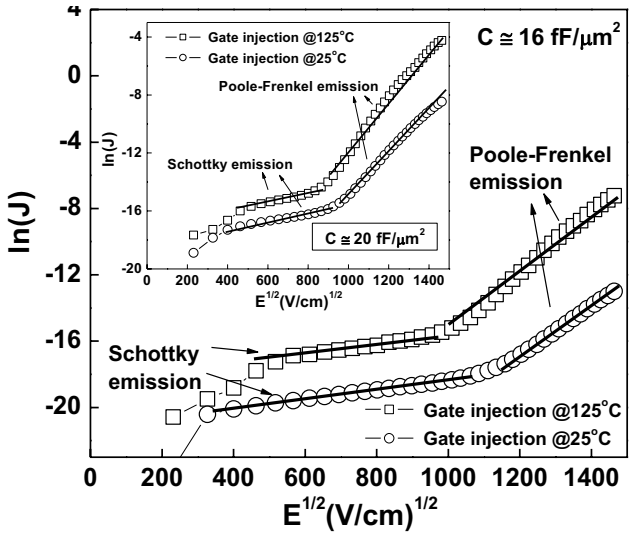
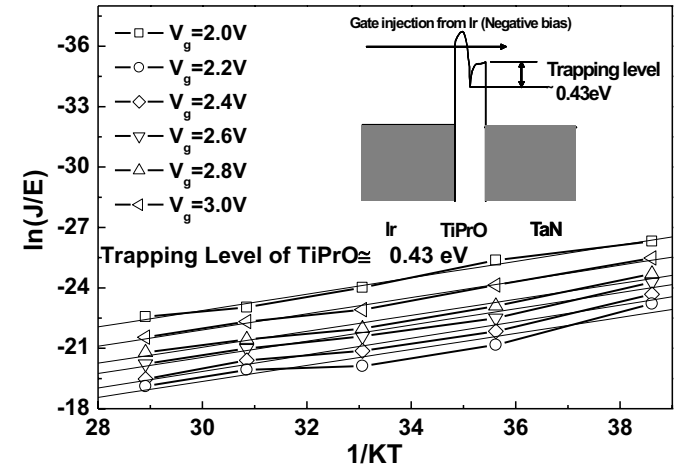
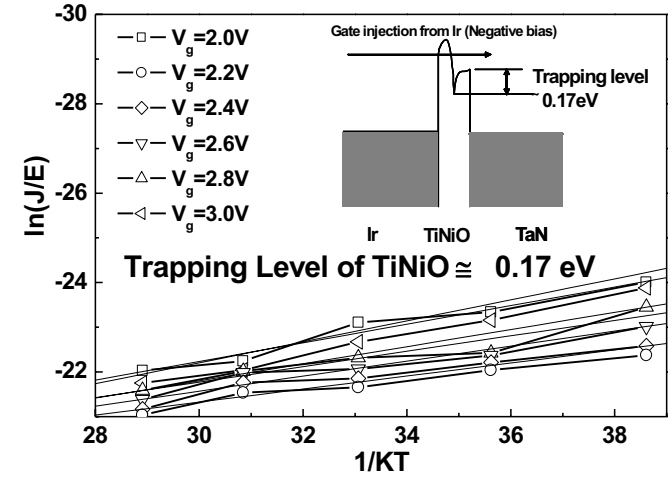


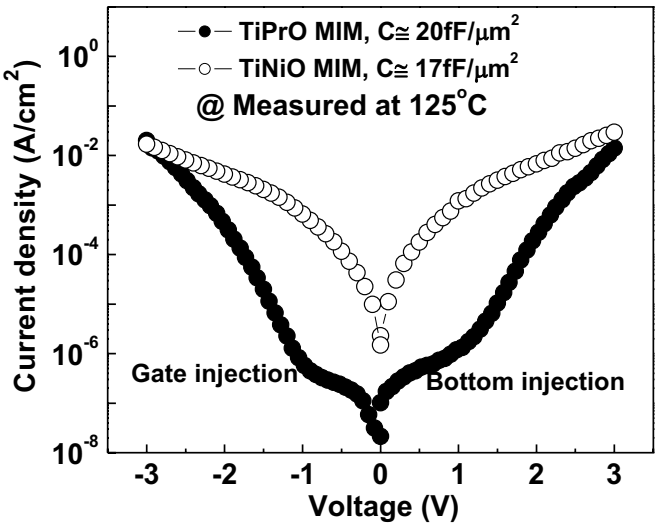
Figure 5. Plot of *ln(J)* versus $E^{1/2}$ under electron injection from top electrode for Ir/TiPrO/TaN capacitors with capacitance density of 16 fF/μm^2 and capacitance density of 20 fF/μm^2 is shown in the inserted figure. The SE emission fitting at low electric field and the FP emission fitting at high electric field are measured at 25 ^{o}C and 125 ^{o}C, respectively.



(a)



(b)



(c)

Figure 6. The FP conduction fitting at high field for (a) Ir/TiPrO/TaN capacitor and (b) Ir/TiPrO/TaN capacitor are shown. The leakage current measured at 125 °C for Ir/TiPrO/TaN and Ir/TiNiO/TaN MIM are also shown in (c).

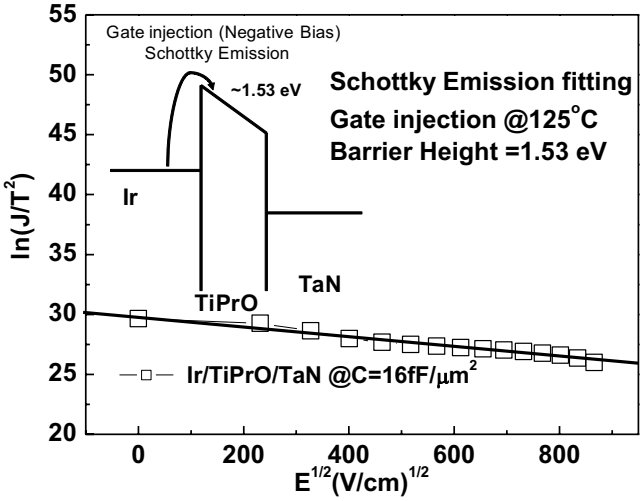


Figure 7. The SE emission fitting of Ir/TiPrO/TaN capacitors at low electric field.

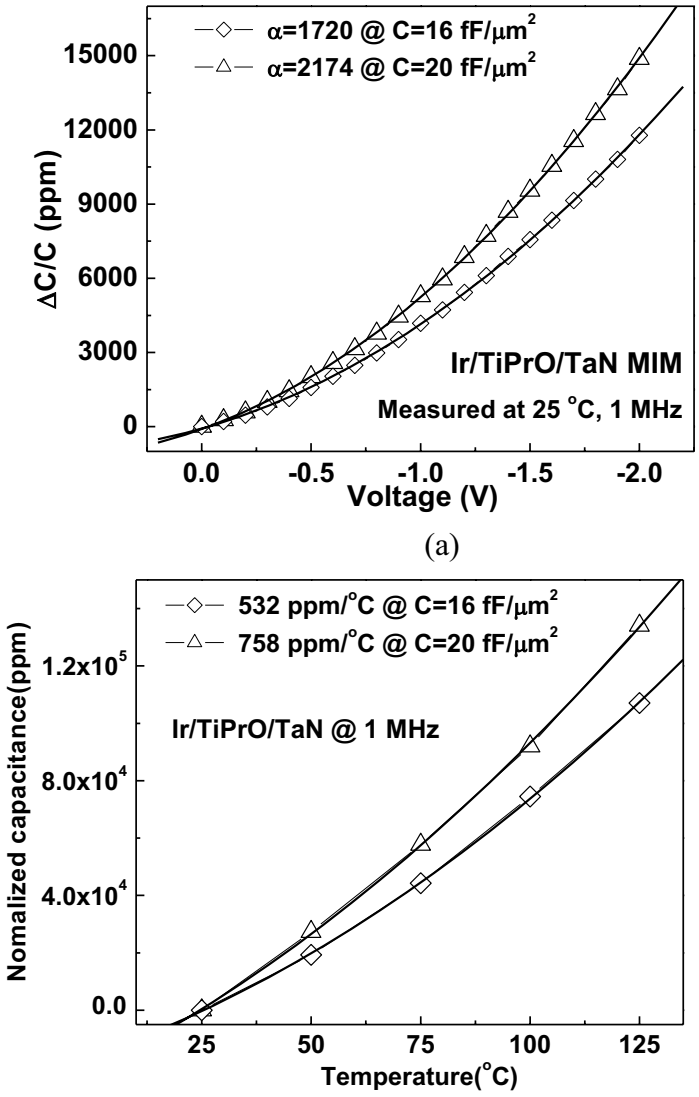


Figure 8. (a)*ΔC/C -V* characteristics of Ir/TiPrO/TaN capacitors for different capacitance density. (b)The temperature-dependent normalized capacitance for Ir/TiPrO/TaN capacitors for different capacitance density.