Thin Polyoxide on the Top of Poly-Si Gate to Suppress Boron Penetration for pMOS

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***Abstract*— A method of using a thin oxide on the top of the poly-Si gate to getter fluorine for BF_2^+ in pMOS is proposed and demonstrated. Due to less amount of fluorine in the poly-Si as well as in the gate oxide, the boron penetration through the gate oxide is suppressed. The MOS capacitors fabricated by using this method show less shifts and distortion on C-V curves and better electrical characteristics.**

I. INTRODUCTION

RECENTLY, the p^+ poly-Si gate has been widely used for submicrometer CMOS technology to avoid the short-channel effects [1]. However, the boron used to dope this p^+ poly-Si gate is easy to penetrate through the gate oxide into the underlying Si-substrate, especially for the BF_2^+ implanted poly-Si gate. This will cause the positive shift of the threshold voltage, increments of the gate oxide electron trapping rate, and the P-channel inverse subthreshold slope. Previously, we had proposed a stacked poly-Si gate structure with an ultra-thin oxide inserted in-between to suppress the boron penetration [2], [3]. It had also been found that the inclusion of a $TiSi_2$ salicide prior to the gate implantation can eliminate the fluorine-related V_{fb} shifts [4] and fluorine is primarily to segregate at the oxide and the defect region after the post-implant annealing process [5]. In this work, a thin polyoxide is to replace the $TiSi_2$ salicide on the top of the poly-Si gate. In the post-implant annealing process, this thin oxide will getter fluorine out of the poly-Si gate, hence reduce the amount of fluorine in the poly-Si as well as in the gate oxide [3]. Thus, the enhancement on the boron penetration by fluorine is reduced [6]. Hence, the gate oxide prepared by this process has better electrical characteristics.

II. EXPERIMENTALS

The p^+ poly-Si gate MOS capacitors were fabricated on (100), $5 \sim 10$ Ω-cm, n-type Si wafers with a 88 Å gate oxide. The gate oxide was grown in diluted dry O_2 ($O_2/N_2 = 1/6$) at 900°C and annealed in N_2 at the same temperature for 15 min. After that, 3000 Å of undoped polysilicon was deposited and a thin polyoxide ($\sim$100 Å) was grown on the top of the deposited polysilicon layer (OTP) in O_2 at 900°C for 10 min. For comparison, control samples without the polyoxide were also fabricated. Then, all the samples were implanted with BF_2^+ of a dose 5×10^{15} cm^{-2} at 50 KeV, and annealed at 800°C in O_2 for 30 min first and then at 900°C in N_2 for 10, 20, 30, and 40 min respectively, to activate the implanted dose. The oxidizing anneal at 800°C was intended to grow a thin polyoxide on the poly-Si gate to prevent the boron out-diffusion during the latter inert annealing at 900°C. After the polyoxide was removed, Al was deposited and annealed at 400°C in N_2 for 30 min to make capacitors. The area of capacitors was 4.324×10^{-3} cm^2. The boron and fluorine profiles of the samples were analyzed with SIMS and a Keithley C-V analyzer was used to measure the high frequency (100 KHz) and quasi-static capacitances of the capacitors.

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III. RESULTS AND DISCUSSIONS

Fig. 1 shows the fluorine and boron profiles of the OTP and control samples after annealing, respectively. The control sample had two fluorine peaks, one at the location of the gate oxide, and the other at the BF_2^+ implant region. For the OTP sample, the fluorine peak at the implant region disappeared and the fluorine which segregated at the gate oxide had a lower peak, about 0.7 of that of the control sample. The polyoxide on the top of the poly-Si had acted as a sink for fluorine, thus reduced the fluorine in the poly-Si gate and the gate oxide. Since fluorine enhances the boron diffusion in oxide [6], this less fluorine in the OTP gate had a less boron penetration [3]. This is seen that the OTP sample had the boron peak at the gate oxide about 0.65 of that of the control sample and a shallower profile in the Si substrate.

Fig. 2(a) and (b) show the normalized high frequency (100 KHz) and quasi-static C-V curves for the OTP and control samples annealed for different times, respectively. It is seen that the shifts of the C-V curves, which were due to the negative fixed charge generated by F-B complexes and a very shallow P-type layer in the silicon substrate as a result of the boron penetration [4], of the OTP samples were much less than those of control samples. For the control sample of 40 min annealing, the high frequency C-V curve had distorted so much that a shallow P-type layer had formed, due to the boron penetration, underlying the gate oxide and the sample acted like an nMOS capacitor. However, for the OTP sample of the same annealing, the shape of the high frequency C-V curve stayed still the same except that it shifted to the right a little.

It is noted that although the polyoxide on the poly-Si gate gettered boron thus reduced the amount of boron in the poly-Si

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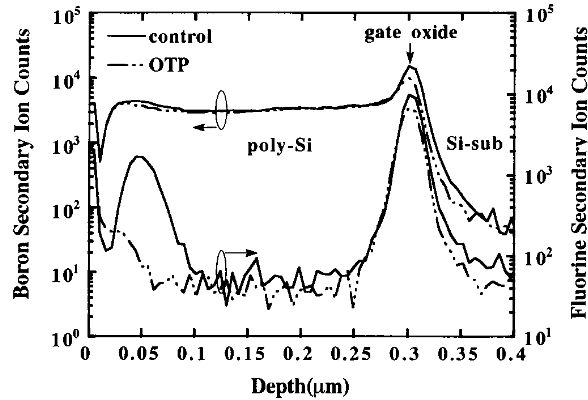


Fig. 1. The SIMS depth profiles of fluorine and boron for the OTP and control samples annealed in O_2 at 800°C for 30 min then in N_2 at 900°C for 40 min after the BF_2^+ implantation.

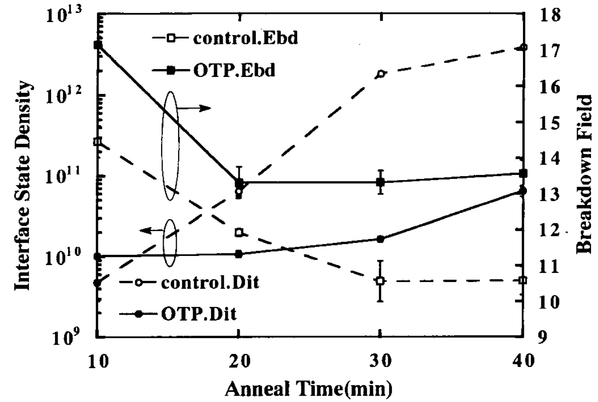
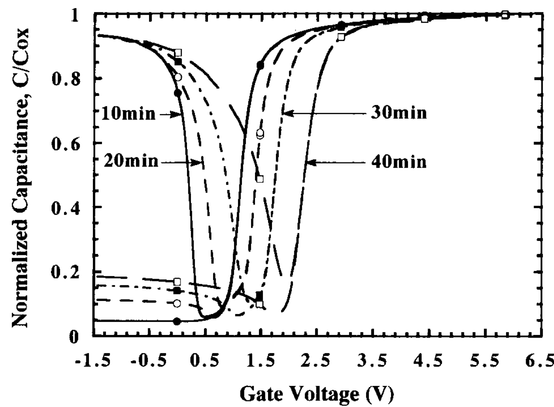
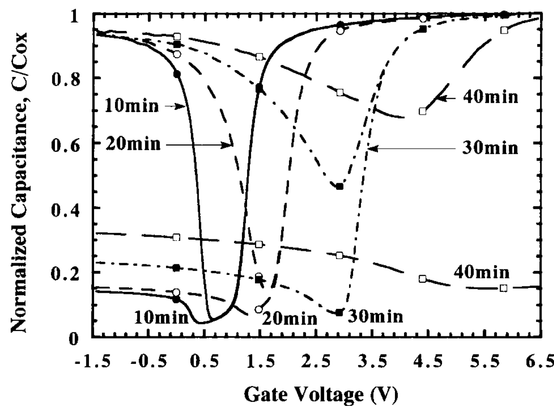


Fig. 3. The mid-gap interface state densities (state/cm^2/eV) and breakdown fields (MV/cm) for the OTP and control samples, annealed at 900°C for different times.



(a)



(b)

Fig. 2. The normalized high frequency (100 KHz) and quasi-static C-V curves of the (a) OTP samples, and (b) control samples annealed at 900°C for different times.

gate, the poly-Si depletion effect did not occur, which is seen from the C-V curves for the OTP samples. The $C_{qs,inv}/C_{ox}$ values were all between 0.95 and 0.935, and were nearly the same for both the OTP and the control samples.

Fig. 3 lists the mid-gap interface state densities (D_{it}) and the breakdown fields (E_{bd}) for the OTP and control samples annealed for different times. For both D_{it} and E_{bd}, the OTP samples had much better results than that of control samples. This was due to the less fluorine, consequently, less boron at the gate oxide [6], which kept a better integrity of the oxide, for the OTP samples.

IV. Conclusion

In conclusion, by growing a thin polyoxide on the top of the poly-Si gate, as the experimental results show, can getter fluorine out of the poly-Si gate during the post-implant annealing process. As a result, less fluorine segregate at gate oxide, and thus the boron penetration is suppressed. This improves the characteristics and also the reliability of pMOSFET.

References

[1] H. H. Tseng, P. J. Tobin, F. K. Baker, J. R. Pfiester, K. Evans, and P. L. Fejes, "The effect of silicon gate microstructure and gate oxide process on threshold voltage instabilities in p$^+$-gate p-channel MOSFET's with fluorine incorporation, *IEEE Trans. Electron Devices,* vol. 39, p. 1687, 1992.

[2] S. L. Wu, C. L. Lee, and T. F. Lei, "Suppression of the boron penetration induced Si/SiO_2 interface degradation by using a stacked-amorphous-silicon film as the gate structure for pMOSFET," *IEEE Electron Device Lett.,* vol. 5, p. 160, 1994.

[3] Y. H. Lin, C. L. Lee, T. F. Lei, and T. S. Chao, "Suppression of boron penetration in pMOS by using oxide gettering effect in poly-si gate," *Extended Abstracts Conf. SSDM,* Japan, p. 685, 1994, and *Jpn. J. Appl. Phys.,* vol. 34, part 1, no. 2B, p. 142, 1995.

[4] F. K. Baker, J. R. Pfiester, T. C. Mele, H.-H. Tseng, P. J. Tobin, J. D. Hayden, C. D. Gunderson, and L. C. Parrillo, "The influence of fluorine on threshold voltage instabilities in P$^+$ polysilicon gate P-Channel MOSFETs," *IEDM,* p. 443, 1989.

[5] T. Kinoshita, M. Takakura, S. Miryazaki, S. Yokoyama, M. Koyanagi, and M. Hirose, "Chemical bonding features of fluorine and boron in BF2$^+$-ion-implanted Si," *Jpn. J. Appl. Phys.,* vol. 29, p. L2349, 1990.

[6] J. J. Sung and C. Y. Lu, "A comprehensive study on p$^+$ polysilicon-gate MOSFET's instability with fluorine incorporation," *IEEE Trans. Electron Devices,* vol. 37, p. 2312, 1990.