A Physically-Based Built-in Spice Poly-Si TFT Model for Circuit Simulation and Reliability Evaluation

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Abstract

A Poly-Si TFT model for circuit simulation in Spice is presented, combined with a device degradation model for the first time to evaluate the circuit reliability. Both I-V and C-V models for the whole device operating regime have been developed. In the I-V model, emphasis has been taken to derive the mobility degradation induced by the grain boundary potantial barrier height and trap density. The small geometry effect, off-state current and the parasitic BJT effect are also considered in the model. Good agreements between modeled and experimental data were achieved. To evaluate the circuit reliability after electrical stress, the device reliability model has also been developed. Finally, simulation a 27-stage ring oscillator has been demonstrated, which shows delay time of about 1nsec per stage.

1. Introduction

Basically, the poly-Si TFT operates with a floating substrate and its characteristics are easily affected by the imperfection of grain boundaries. Therefore, the characteristics of the poly-Si TFT's cannot be accurately modeled by the bulk MOSFET model. Recently, some circuit models for poly-Si TFT's are either just modification of bulk MOS models [1] or incomplete [2]. We are in lack of a complete model which can be implemented in commercially available circuit simulator so far. On the other hand, the lack of an accurate circuit model will be the major factor limiting TFT circuit integration. Therefore, it is essential to establish a precise poly-Si TFT model for circuit simulation use.

In this paper, we present a complete poly-Si TFT I-V and C-V models for circuit simulation in Spice. The basic formulation of the device model is similar to those we developed in our previous works [3-5] on MOS devices with additions of several special features inherent in TFT. In addition, the device behavior of TFT is different from that of conventional MOS device after electrical stress. This has been considered for developing TFT device degradation model. Typical examples for circuit level reliability simulation using Spice has also been demonstrated.

2. Formulation of the I-V Model

The present I-V model is built upon an MOS device model that we developed in [3-5] with additions of the small geometry effect, off-state current, parasitic BJT effect, and more importantly a physically-based mobility model by considering the grain boundary trap state and the potential barrier effect. The drain current from off-state, through subthreshold and weak inversion, to the linear region and saturation region are given as follows.

A. Linear Region

The linear region drain current of a TFT is given by

$$I_{DS} = \mu W Q_n(y) dV_C/dy. \quad (1)$$

Here, Q_n is the inversion layer charge given by

$$Q_n = C_{OX}(V_{GS}-V_T- aV_c). \quad (2)$$

The mobility of electrons at the grain boundary is less than the grain mobility and is dominated by the trap state and the poptential barrier height. Also the vertical field scattering effect can be neglected since with increasing gate voltages the potential barrier height (Ψ_b) at grain boundaries is reduced and results in more conducting carriers. Therefore, a reasonable channel mobility μ is proposed as the following expression:

$$\mu = \mu_b \exp(-q\Psi_b/kT) \quad (3)$$

and

$$\mu_b = \mu_0/[1+E_y/E_c][1+\alpha N_t(L)]. \quad (4)$$

Combining eqs. (1) to (4) and integrating it over the channel length, we have the linear region drain current

$$I_{DS} = \mu_n C_{ox}(W/L)[(V_{GS}-V_T)V_{DS} - 0.5\, aV_{DS}^2] \quad (5)$$

where

$$\mu_n = \frac{\mu_0 \exp\left(\frac{-\theta}{V_{GS}-V_T}\right)}{(1+\eta V_{DS})(1+\alpha N_t(L))} \quad (6)$$

$$V_T = V_{FB} + \phi_S + K(L,W)\sqrt{\phi_S} - \sigma V_{DS} \quad (7)$$

$$K(L,W) = K - Q_t(L,W)/(C_{ox}\sqrt{\phi_S}) \quad (8)$$

$$Q_t = -qN_t(L) \quad (9)$$

$$N_t = t_{inv}/W_g \cdot N_{trap}(L) \quad (10)$$

and

$$a = 1 + 0.5\frac{K(L,W)}{\sqrt{\phi_s}}\left(1 - \frac{1}{(1.744+0.836\phi_s)}\right). \quad (11)$$

In the above formulation, the threshold voltage of the poly-Si TFT considers the small geometry factor K(L,W) and the effect of trap density (N_t). The short channel effect of the V_T is shown in Fig. 1 and the corresponding N_t distribution with channel length is also shown.

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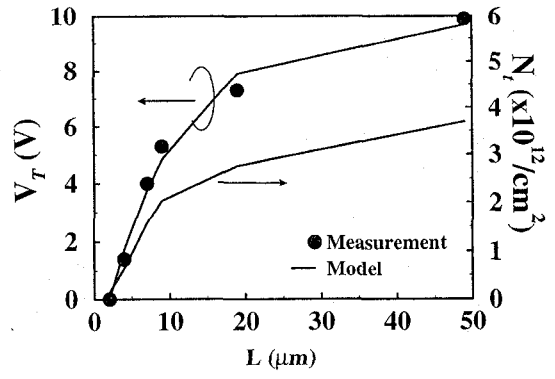

Fig.1 The channel length dependence of the threshold voltage and the corresponding trap densities.

B. Saturation Region

In the saturation region, not only the channel length modulation (CLM) but also the BJT induced currents are included and summarized as follows:

$$I_{DS} = \frac{I_{DSAT}}{1 - \Delta L/L} + I_{DS(BJT)} \quad (12)$$

where

$$V_{DSAT} = (V_{GS} - V_T)/a \quad (13)$$

$$\Delta L = \sqrt{2\,\varepsilon_s\,(V_{DS} - V_{DSAT})/(q\,N_{sub})} \quad (14)$$

and

$$I_{DS\,(BJT)} = \beta_i\, I_{DSAT}\cdot(V_{DS} - V_{DSAT}) \cdot exp\left((-\Delta L\,\alpha_i)/(V_{DS} - V_{DSAT})\right). \quad (15)$$

The parasitic BJT effect in poly-Si TFT's mainly results from the extra holes accumulated in the floating substrate and leads to a forward bias of the source junction. The BJT effect induced current is decsribed by eq. (15). Figs. 2-3 show the I-V characteristics of the modeled and experimental data for L=10μm and 1μm respectively, in which the BJT effect induced kink current is obviously more severe for the 1μm device. Our model shows good accuracy for both long- and short-channel devices.

C. Weak Inversion Region

The weak inversion region consists of the subthreshold region and the transition region(between subthreshold and linear region). For the subthreshold region, its current can be derived as [4]

$$I_{sub} = \mu_n C_{OX} W/L \cdot f\,(1 - exp\,(-qV_{DS}/kT))\,(q/kT)^2 \cdot exp\,[m\,(V_{GS} - V_T)] \quad (16)$$

where m is the subthreshold slope and f is a fitting parameter. The current in the transition is given by the sum of strong inversion region current, eq.(5), and the weak inversion current, i.e.,

$$I_{DS} = I_{D,S} + I_{D,W} \quad (17)$$

where

$$I_{D,W} = I_{sub}\, I_T/(I_{sub}+I_T)\,. \quad (18)$$

The difficulty in developing the transition current is to ensure its continuity in that region. Here, we proposed an artifact by finding the current I_T empirically from experimentally measured I-V data [6]. The modeled and measured I-V results are compared in Fig.4. The smooth I-V curve in the transition region ensures good convergence of Spice program.

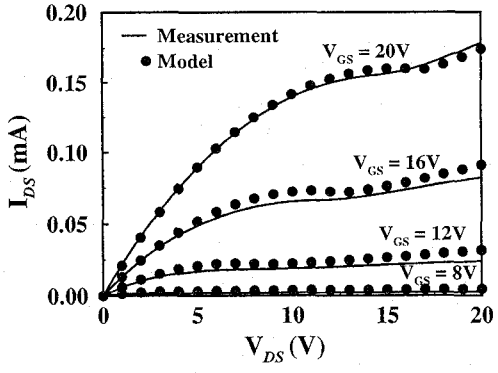

Fig. 2 The modeled and measured output characteristics of an n-channel TFT with W/L=10μm / 10μm.

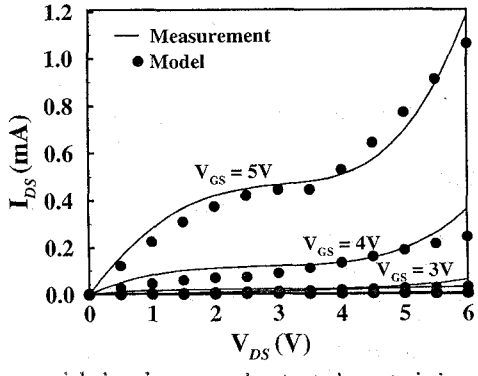

Fig. 3 The modeled and measured output characteristics of an n-channel TFT with W/L=10μm / 1μm.

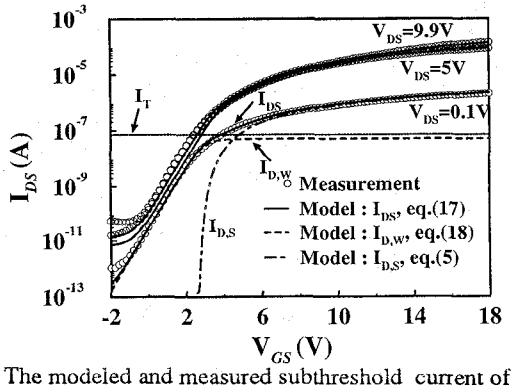

Fig. 4 The modeled and measured subthreshold current of an n-channel TFT at various V_{DS}, in which smooth transition is achieved.

D. Off-state Region

The current in the off-state is given by

$$I_{off} = I_0 \exp(\alpha\sqrt{E}) \quad (19)$$

where

$$E=\sqrt{E_{//}^2+E_{\perp}^2},\ E_{//}=\sqrt{\frac{2qN_{sub}(V_{bi}+V_{DS})}{\varepsilon_{si}}},\ E_{\perp}=\frac{V_{DG}-V_{FB}}{3t_{ox}}. \quad (20)$$

Fig. 5 shows the modeled and experimental I-V curves throughout the whole regimes for various V_{DS}. The off-state current can be well modeled according to the Poole-Frenkel mechanism [7] rather than the common band-to-band tunneling mechanism in MOSFET [1] since in TFT's, large amounts of defects in the channel and thicker gate oxide make the trap-assisted thermionic field emission much easier than the field-induced tunneling.

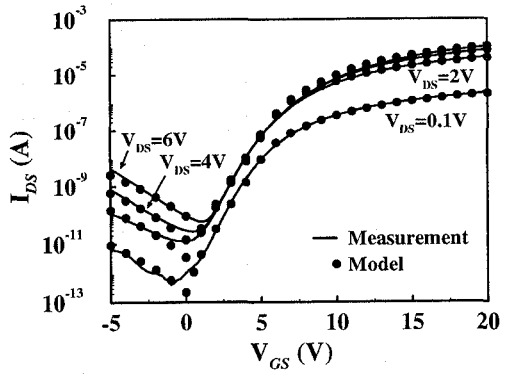

Fig. 5 The modeled and measured transfer curves of an n-channel TFT at various V_{DS}.

3. The Capacitance Model

The capacitances associated with a TFT device include the gate-drain (or gate-source) overlap capacitance and the intrinsic capacitance. Since the TFT operates with a floating body, there are 12 intrinsic capacitance components required for implementation in Spice. According to the charge density equations for gate (q_G) channel (q_C) and bulk charges (q_b), we may derive the total charges Q_G, Q_c, and Q_B using the BSIM approach [8]. Also, based on the charge partition scheme, we may further divide Q_C into Q_S and Q_D. Charge conservation gives $Q_G+Q_B+Q_S+Q_D= 0$. We can easily calculate these 12 intrinsic capacitances in a TFT device through $C_{ij}= \partial Q_i/\partial Q_j$, where i,j= G,D,S or i= B. However, there is considerable BJT current added to the drain current due to the floating body which induces a certain amount of capacitance. This BJT effect induced additional capacitance only occurs in the saturation region and is summarized in Table 1. Fig. 6(a) shows the modeled and experimental C_{GD} and C_{GS} versus V_{GS} characteristics, which is similar to those of MOSFET but with smaller capacitance values. Fig. 6(b) shows the modeled and experimental C_{GD} dependence on the V_{DS}, where we see clearly that the increase of C_{GD} at high drain bias is due to the BJT effect.

$$q_{c1}(y) = \frac{I_{DS(BJT)}}{W\, v(y)} \text{ (linear region)} \quad q_{c2}(y) = \frac{I_{DS(BJT)}}{W\, v_{sat}} \text{ (saturation region)} \quad (21)$$

$$Q_{G(BJT)} \approx -Q_{C(BJT)} = -W\int_0^{L-\Delta L} q_{c1}(y)dy - W\int_{L-\Delta L}^{L} q_{c2}(y)dy$$

$$= -C_{ox}W[(L-\Delta L)/V_{DSAT}-\mu_n/\upsilon_{SAT}][(V_{GS}-V_T)V_{DSAT}-0.5aV_{DSAT}^2]$$

$$-[C_{ox}W\mu_n/\upsilon_{SAT}][(V_{GS}-V_T)V_{DS}-0.5aV_{DS}^2] \quad (22)$$

Table 1 Developed BJT effect induced intrinsic capacitances.

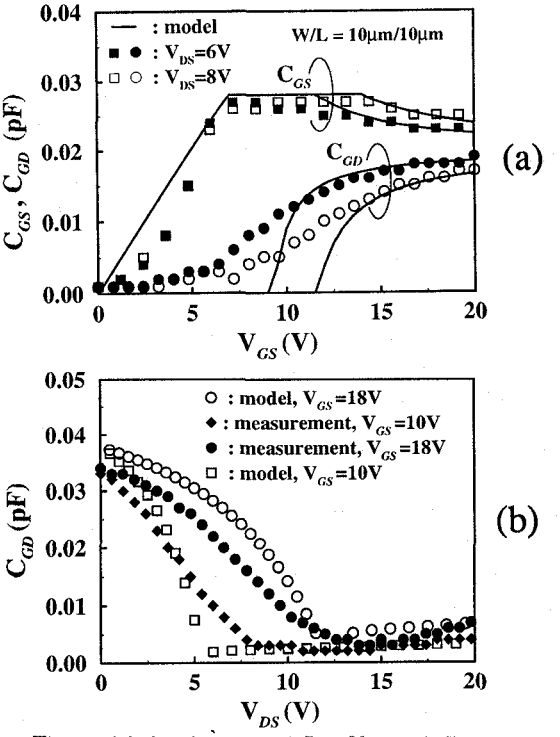

Fig. 6 (a) The modeled and measured C_{GD}-V_{GS} and C_{GS}-V_{GS} characteristics at various V_{DS}.
(b) The modeled and measured C_{GD}-V_{DS} characteristics at various V_{GS}.

4. Degradation Model and Reliability Evaluation

In general, conventional device degradation mechanism can be one of the following possibilities such as defect state generation in the channel, charge trapped in the gate oxide and the hot carrier effect. In poly-Si TFT's, the hot carrier effect is not severe enough as compared with other degradation mechanisms. The defect state generation in the channel is the main degradation mechanism of poly-Si TFT's. Hack *et al.*

[9] pointed out that the device degradation after bias stress is mainly due to the creation of metastable gap states in the channel. These states are uniformly distributed in the channel and can be annealed by the sintering step. To investigate the device degradation after bias stress, assuming a power law of the device current degradation, the trap state of a device after bias stress can be represented by

$$N_t' = N_t + N_t\frac{\Delta I_{DS}/I_{DS}}{1 - \Delta I_{DS}/I_{DS}} = N_t + N_t\frac{At^n}{1 - At^n}. \qquad (23)$$

The degradation rate is dependent on V_{GS}, L and t_{ox}, which are closely related to the degradation factor (A). Fig. 7 shows the dependence of drain current degradation and the generated trap states (N_t') on the stress time. Fig. 8 shows the comparison of modeled and experimental I-V characteristics before and after the stress. The modeled I-V is calculated by substituting N_t', eq. (23), into eq. (6), the mobility term, to predict the drain current degradation. To evaluate the reliability of TFT circuits, a 27-stage ring oscillator circuit before and after stress has been simulated. Fig. 9 shows the simulated output waveforms, in which the stress effect causes an increasing propagation delay time of about 1ns per stage. Results in Fig. 10 from the measurement show that the maximum allowable V_{DS} is about 9V at the lifetime of 10 years. The bias stress of devices at $V_{DS}=V_{GS}$ is used with the lifetime chosen at $\Delta I_D/I_D=10\%$.

In conclusion, we have successfully developed a Spice compatible TFT model feasible for circuit simulation and reliability evalution. It includes a complete set of device I-V, C-V, and trap state induced reliability model throughout the whole device operating regime. Parameter extraction has also been developed to determine the model parameters and so the model accuracy can be preserved. Several benchmark circuits have also been tested using the modified Spice code. Moreover, a device degradation model has also been implemented successfully in the simulator to evaluate the TFT circuit reliability.

Acknowledgments

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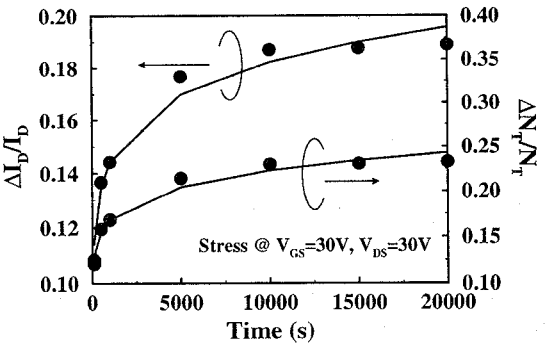

Fig. 7 The dependence of current degradation and trap state generation on the stress time.

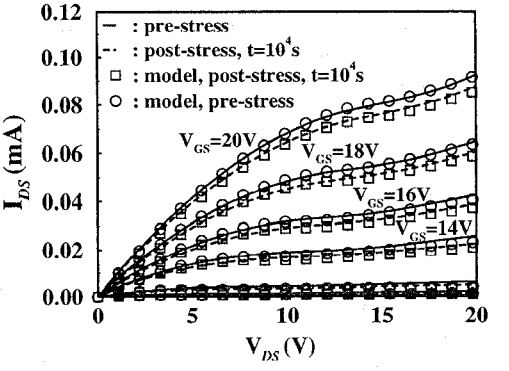

Fig. 8 Comparison of the modeled and measured device I-V characteristics before and after the stress.

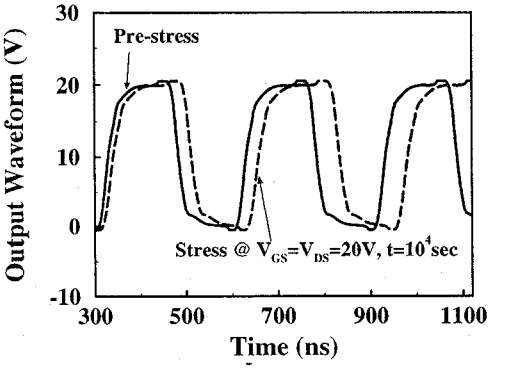

Fig. 9 The simulated output waveforms of a 27-stage ring oscillator circuit before and after the stress.

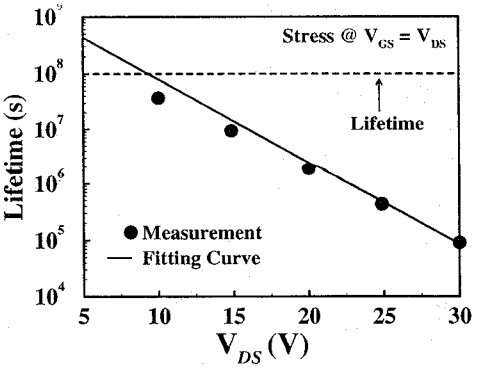

Fig. 10 The measured dependence of lifetime on the stress biases ($V_{DS}=V_{GS}$).